VDEC設立20周年記念行事
東京大学武田先端知ビル、2017年1月20日

スピントロニクス素子と集積回路応用

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東北大学 スピントロニクス学術連携研究教育センター
東北大学 国際集積エレクトロニクス研究開発センター
東北大学 原子分子材料科学高等研究機構

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Work supported in part by the FIRST Program from JSPS, ImPACT from JST,
and by the R & D for Next-Generation Information Technology of MEXT

http://www.csis.tohoku.ac.jp/

TOHOKU UNIVERSITY

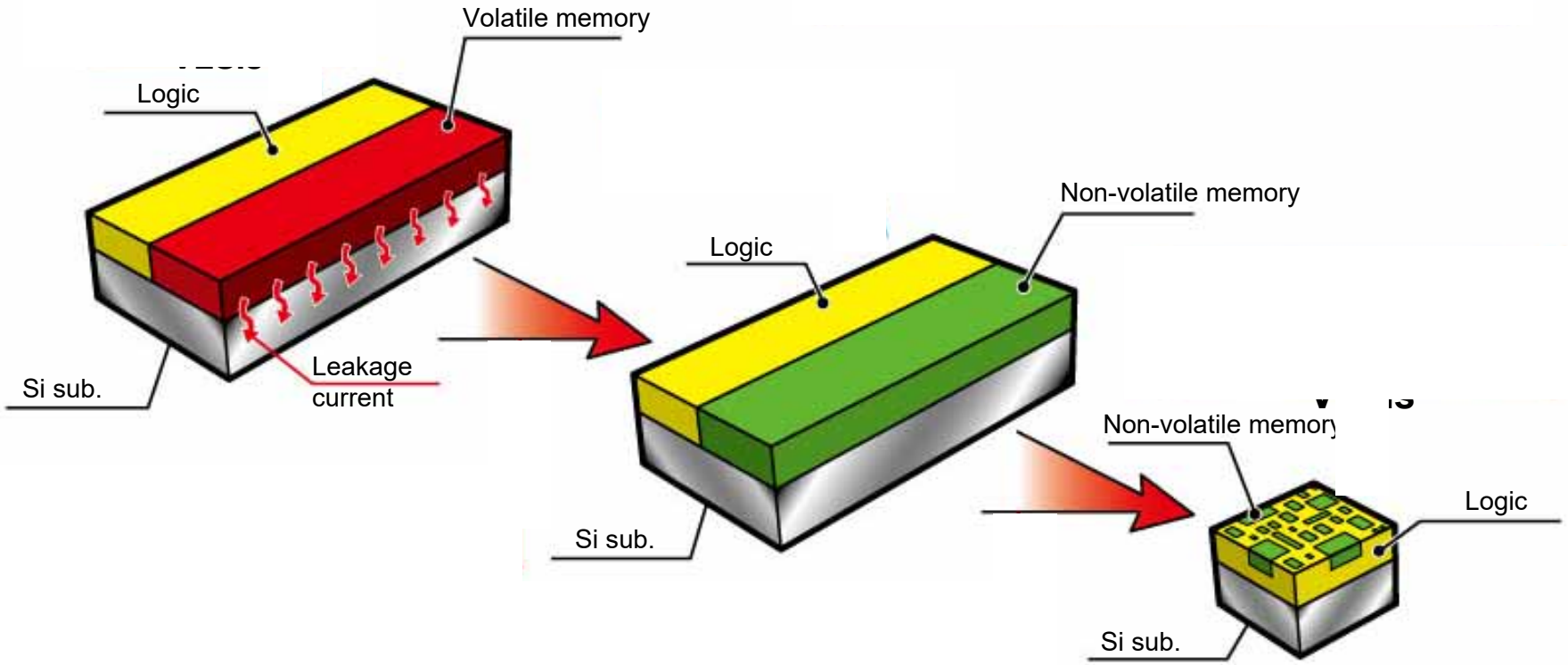
Current Working Memories

DRAM: dense, $6F^2$

SRAM: fast, $200F^2$

Volatile

Toward Nonvolatile CMOS VLSI



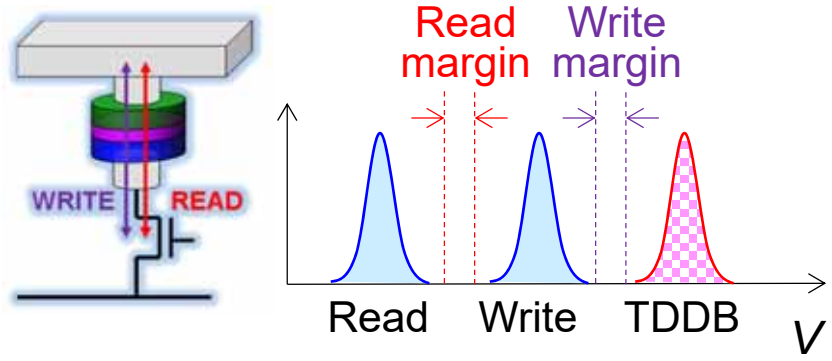
Nonvolatile memory that is

- scalable
- fast
- *virtually infinite endurance*
- back-end-of-line compatible
- low resistance

Two versus Three terminal: operation window

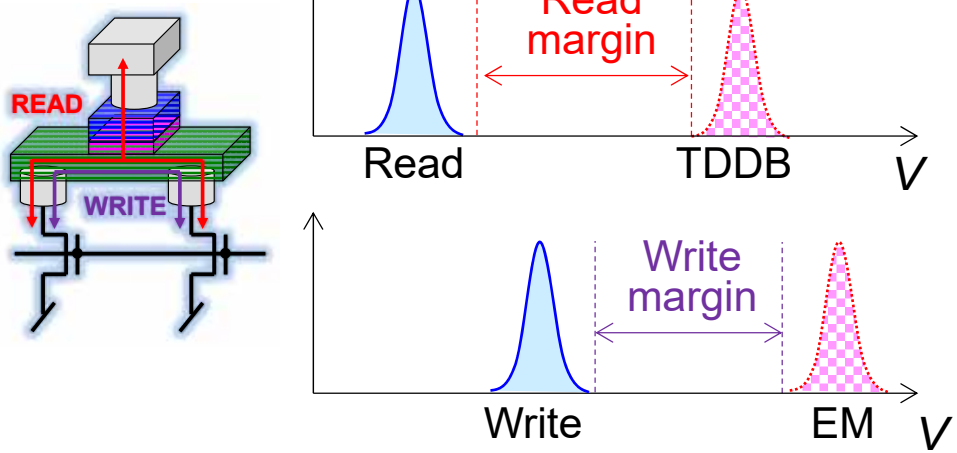
Two-terminal

(Magnetic Tunnel Junction)



6-8 F²

Three-terminal



12 F²

◆**Three-terminal:** Different READ and WRITE current path

- ➢ High-speed operation, Simple and small-area peripheral circuits
  ←Wide waveform tolerance owing to the large operation window
- ➢ Long lifetime ← Much less stress on tunnel barrier
- ➢ Low error rate ← No read disturbance, overdrive possible

- TDDB : Time-dependent dielectric breakdown
- EM : Electromigration

S. Fukami et al. IEEE Trans. Magn. **50**, 3401006 (2014).

2 terminal device

Magnetic Tunnel Junction (Spin-transfer torque)

I_{c0} and $\Delta = E/k_B T$

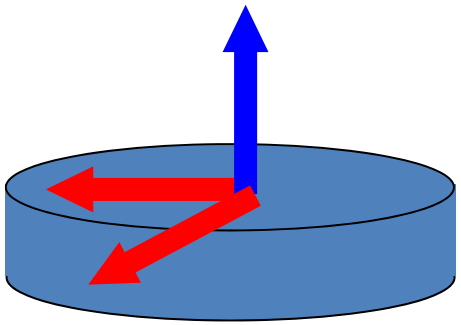
perpendicular

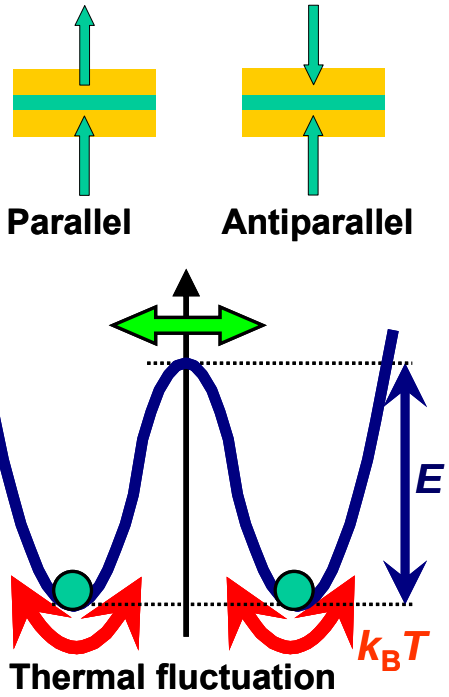
$$E = K_{eff} V$$

$$I_{C0} = \frac{2\alpha\gamma e}{\mu_B g}\left(K_{eff} V\right)$$

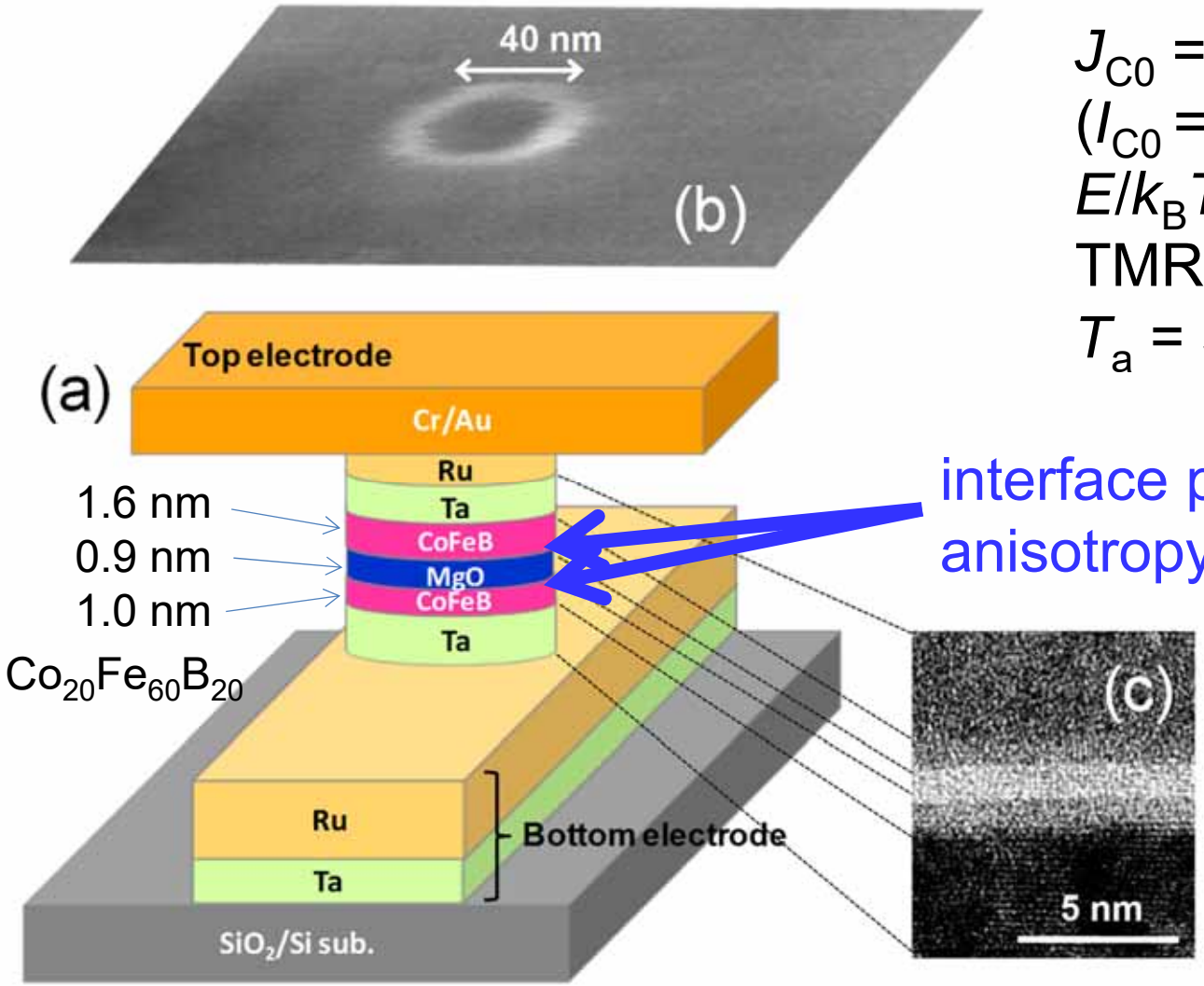
$$\propto \alpha E$$

$$K_{eff} = K_{eff}$$





Perpendicular MgO-CoFeB MTJ

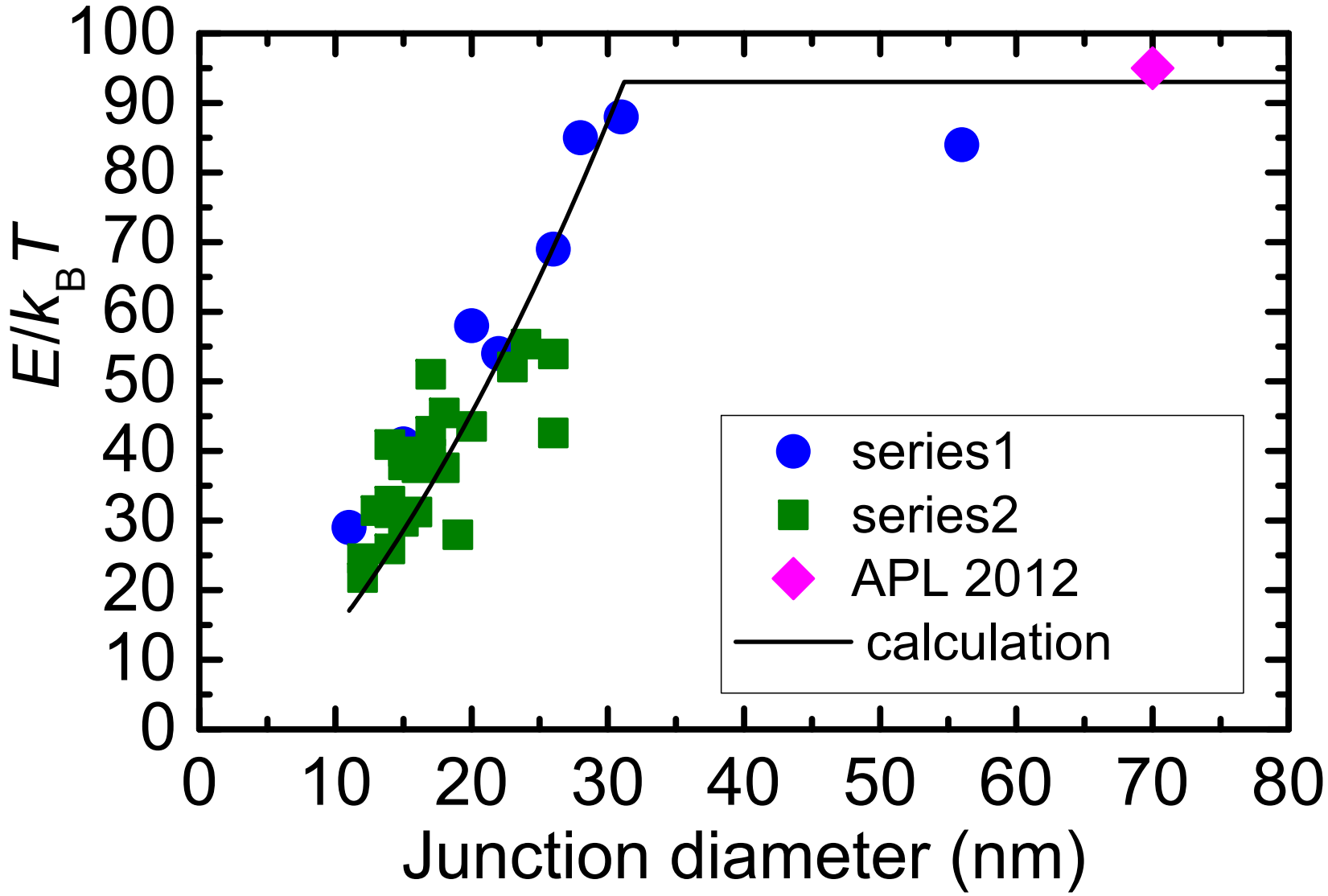


J_{C0} = 3.8 MA/cm^2
(I_{C0} = 48 μA)
E/k_BT ~ 40
TMR ratio = 110%
T_a = 350°C

interface perpendicular anisotropy

S. Ikeda *et al.*, Nature Mat. **9**, 721 (2010)

E/k_BT



H. Sato *et al.*, Appl. Phys. Lett. **105**, 062403 (2014)

STT-MRAM

PUBLIC RELEASE: 16-MAY-2016

New technology reduces 30 percent chip area of STT-MRAM while increasing memory bit yield by 70 percent

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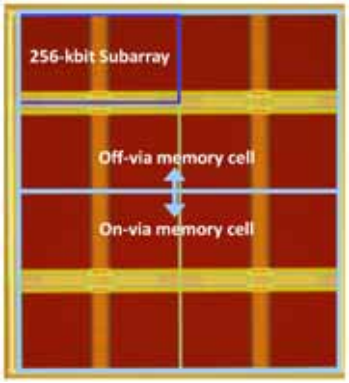
H. Koike et al. IMW2016



MRAM-info

Everspin starts sampling 256Mb ST-MRAM chips, plans 1Gb chips by the end of 2016

Apr 15, 2016 EverSpin MRAM production STT-MRAM

Everspin to show world's fastest SSD

Non-volatile RAM -- NVRAM for short -- is the Next Big Thing in digital storage. Everspin has announced that the industry's first Perpendicular Magnetic Tunnel Junction chip is now shipping. The company will demo the worlds's fastest SSD using it next week.

NEWS

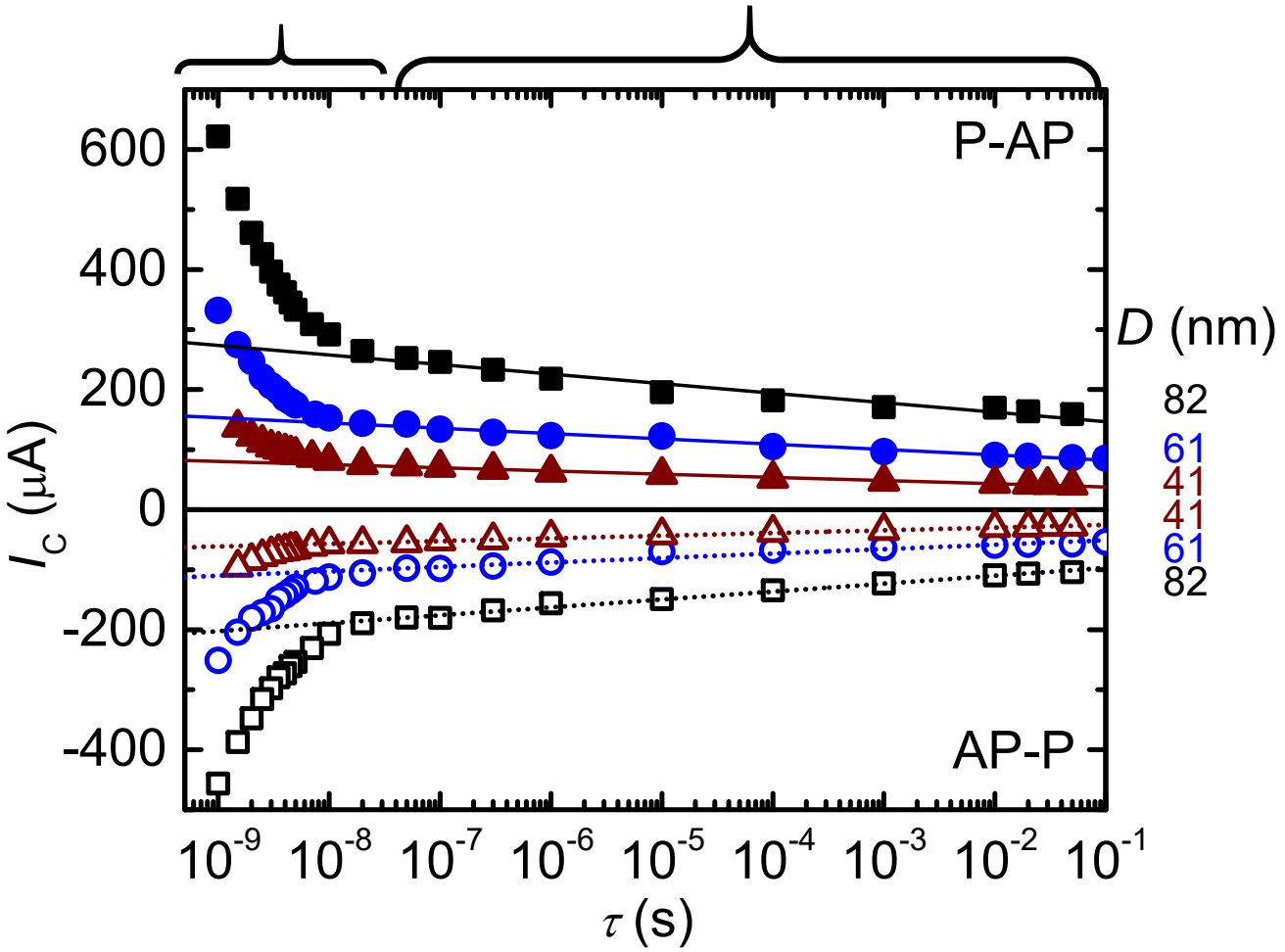
IBM and Samsung achieve breakthrough on flash killer for wearables, mobile devices

Computerworld | Jul 12, 2016 1:18 PM PT

Qualcomm, GlobalFoundries, TSMC, TDK Headway, Toshiba, Hynix, Avalanche, …
TEL, AMAT, CANON-ANELVA, …
Tohoku University, IMEC

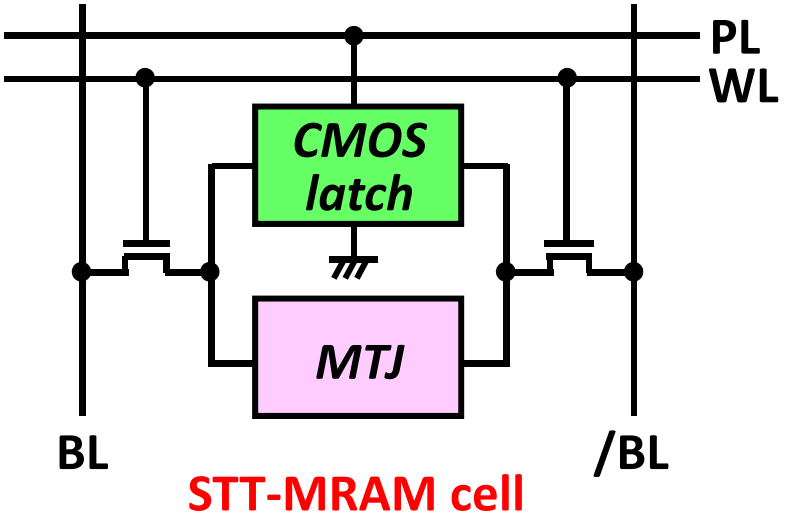
Switching current versus switching speed

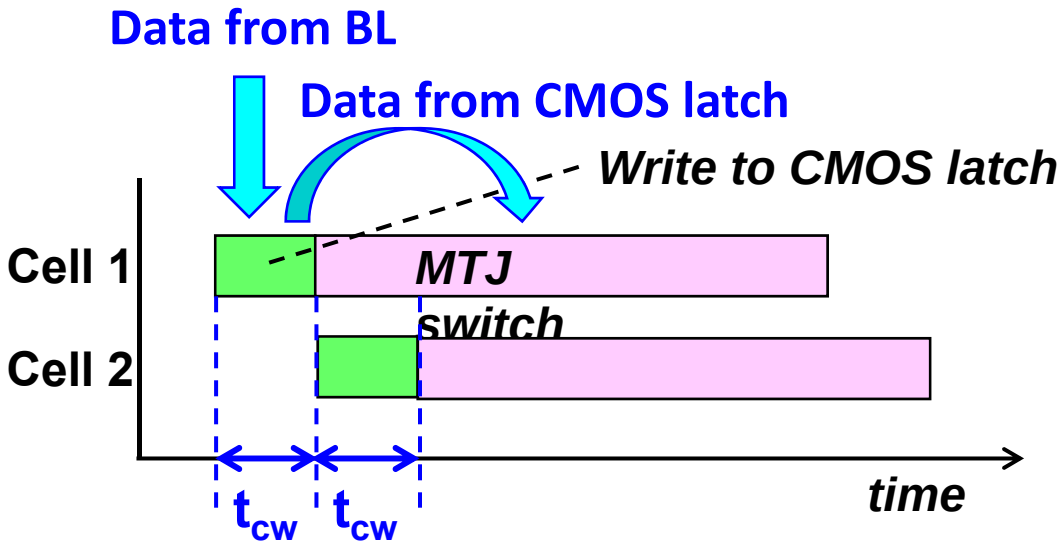
$$\frac{1}{\tau} = \frac{1}{A}\left(I - I_{C0}\right)$$



N. Ohshima *et al.*, 76th JSAP fall meeting, 14p-2J-8.

Background Write

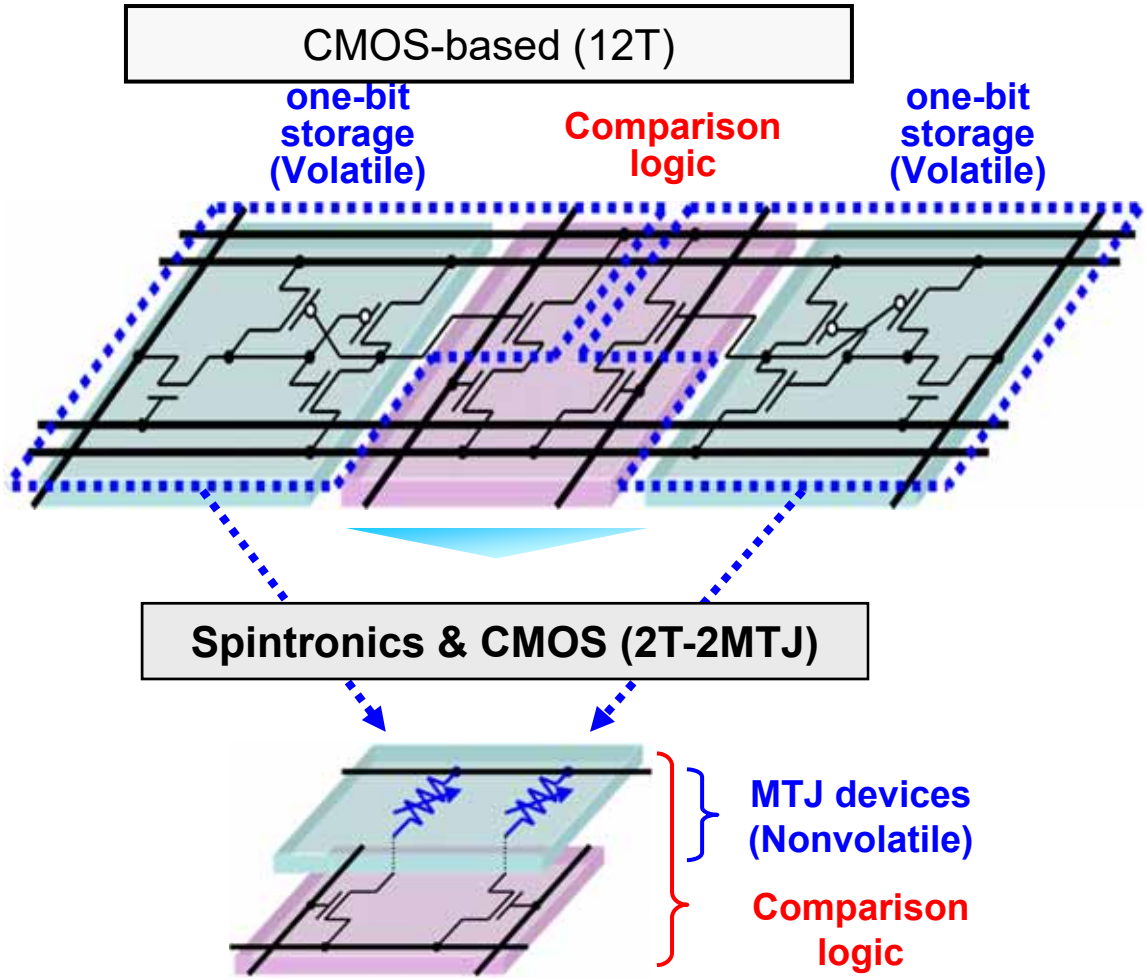




T. Ohsawa et al., Symp. VLSI Circuits, pp. C110-C111, June 2013. @Endoh Gr. of Tohoku Univ.

Ternary CAM Cell

T. Hanyu Group

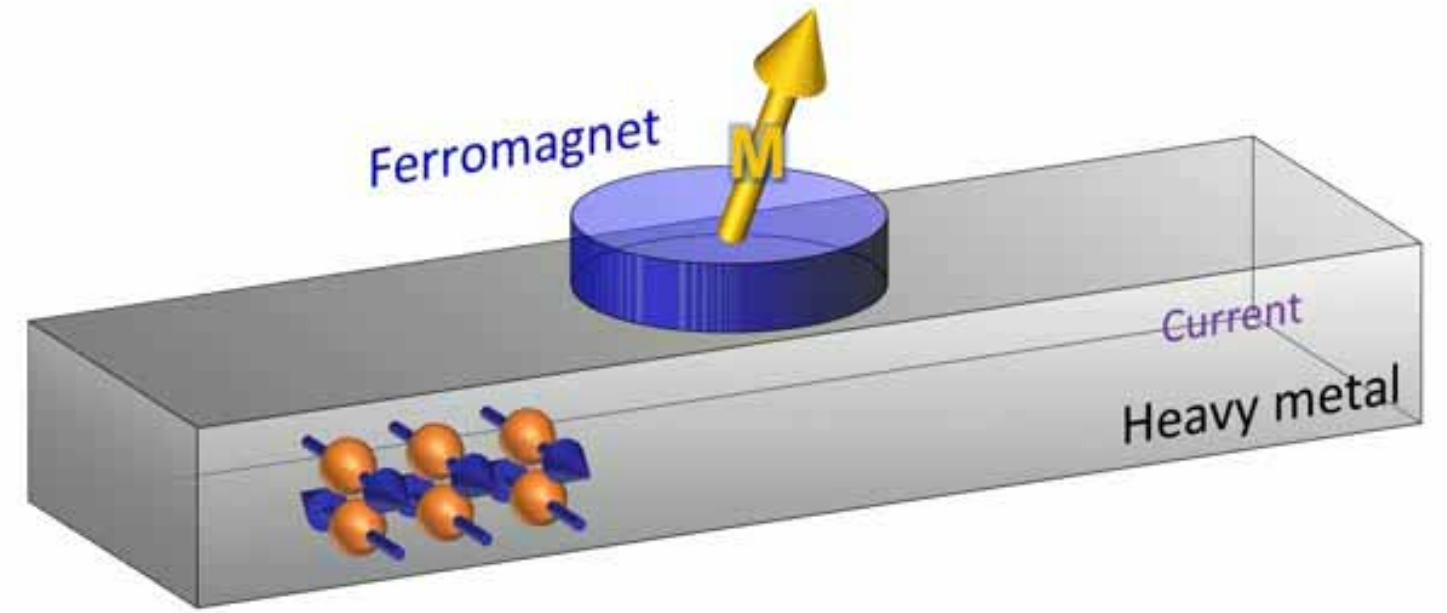


Area, Activity and Standby → Low Power

3 terminal device

Spin-Orbit Switching for SOT-MRAM

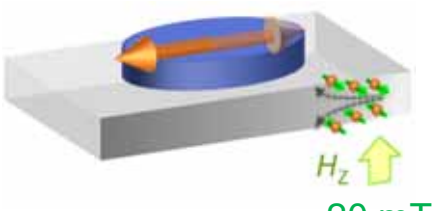
Spin-Orbit Torque (SOT) switching



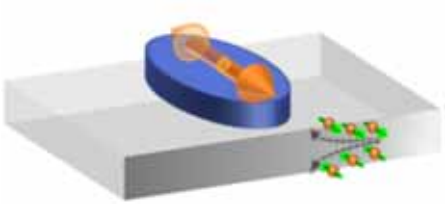
1. In-plane current → Spin accumulation (through SOI)
2. Accumulated spin → Torque (=Spin Orbit Torque; SOT)
3. Torque → Magnetization switching

Experiment

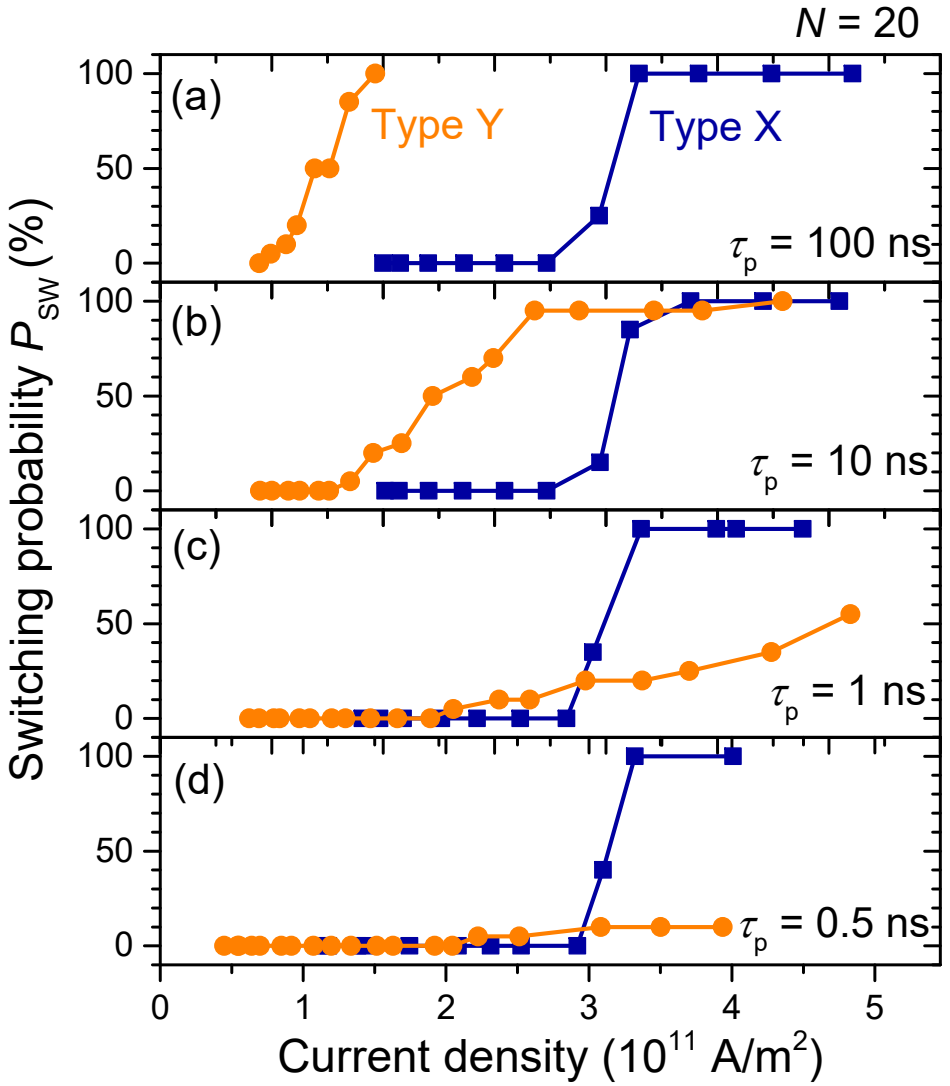
- Type X



- Type Y
  (≈STT switching)



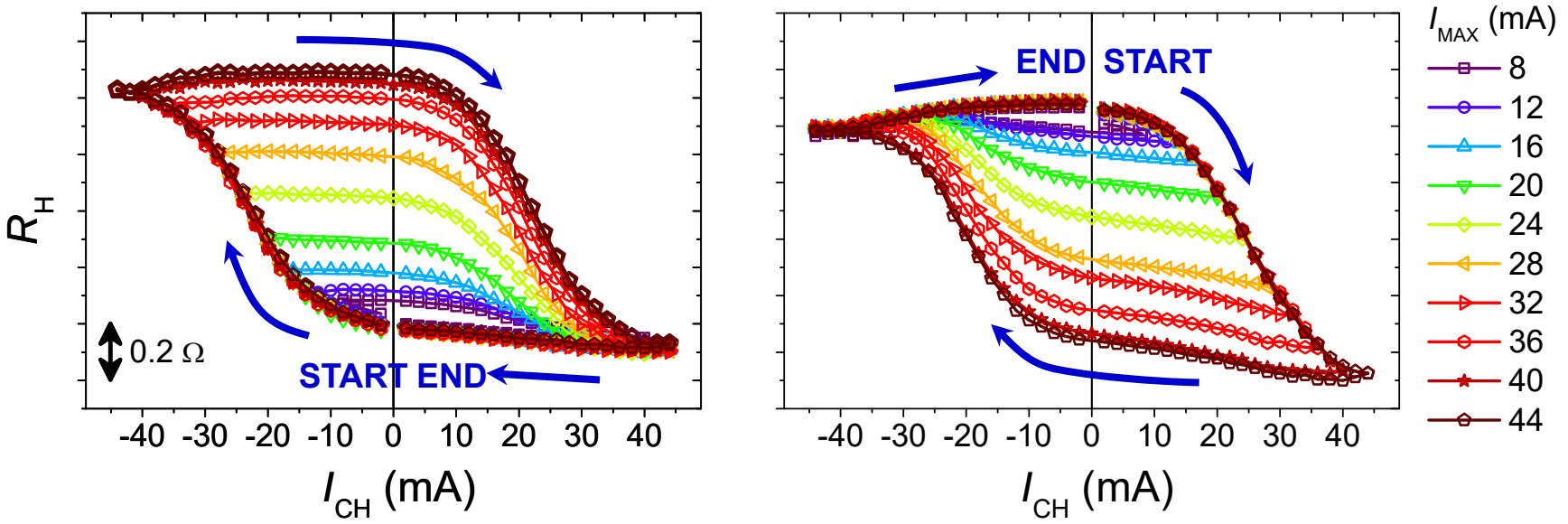
SOT switching in Type X (and Type Z) is promising for GHz-class operation.



S. Fukami *et al.*, Symp. on VLSI Tech. T06-5 (2016).

(Co/Ni)/(Pt/Mn) SOT Device

t_{PtMn} = 8 nm (biased)
H = 0



- Change in R_H varies gradually with I_{MAX}.
  = Magnetization state can be controlled in an analogue manner by the I_{CH}.

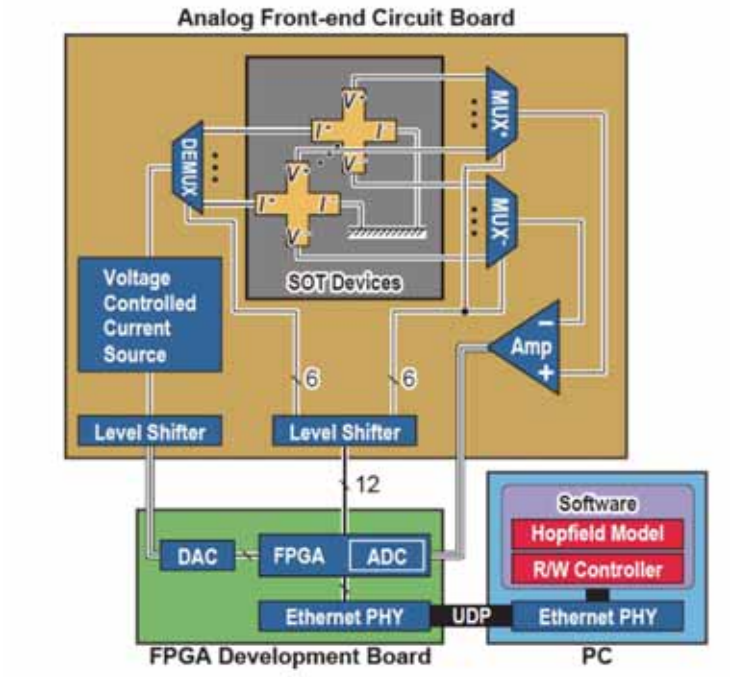
… Function of synapse ➔ Neuromorphic computing (AI)

S. Fukami *et al.*, Nature Mater. **15**, 535 (2016).

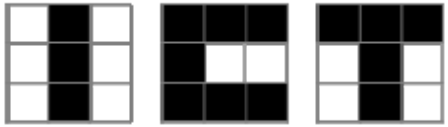
Applied Physics Express **10**, 013007 (2017)
https://doi.org/**10.7567/APEX.10.013007**

Analogue spin–orbit torque device for artificial-neural-network-based associative memory operation

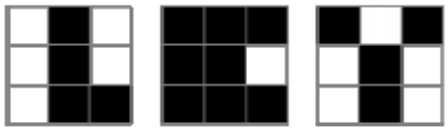
William A. Borders[1], Hisanao Akima[1*], Shunsuke Fukami[1,2,3,4*], Satoshi Moriya[1], Shouta Kurihara[1], Yoshihiko Horio[1], Shigeo Sato[1], and Hideo Ohno[1,2,3,4,5]



Memorized patterns



Input patterns (example)



Result for 100 trials

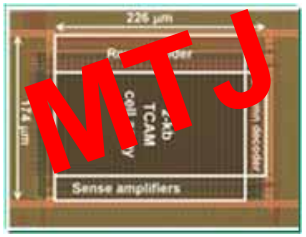
Synaptic weight	Mean direction cosine
Ideal	0.905
Before learning	0.601
After learning	0.852

- Recovery of direction cosine confirmed.
- Difference from ideal value is due to variation of dynamic range

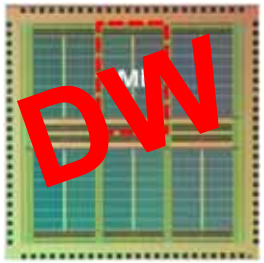
Non-volatile CMOS VLSIs with spintronics

TOHOKU

600MHz
MTJ/CMOS Latch
(**Fastest** nonvolatile latch)
(IEDM 2011)

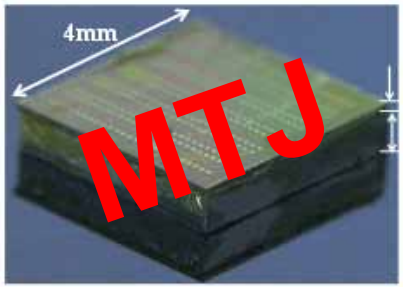


Nonvolatile TCAM
(**Most compact** TCAM
cell, 4T-2MTJ)
(VLSI 2011)



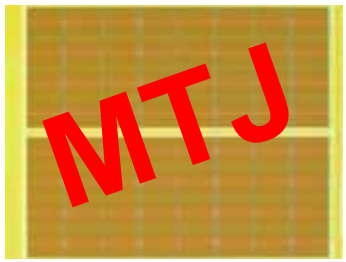
1Mb Array Three
Terminal **DW** Cell
(**High endurance**)
(VLSI 2012)

First Auto **Design**
Tool for
Spintronics CMOS
(2011)



Nonvolatile FPGA
with TSV
(**First 3D** Spintronics
CMOS Processor)
(VLSI 2012)

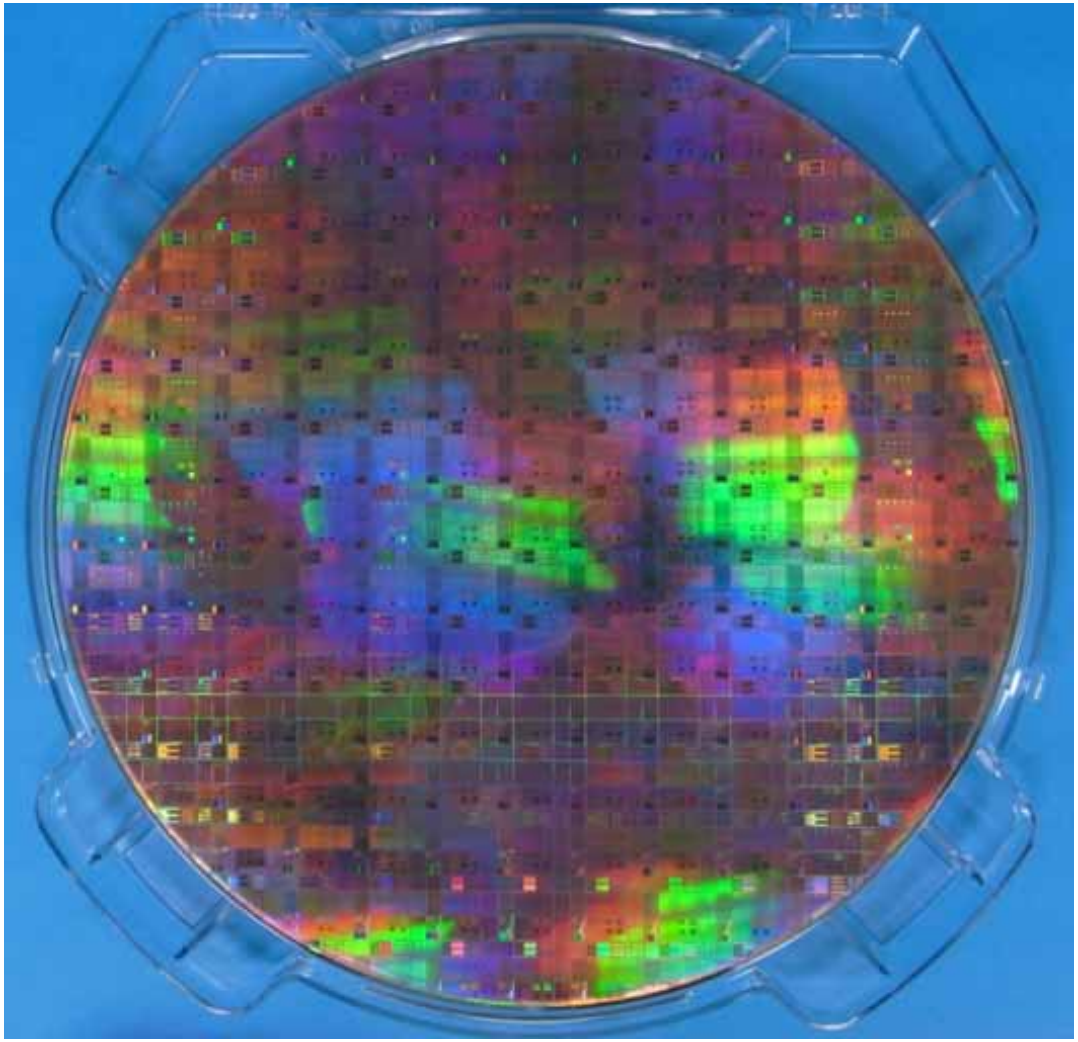
Nonvolatile GPU
(**Largest Scale**
Spintronics Random
Logic 500kgate/chip)
(ISSCC 2013)



1.5nsec / 1Mbit
Embedded MRAM
(**Fastest** nonvolatile
1Mbit memory)
(VLSI 2013)

Nonvolatile
microcomputer
(**First** nonvolatile
microcomputer)
(ISSCC 2014)

On 300 mm wafers



Development framework for spintronics devices

Tohoku University

Center for Spintronics Integrated Systems (CSIS)
(**Director : Hideo Ohno**)

Development of key technologies for spintronics materials and devices using 3in process tools

+

Center for Innovative Integrated Electronic Systems (CIES)
(**Director : Tetsuo Endoh**)

Development of spintronics materials, devices and integration technologies using 300 mm-wafer process tools

Paradigm Shift by Spintronics