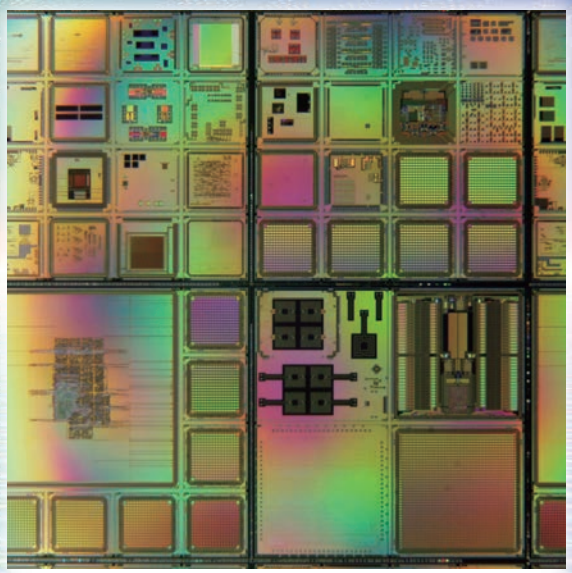
VDEC

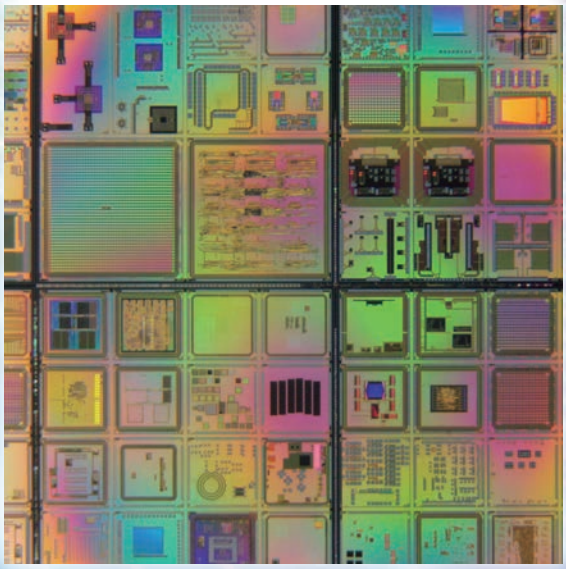
平成26年度

東京大学
大規模集積システム設計教育研究センター

年 報

2014
VLSI Design and Education Center, The University of Tokyo Annual Report





VLSI Design and Education Center
The University of Tokyo

This is the 2013 Annual Report of VDEC（VLSI Design and Education Center, University of Tokyo）.

In 2013 VDEC has decided a new policy of activities; “international collaborations and cross-bridges to industry”. As a result of Japanese semiconductor industry, which has given up in-house development of advanced technologies beyond 40 nm and steered to “fabless” or “fablite” business models, it is getting hard for VDEC to find partners for advanced chip fabrication. So, we decided to make an agreement with CMP in France in order access to 28nm FDSOI/CMOS technology of ST Microelectronics as an advanced fabrication technology for the time being. Since it is a new and complicated technology, we carried out a test run under a support from STARC. Experienced design teams about 10 laboratories in Japanese universities has contributed to the test run to check design rules and design environments for establishing VDEC design flow. Measurement results of the test chips will be available soon. VDEC has a plan to start a new chip fabrication service of 28 nm FDSOI/CMOS twice a year, based on the measurement results.

VDEC and ICREC in Vietnam National University signed an MOU last November for collaborations in education and research. ICDREC is enthusiastic about developing commercial products. It will be a good partner for VDEC to establish cross-bridges to industry. ICDREC has a plan to send engineers to VDEC this year for training of clean room technologies. We would also like to start collaborations with other countries in Asia and Middle East.

In order to lead to a breakthrough in current situation of the semiconductor industry in Japan, we need to bridge gaps between researches in universities and venture businesses, making transition smooth in terms of design and fabrication environments. We have started discussions with CAD vendors and semiconductor foundries. But, because it is impossible without a new budget plan, we would like to proceed step by step. When we make a progress, we will report in the VDEC seasonal letters.

Today, the number of registered members of VDEC design services and the number of VDEC clean room users (mainly MEMS researchers) are almost identical. Since the former is the number of teachers and the latter is the number of researchers and students, it is not simple to compare them. But, it is remarkable that the clean room users are increasing recent years. It is indispensable to maintain and renew facilities for keeping clean room processes in good conditions. Fortunately last year, we could newly introduce or replace VDEC facilities, such as EB pattern generator, FIB machine, etching equipment and high speed measurement apparatuses, by the supplementary budget of the Government. Especially booking of the old EB pattern generator has been full, but this year it will be relaxed due to higher throughput of the new machine.

As an annual event of the D2T (Design-to-Test) research division, which was donated by Advantest Corporation, the 8th symposium was successfully held on October 24th 2013, inviting distinguished lecturers on future LSI system and test technologies from oversea and domestic counties. We are scheduling the 9th symposium in August 26th this year, too. We would like to express our sincere thanks to Advantest Corporation for the continuous support.

We will continue to make our best effort for the original mission of VDEC, “promotion of education and research in LSI design field by means of practical chip-design and implementations”, with foreseeing the future of semiconductor society. We thank you for your continuous supports again.

June 2014

VLSI Design and Education Center, University of Tokyo

Director Kunihiro Asada

VLSI Design and Education Center, The University of Tokyo
Annual Report 2013

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Chapter 1 Activity Report of VDEC

1.1 Introduction of VDEC activities and activity report of FY2013

VLSI Design and Education Center (VDEC), University of Tokyo was established in May 1996. VDEC has been operating for the following 3 major roles:"spreading the latest information on VLSI design and education," "providing licenses of CAD tools," and"supporting on VLSI chip fabrications for academic use." The VDEC activity report of FY 2013 is described hereafter according to Fig. 1. 1.

The missions of VDEC are for advancement of researches and education on LSI design in public and private universities and colleges in Japan and send many distinguished VLSI designers into industry. After 17 years of VDEC establishment, educations on CAD software, LSI design and design flow in universities have been well established. On the other hand, advancement on nano-meter CMOS technologies forces design flow and CAD software complicated. We have been continuing CAD tool seminar by the lecturers from EDA vendors for twice a year. We hold the seminar in VDEC and provide distance learning through video streaming. We expect spread of the up-to-date LSI design methodology by using CAD tools.

We assume our LSI design flow seminars as educations on basic LSI design concepts and practical experience of LSI design with CAD tool chain. VDEC holds"LSI design education seminar", aka VDEC Refresh Seminar, once a year from November to January time frame for this purpose. As for the VDEC Refresh Seminar, this year we continued"Analog design course" and"RF design course", and initiated"MEMS design course". We invite experienced professors among universities as lecturers for the courses to conduct LSI design education courses with practical experience. We also hold"Transistor level design flow in VDEC" and"Digital design flow in VDEC EDA environment" for designers in universities.

In addition to the above seminars, we hold"VDEC

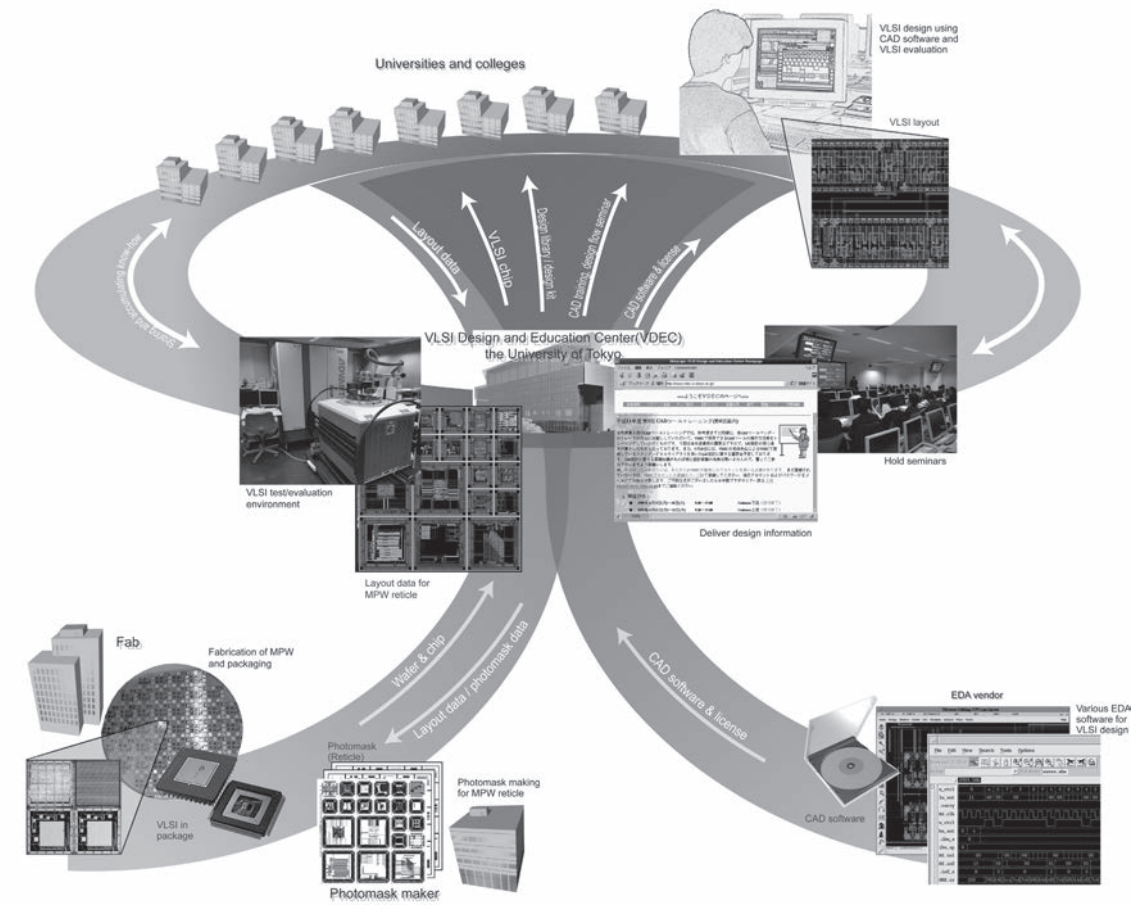


Fig. 1. 1 VDEC activities

Designer'Forum" among young professors and students annually. This is a workshop that the participants exchange their design examples with not only success stories but also their failure stories, in addition to invited talks. We expect students and professors who will start designs to learn kinds of know-hows. We have initiated "IEEE SSCS Japan Chapter VDEC Design Award" this year, and final examination and awarding have carried out during the"VDEC Designer'Forum". Mr. K. Imai (Shizuoka Univ.) is awarded as"IEEE SSCS Japan Chapter VDEC Design Award" winner, and Dr. G. He (Kobe Univ.), Dr. S. Yoshimoto (Kobe Univ.), Dr. H. Konoura (Osaka Univ.), and Mr. K. Takagi (Kobe Univ.) are awarded as"the best VDEC Design Award", and Mr. R. Wu (TITECH), H. Takehara (NAIST), Mr. Y. Umeki (Kobe Univ.), Mr. R. Hori (Ritsumeikan Univ.), and Dr. N. Kamae (Kyoto Univ.) are awarded as the"VDEC Design Award."

LSI designers come up against various difficulties during actual LSI design scene, even after the basic educations through various seminars and the forum. One of the biggest problems for beginners is the setup of CAD softwares. Many of them also get confused by"Esoteric messages" come out from CAD softwares, even after they successfully setup CAD tools. In such situations, VDEC mailing-lists make significant contributions. VDEC users can register to VDEC mailing-lists on CAD tools, and process dependent groups through VDEC web pages, and can ask questions and helps on their facing issues. It is not a responsibility for the registrant of such mailing-lists to give answers to questions, however, in most cases, replies are given by the experienced users of CAD tools and experienced designers within a couple of hours to a couple of days. Moreover, emails are accumulated and are open to the VDEC users, as shown in Fig. 1. 2, who have registered VDEC accounts, as the important educational assets. We expect all the VDEC users to make the full use of this mechanism to help solve problems.

With August 2013 shuttle, we shut-down eShuttle 65 nm CMOS chip fabrication service. After METI-STARC project terminated in FY2012, STARC supported to have chip fabrication test run for STMicro 28 nm FDSOI CMOS chip fabrication. We continue chip fabrication services on 0.18 μm CMOS by Rohm and 0.8 μm CMOS by On-semi Sanyo Semiconductor.

Our donated division"Design To Test (D2T)", which was founded by donation from Advantest in Oct. 2008, focuses on enrichment of education on LSI testing and bridging between design and testing.

Fig. 1. 3 shows trends of number of papers through VDEC activities. Number of papers is increasing, which means researches in the field of VLSI design have been encouraged after VDEC establishment.

Fig. 1. 4 shows number of papers related to CAD usage, chip fabrications and VDEC facility usages. CAD tools are widely used to write papers. CAD tools are used not only chip designs themselves but also used for preparation of chip fabrication and they contribute to verify fundamental ideas of researches. Advanced CMOS processes are preferred for publications, and not only papers with 65 nm CMOS chips, but also with 45 nm CMOS, 32 nm CMOS and 22 nm CMOS are emerging in the world. We would like to prepare chip fabrication services for the advanced CMOS processes. In addition, we would like to setup chip

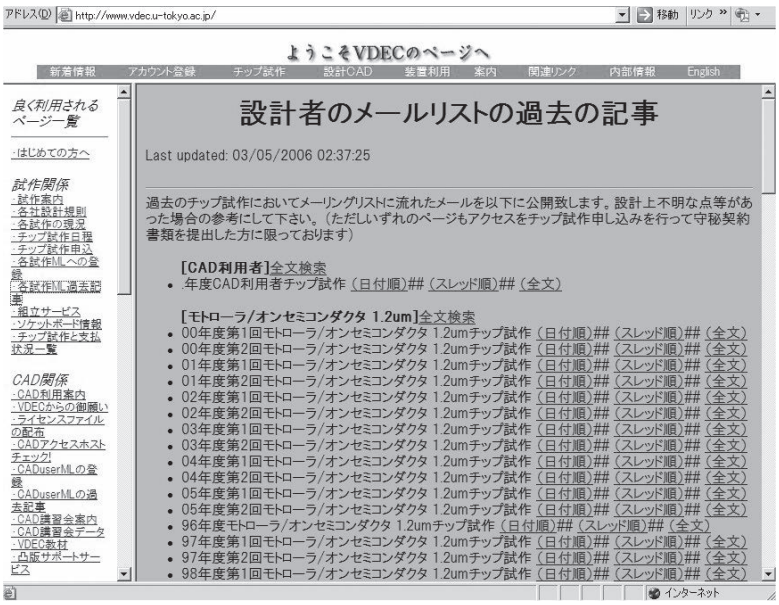


Fig. 1. 2 Archives of emails of VDEC mailing-list.

fabrication services related to CMOS/MEMS to fulfill the researches for “More than Moore”. We also encourage researchers to fully use of VDEC facilities such like LSI testers, FIB systems and EB writer for the wide spread of research purposes.

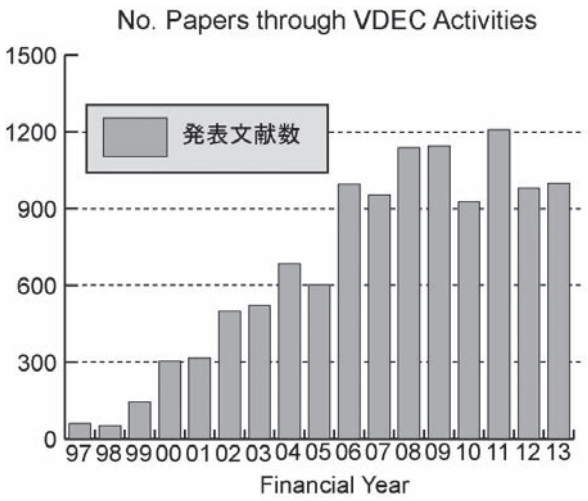


Fig. 1. 3 Trends of number of papers through VDEC activities.

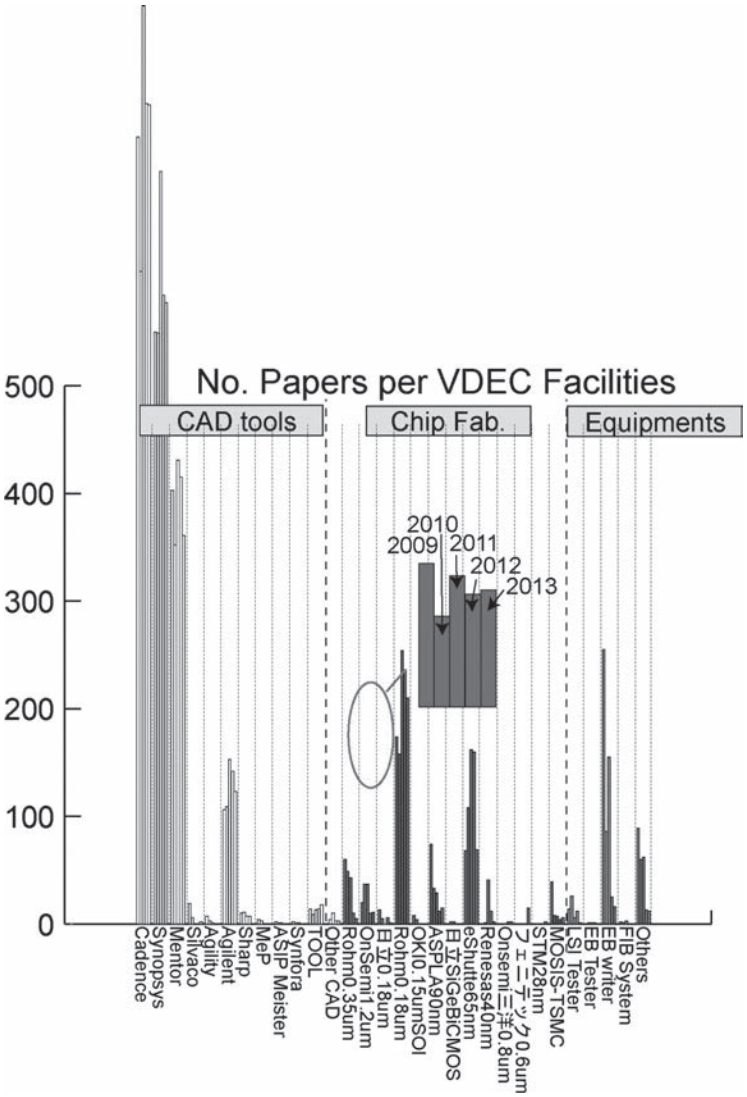


Fig. 1. 4 Number of papers related to VDEC facilities.

1. 2 VDEC CAD Tools

Since 1996, VDEC has provided CAD software licenses to the registered researchers in universities and colleges in Japan. The CAD tools we provided in 2009 are shown in Table 1. 2. 1. The researchers can use those CAD tools when their local machines, whose IP addresses are registered in advance, are authorized by one of VDEC license server located in the ten VDEC subcenters shown in Figure 1. 2. 1. For each CAD tool, VDEC provides 10–100 floating licenses. Those CAD tools can be utilized only for research and education activities in national universities, other public universities, private universities, and colleges.

When one is going to use VDEC CAD tools and chip fabrication service (the details are described in Section 1-3), some faculty member of his/her research group in a university or a collage needs to do user registration. Figure 1. 2. 2 shows (a) the number of registrants, (b) the number of distinguished universities/colleges of the registrants, and (c) the number of registrants who applied VDEC CAD tools.

Table 1. 2. 1 VDEC CAD tools

Name	Function	Vendor
Cadence tool set	Verilog-HDL/VHDL entry, Simlation, Logic synthesis, Test pattern generation, Cell-based (including macros) place, route, and back-annotation, Interactive schematic and layout editor, Analog circuit simulation, Logic verification, Circuit extraction	Cadence Design Systems, Inc.
Synopsys tool set	Verilog-HDL/VHDK simulation, Logic synthesis, Test pattern generation, Cell-based (including macros) place, route, and back-annotation, Circuit simulation, Device simulation	Synopsys, Inc.
Mentor tool set	Layout verification, Design rule check	Mentor Graphics Co. Ltd.
Silvaco tool set	Fast circuit simulation	Silvaco
ADS/Golden Gate	Design and verification of high-frequency circuits	Agilent Technologies
Bach system	BachC-based design, synthesis, and verification	Sharp
LAVIS	Layout visualization platform	TOOL

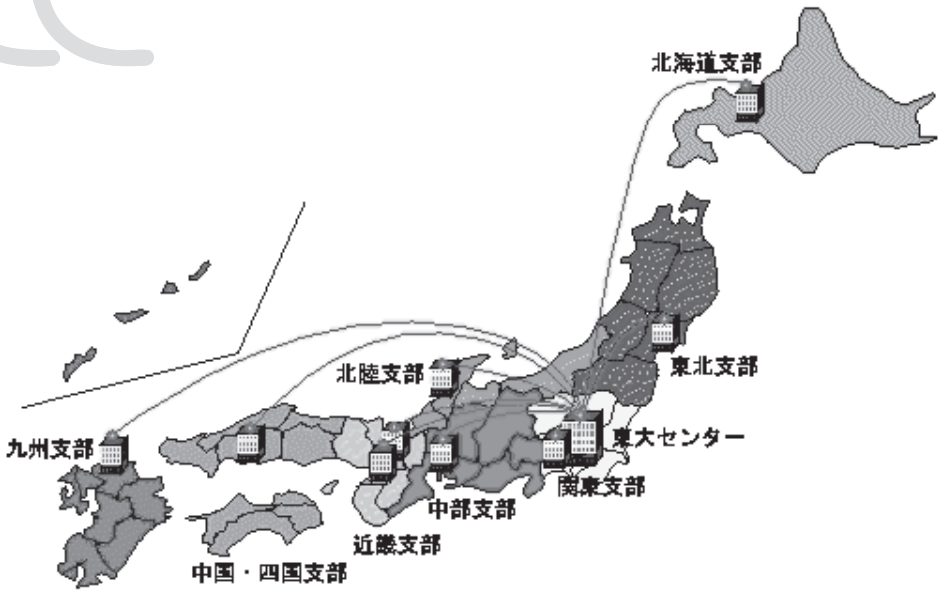
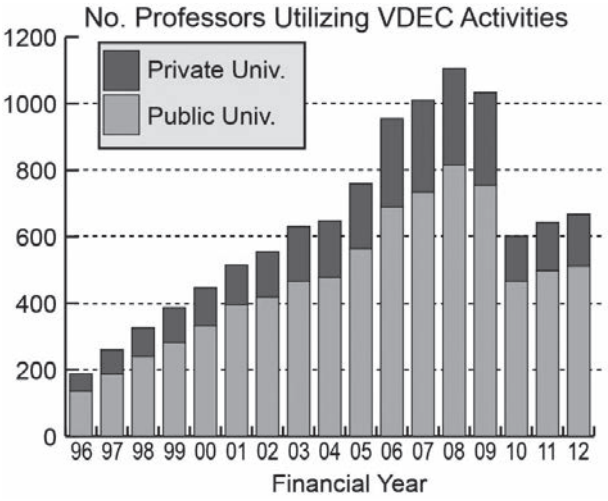
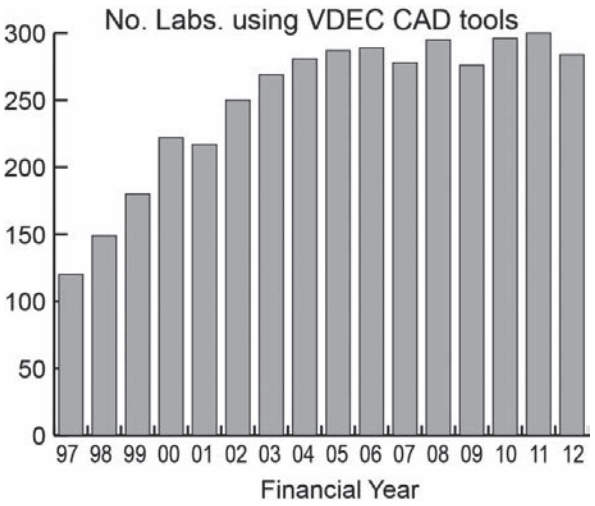


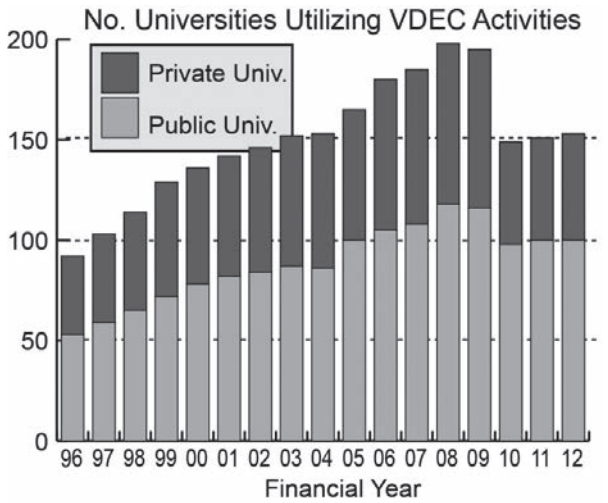
Fig. 1. 2. 1 VDEC Subcenters



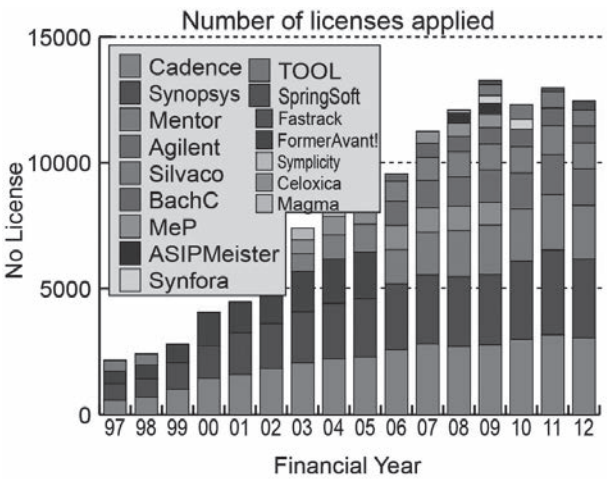
(a) The number of registrants



(c) The number of research group applied CAD tools



(b) The number of universities colleges of the registrants



(d) The number of applied licenses of all CAD tools

Fig. 1. 2. 2 The numbers of VDEC CAD Applications

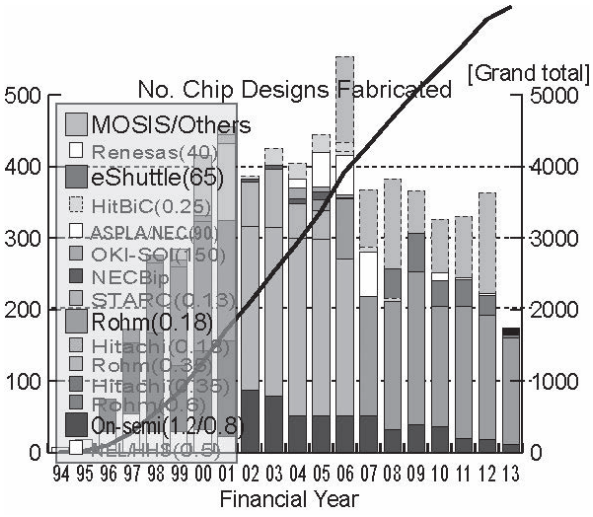
1. 3 VLSI Chip Fabrication

1. 3. 1 Trends of VLSI Chip Fabrication Services

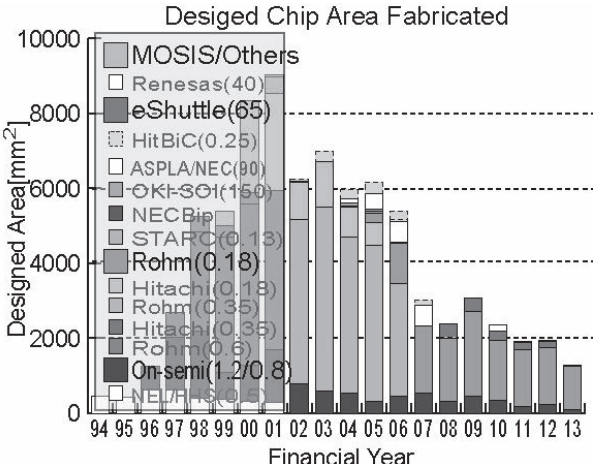
Fig. 1. 3. 1 shows a trend of number of designed chips for VDEC chip fabrication services, including pilot project prior to VDEC establishment.

VLSI chip fabrication is limited to 0.5 μm CMOS provided by NTT Electronics during the pilot project in 1994 and 1995. VDEC chip fabrication had started in 1996 with 1.2 μm CMOS provided by Motorola Japan, which is now On-Semiconductor as well as the 0.5 μm CMOS. In 1997, VDEC received cooperation from Rohm and has started 0.6 μm CMOS process. In 1998, VDEC started chip fabrication services of 0.35 μm CMOS by Hitachi, and in 1999, VDEC started 0.35 μm CMOS by Rohm. We had a test chip fabrication of 0.13 μm CMOS by STARC through"IP development project" in 2001. We added 0.18 μm CMOS by Hitachi into our chip fabrication menu in 2001. From 2002, we started VDEC-MOSIS chip fabrication program initiated by Prof. Iwata of Hiroshima University. Under this program, VDEC member can access to TSMC and IBM processes with lower price. We also started Bipolar chip fabrication by NEC Compound Semiconductor Devices. In 2004, we started 0.15 μm SOI-CMOS chip fabrication by Oki Electric as test chip fabrications. In the same year we started 90 nm CMOS chip fabrication by ASPLA/STARC. In 2006, we started 0.18 μm CMOS by Rohm and 0.25 μm SiGeBiCMOS by Hitachi. In 2008, we started 65 nm CMOS process by eShuttle, after closure of 90 nm CMOS chip fabrication in 2007. In 2010, we started 40 nm CMOS process by Renesas Electronics through"Next Generation Semiconductor Circuits & Architecture" project between METI and STAR. On the other hand, 1.2 μm CMOS chip fabrication program came to end by the September 2011. 40 nm CMOS by Renesas Electronics and 65 nm by eShuttle also come to end by Oct. 2012 and Aug. 2013, respectively. We started CMOS0.8 μm in Oct. 2012 by On-semiconductor-Sanyo as a test chip fabrication and opened it as the regular chip fabrication menu in 2012. We started FD-SOI 28 nm CMOS by ST-Microelectronics through CMP, France, as the advanced CMOS process in 2013.

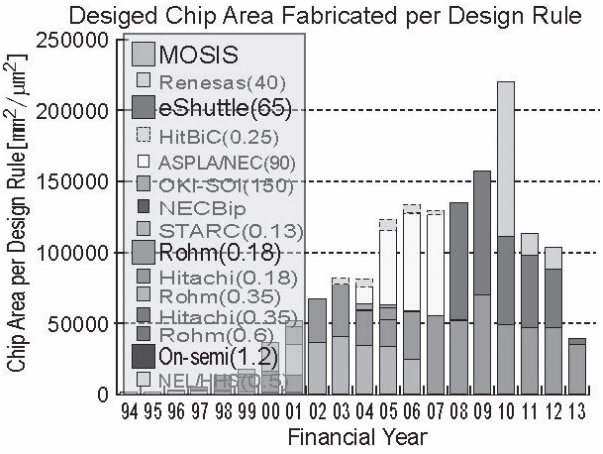
Fig. 1. 3. 1(a) shows trends of number of chip designed for VDEC chip fabrication. For the first 6 years until 2001, the number of designed chips shows steady increase, which means drastic improve of the effectiveness researches and education of LSI design, and we assume



(a) Trend of number of designs fabricated.



(b) Trend of designed area.



(c) Trend of designed area normalized by design rule.

Fig. 1. 3. 1 Trend of number of designs and designed chip area.

drastic increase of number of students related to LSI chip design and education. During few years of stable number around 400 chip designs per year, we can see transition of designs toward finer process. In 2007, we saw a large drop, which was caused by sudden process transition from 0.35 μm CMOS to 0.18 μm CMOS, and in 2008, we also saw another drop by process transition from 90 nm CMOS to 65 nm CMOS.

Fig. 1. 3. 1(b) shows trends of designed chip area, which shows much clear trends of drop by process migration. On the other hand, Fig. 1. 3. 1(c) shows trends of designed chip area normalized by design rule, which assume to be strong relation with design efforts. Coming from the fact that the normalized chip area is still growing, we assume the major reason for decrease of number of chips and designed area is increase of design effort per chip and per unit area due to process scaling.

Fig. 1. 3. 2 shows trends number of professors and universities fabricated chip. Number of professors who have contracted NDA for process technologies to access design rules and design libraries are, 253, and 28, respectively, for 0.18 μm CMOS, and 0.8 um CMOS.

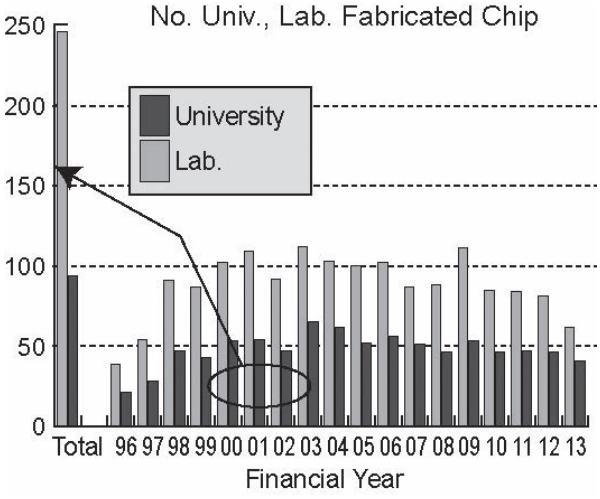


Fig. 1. 3. 2 Trend of number of processors and universities fabricated chip.

1. 3. 2 Overview of chip fabrication in 2013

Table 1. 3. 1 lists chip fabrication schedule in 2013. Please refer to list in Chapter 2 for details of designers and contents of chip designed.

Table 1. 3. 1 Chip fabrication schedule in 2013

○ **0.8 μm CMOS (On-Semiconductor - Sanyo)**

	Chip application deadline	Design deadline	Chip delivery
2013 #1	2013/ 6/ 3	2013/ 8/26	2013/12/10
2013 #2	2012/ 1/10	2014/ 3/24	2014/ 7(Schedule)

○ **0.18 μm CMOS (Rohm)**

	Chip application deadline	Design deadline	Chip delivery
2012 #5	2013/ 1/ 8	2013/ 3/12	2013/ 5/16
2013 #1	2013/ 3/25	2013/ 6/17	2013/10/16
2013 #2	2013/ 5/ 1	2013/ 7/24	2013/10/16
2013 #3	2013/ 6/19	2013/ 9/11	2013/12/26
2013 #4	2013/ 7/29	2013/10/21	2014/ 2/14
2013 #5	2013/11/ 4	2014/ 1/27	2014/ 5/14

○ **65 nm CMOS (eShuttle/STARC)**

	Chip application deadline	Design deadline	Chip delivery
2013 April	2013/ 6/12	2013/ 7/24	2013/11/12

○ **28 nm CMOS (STMicro/CMP)**

	Chip application deadline	Design deadline	Chip delivery
2013 Nov.		2013/11/24	

This chip fabrication is carried out as METI/STARC project.

1. 3. 3 Libraries and design flows

VDEC have been working to prepare design libraries and design flows for digital design and PDKs for analog design. Table 1. 3. 2 lists libraries available now.

Table 1. 3. 2 Libraries available for VDEC chip fabrication

Technology	Name	Author	Contents
0.18 μm CMOS (Rohm)	Rohm library	Rohm Library Std. Cells, IO cells, RAM (Distributed with CDROM)	Synthesis(Synopsys)
			Simulation(VerilogXL)
			P&R(LEF/DEF)
	Kyodai Library	Onodera Lab., Kyoto University	Synthesis(Synopsys)
			Simulation(VerilogXL)
			P&R(Astro)
	Todai Library	VDEC Design flow based on library prepared by Onodera Lab., Kyoto University	Synthesis(RTL Compiler)
			Simulation(VerilogXL)
			P&R(Encounter)
	PDK	VDEC	PDK(IC6.1)

1.4 Seminar

Seminar is indispensable for the improvement of LSI design technology. Some seminar and forums, such as technical seminar for CAD use, refreshing seminar for working people, designer's forums for young professors and students were held in 2011.

【Technological seminar for CAD use】

In a technological seminar for CAD use, VDEC invites lecturer from each tool vender, such as Cadence, Synopsys and Agilent, to hold the CAD operation course. Moreover, the course concerning the design flow in the VDEC environment was held by the VDEC staff. A technological seminar for CAD use for the beginner was held in The University of Tokyo VDEC in August and September at the year 2013. This seminar took 5 days for 2 kinds of Cadence tools, 5 days for 3 kinds of Synopsys tools, 1 days for 1 kind of Agilent tool. In addition, VDEC teachers gave lecturers on transistor level circuit design course, and digital circuit design course under the VDEC EDA environment. Teachers and students up to 40 people attended a lecture in each course, and master the use of each tool for VLSI design flow that uses the VDEC library. Moreover, another technical seminar for CAD use for matured teachers and students was held in March by Cadence 2 kind and 3 days, Synopsys 1 kind and 1 days, Agilent 1 kind and 1 days (Table 1. 4. 1). The demand for these CAD technological seminars is very large, and VDEC has maintained the mechanism of a large-scale CAD technological seminar holding corresponding to this situation. So far, the seminar was held at the University of Tokyo OR other VDEC branch, however, we started to distribute the lecture using Web streaming, so that students around VDEC branch can take the seminar at the branch school.

Table 1. 4. 1 CAD technological seminar in summer of the year 2013

2013/08/05-06	Synopsys DesignCompiler+Power Compiler Seminar	Univ. of Tokyo	19
2013/08/05-06	Synopsys DesignCompiler+Power Compiler Seminar	Tohoku Univ.	2
2013/08/05-06	Synopsys DesignCompiler+Power Compiler Seminar	Nagoya Univ.	11
2013/08/05-06	Synopsys DesignCompiler+Power Compiler Seminar	Kyoto Univ.	2
2013/08/07-08	Synopsys Milkyway+IC Compiler Seminar	Univ. of Tokyo	25
2013/08/07-08	Synopsys Milkyway+IC Compiler Seminar	Tohoku Univ.	4
2013/08/07-08	Synopsys Milkyway+IC Compiler Seminar	Nagoya Univ.	2
2013/08/07-08	Synopsys Milkyway+IC Compiler Seminar	Kyoto Univ.	8
2013/08/07-08	Synopsys Milkyway+IC Compiler Seminar	Osaka Univ.	6
2013/08/07-08	Synopsys Milkyway+IC Compiler Seminar	Hiroshima Univ.	3
2013/08/09	Synopsys VCS-AMS(XA)+Mixed Signal sim Seminar	Univ. of Tokyo	10
2013/08/09	Synopsys VCS-AMS(XA)+Mixed Signal sim Seminar	Tohoku Univ.	3
2013/08/09	Synopsys VCS-AMS(XA)+Mixed Signal sim Seminar	Nagoya Univ.	1
2013/08/09	Synopsys VCS-AMS(XA)+Mixed Signal sim Seminar	Kyoto Univ.	7
2013/08/09	Synopsys VCS-AMS(XA)+Mixed Signal sim Seminar	Osaka Univ.	7
2013/08/09	Synopsys VCS-AMS(XA)+Mixed Signal sim Seminar	Hiroshima Univ.	2
2013/08/26-27	Cadence ADE Simulation Seminar	Univ. of Tokyo	26
2013/08/26-27	Cadence ADE Simulation Seminar	Tohoku Univ.	6
2013/08/26-27	Cadence ADE Simulation Seminar	Nagoya Univ.	1
2013/08/26-27	Cadence ADE Simulation Seminar	Kyoto Univ.	2
2013/08/26-27	Cadence ADE Simulation Seminar	Osaka Univ.	4
2013/08/26-27	Cadence ADE Simulation Seminar	Hiroshima Univ.	4

2013/08/26-27	Cadence ADE Simulation Seminar	Miyazaki Univ.	16
2013/08/28-30	Cadence IC 6 1 x Virtuoso Layout Seminar	Univ. of Tokyo	24
2013/08/28-30	Cadence IC 6 2 x Virtuoso Layout Seminar	Tohoku Univ.	10
2013/08/28-30	Cadence IC 6 4 x Virtuoso Layout Seminar	Nagoya Univ.	1
2013/08/28-30	Cadence IC 6 5 x Virtuoso Layout Seminar	Kyoto Univ.	3
2013/08/28-30	Cadence IC 6 6 x Virtuoso Layout Seminar	Osaka Univ.	6
2013/08/28-30	Cadence IC 6 6 x Virtuoso Layout Seminar	Hiroshima Univ.	3
2013/08/28-30	Cadence IC 6 7 x Virtuoso Layout Seminar	Miyazaki Univ.	14
2013/09/09-10	Digital Design Flow on VDEC Environment Seminar	Univ. of Tokyo	30
2013/09/11-12	Transistor Level Design Flow on VDEC Environment seminar	Univ. of Tokyo	26
2013/09/13	Agilent GoldenGate Seminar	Univ. of Tokyo	7
2013/09/13	Agilent GoldenGate Seminar	Tohoku Univ.	2
2013/09/13	Agilent GoldenGate Seminar	Kyoto Univ.	1

2014/03/03	Synopsys CustimSim-VCS Co-sim Seminar	Univ. of Tokyo	7
2014/03/03	Synopsys CustimSim-VCS Co-sim Seminar	Hokkaido Univ.	12
2014/03/03	Synopsys CustimSim-VCS Co-sim Seminar	Tohoku Univ.	1
2014/03/03	Synopsys CustimSim-VCS Co-sim Seminar	Kanazawa Univ.	1
2014/03/03	Synopsys CustimSim-VCS Co-sim Seminar	Osaka Univ.	2
2014/03/03	Synopsys CustimSim-VCS Co-sim Seminar	Hiroshima Univ.	2
2014/03/03	Synopsys CustimSim-VCS Co-sim Seminar	Nagasaki Univ.	2
2014/03/04	Cadence Encounter Test Seminar	Univ. of Tokyo	5
2014/03/04	Cadence Encounter Test Seminar	Hokkaido Univ.	10
2014/03/04	Cadence Encounter Test Seminar	Tohoku Univ.	1
2014/03/04	Cadence Encounter Test Seminar	Kanazawa Univ.	2
2014/03/04	Cadence Encounter Test Seminar	Osaka Univ.	1
2014/03/04	Cadence Encounter Test Seminar	Hiroshima Univ.	3
2014/03/04	Cadence Encounter Test Seminar	Nagasaki Univ.	3
2014/03/26-27	Cadence IC615 Virtuoso Seminar	Univ. of Tokyo	12
2014/03/26-27	Cadence IC615 Virtuoso Seminar	Hokkaido Univ.	10
2014/03/26-27	Cadence IC615 Virtuoso Seminar	Tohoku Univ.	5
2014/03/26-27	Cadence IC615 Virtuoso Seminar	Kanazawa Univ.	11
2014/03/26-27	Cadence IC615 Virtuoso Seminar	Osaka Univ.	7
2014/03/26-27	Cadence IC615 Virtuoso Seminar	Hiroshima Univ.	3
2014/03/26-27	Cadence IC615 Virtuoso Seminar	Tsuruoka Kosen	1
2014/03/26-27	Cadence IC615 Virtuoso Seminar	Nagasaki Univ.	3
2014/03/25	Agilent Momentumn Seminar	Univ. of Tokyo	6
2014/03/25	Agilent Momentumn Seminar	Hokkaido Univ.	8
2014/03/25	Agilent Momentumn Seminar	Tohoku Univ.	4
2014/03/25	Agilent Momentumn Seminar	Hiroshima Univ.	3

【Refresh Seminar for Working People】

Teachers of universities and designers in the first line of the enterprise were invited to the lecturer at "VLSI design refresh seminar" was held aiming at the latest, advanced knowledge and technical learning concerning VLSI design as a refreshing education for working people involved in the integrated circuit industry (Table 1. 4. 2). Though this seminar started chiefly in year 1998 under the support of Ministry of Education Technical Education Division to give practicing education of the latest VLSI design technology, it continues under many supports from many societies.

Course A: analog integrated circuit design (1/7–1/9), in addition, newly-started Course M1: MEMS design (1/21–1/22), and Course M2: MEMS fabrication (3/4–3/6) of three courses were held concerning VLSI design of recent year. 7 teachers from industry and universities involved in the integrated circuit research and the education were invited as the lecturer, and they introduced a state-of-the-art VLSI design technology including the practice using a lecture concerning VLSI design and the latest CAD tool. The participants were 13, 13 and 11 people for course A, M1 and M2, respectively.

Fig. 1. 4. 1 Refresh Seminar at VDEC seminar room at the University of Tokyo, VDEC.

Table 1. 4 .2 Refresh Seminar

Course A: Analog Circuit Design (3 days)
Analog Circuit Design and simulation Integrated Circuits Verification (LVS, DRC)
Masahiro Sugimoto (Chuo Univ.), Hidetoshi Onodera (Kyoto Univ.), Koji Kotani (Tohoku Univ.)

Course M1: MEMS Design (2 days)
MEMS Basic 1: Fabrication Process MEMS Basic 2: Operation Principle Structual Design Layout Design
Yoshio Mita (Univ. of Tokyo)

Course M2: MEMS Fabrication (3 days)
CAD Design and Analysis Lithography, Etching, Release Vibration measurement and analysis
Yoshio Mita (Univ. of Tokyo)

【Designer's forum for young eachers and students】

VDEC LSI designer forum intended for students and young teachers has been held. The VDEC LSI designer forum has aimed to sharing information that cannot be obtained at a society and a academic society, for example, the failure case and the solution in which LSI designer has a hard time, the inside story of CAD industry, the construction method in the design milieu in the laboratory, and so on. This year, we had the meeting in The University of Tokyo, Takeda hall from August/24 to 25. No less than 50 participants were flourishing at the gathering.

Table 1. 4. 3 Program of Designers Forum in 2011.

8/24 (Sat) VDEC Designers' Forum

9:10-10:00	Reception
10:00-10:10	Opening Remark
10:10-10:50	VDEC Prenary（VDEC Prof. Takeshi Shimizu）
	(rest)
11:00-17:30	VDEC Design Award Presentaion
17:30-19:00	VDEC Design Award Reception
19:00	Ph.D. session & Poster session

8/25 (Sun) VDEC Seminar

10:00-13:00	Linux Intro and CAD install/setup

1.5 Facilities

The VDEC has provided the big facilities for universities in Japan from the beginning of the VDEC foundation (1996). Big facilities refer to those which are impossible to acquire and or maintain by an individual research unit. Table 1. 5. 1 shows the available facilities of VLSI testers and some process machines, which are placed at the tester room and the super clean room of the Takeda building. In 2004, the VLSI tester (T2000) and the EB lithography machine (F5112+VD01) were donated to the VDEC by the ADVANTEST. In the year 2012, VDEC joined MEXT (Ministry of Education)'s Nanotechnology platform to enforce its multi-use capability. (For Nanotechnology Platform refer section 1.8). In the year 2013, VDEC acquired government's supplemental budget and installed several big apparatuses. The apparatuses include rapid EB lithography machine (ADVANTEST F7000S-VD02), backside access FIB machine (FEI V400 ACE), batch etching machines (ULVAC CE-S and SPTS DRIE MUC-21 ASE-Pegasus). From April 2013 to March 2014, the EB lithography machine F5112 has been used 1,602 times. The reason of the slight decrease from last year (1,882 times) is machine closure for new equipment installation. Average exposure count is increased to 160/month in FY2013 from that of FY2012 (157/month). The facilities for the LSI testing can be used after attending the technical seminar. The licenses are also required to use the EB lithography and the FIB.

Table 1. 5. 1 Available facility list

Facility	Equipment name	Description	Status	Contact
Logic LSI test System	EB tester: IDS10000	The chip surface voltage during operation can be measured with the LST tester. The digital circuit with 384 pins, 1GHz can be tested.	Available	equipment@vdec.u-tokyo.ac.jp
	LSI tester: HP8300	The digital circuit with 384 pins, 1GHz can be tested.	Available	HP83000@vdec.u-tokyo.ac.jp
	LSI tester: ADVANTEST T2000	The digital circuit with 256 pins, 512MHz can be tested. Analog test is optional.	Available	equipment@vdec.u-tokyo.ac.jp
	FIB: IDSP2X	Cutting wires of LSIs and depositing Pt wires are available to repair the LSI design errors.	Available	IDSP2X@vdec.u-tokyo.ac.jp
	Auto prober: PM-90-A	Automated prober for testing LSI wafers, which can be used with the LSI testers. The probe card for LSIs with the VDEC standard pin connections is available.	Available	equipment@vdec.u-tokyo.ac.jp
Analog/RF measurement system	Analog/RF measurement system: HP4156B, HP4284, etc	DC parameter measurement、Capacitance measurement, Network analyzer, Spectrum analyzer, etc.	Available	equipment@vdec.u-tokyo.ac.jp
	Low-noize manual prober: Cascade Microtec	6 inch wafer can be measured with six DC probles and two RF probes upto 50 GHz.		
	Low-noize, temperature controlled semi-auto prober: Süss Microtec	8inch wafer can be measured. The chip temperature range is -50 to 200℃.		
EB lithography system	Mask lithography, Direct lithography: F5112+VD01	Minimum linewidth: 50nm. Lithography for 5 inch photomask (thickness: 2.3 mm), 2-8 inch wafers, and chips is possible.	Available	equipment@vdec.u-tokyo.ac.jp
	Rapid Mask and Direct lithography: F7000S-VD02	Minimum linewidth: 1xnm. Lithography for 5 inch photomask (thickness: 2.3 mm), 2-8 inch wafers, and chips is possible. Stencil character projection of non-square shapes such as circle, triangle is possible.	In preparation	
	Chlorine ICP plasma etcher CE-S	High density plasma etching with Cl_2 and BCl_3 is possible.	In preparation	
	Silicon DRIE MUC-21 ASE-Pegasus	High speed, high aspect ratio etching of silicon is possible	In preparation	
FIB system	FIB: SII XVision200TB	Repairment of photomask, sample etching, etc. (Through Nanotech. Platform and LCNet)	Available	equipment@vdec.u-tokyo.ac.jp

1.6 Activity plan for 2014

VDEC will continue activities on chip fabrication services, CAD tool support, dispatching design related information and donated division"D2T", as has been previous years.

【Design related information dispatching/Seminar】

We will continue holding the following seminars: (1) CAD tools seminars which have been continued since 1997, (2)"Refresh seminar" since 1998, (3)"Designer' Forum" since 1997. We will also continue seminars for LSI tester usage at VDEC and sub-centers, workshops on LSI testing technologies initiated by D2T.

【CAD tool support】

We will continue Cadence tools, Synopsys tools and Mentor tools as the main stream design tools. We will continue analog RF design environment, GoldenGate and ADS by Agilent, C-based design environment, BachC by Sharp. In addition, we continue trial of several CAD tools, such as layout platform, Lavis by TOOL. Design debugging platform from SpringSoft has merged into Cadence tools and will be continued. SmartSpice by Silvaco, will be also continued.

【Chip fabrication services】

We will continue chip fabrication services for 0.18 μm CMOS by Rohm, and 0.8 μm CMOS by On-semiconductor-Sanyo as the regular services. We will start regular services of FD-SOI 28 nm CMOS by ST Microelectronics through CMP. We will ask packaging for the above chip fabrications to J-Device to meet the diverse needs of the assembly.

Table 1. 7. 1 Chip fabrication schedule

【CMOS 1.2μm 2P2M】 On-Semiconductor (Former Motorola Japan)

	Chip application deadline	Design deadline	Chip delivery
2014 #1	2014/ 7/14	2014/10/ 6	2014/12/29
2014 #2	2014/12/29	2015/ 3/23	2015/ 6/15

【CMOS 0.18μm 1P5M (+MiM)】 Rohm

	Chip application deadline	Design deadline	Chip delivery
2014 #1	2014/ 1/27	2014/ 4/21	2014/ 8/11
2014 #2	2014/ 4/14	2014/ 7/ 7	2014/10/27
2014 #3	2014/ 6/ 9	2014/ 9/ 1	2014/12/15
2014 #4	2014/ 8/25	2014/11/17	2015/ 3/16
2014 #5	2014/11/ 3	2015/ 1/26	2015/ 5/18

【FD-SOI CMOS 28 nm 1P10M】ST Microelectronics

Based on the chip fabrication schedule through CMP.

1. 7 Venture companies related to VDEC

Some professors related to VDEC started venture companies. The following is a list of the venture companies related to VDEC.

[1] AIL Co.,Ltd. (http://www.ailabo.co.jp/)

Related professor : Professor Kazuo Taki, Kobe Univ. (President-Director)

[2] Synthesis Corporation (http://www.synthesis.co.jp/)

Related professor : Professor Emeritus Isao Shirakawa, Osaka Univ. (Director)

Description of business : (1) Hardware/software co-design
(2) System LSI design, design services
(3) Development and sales of IPs
(4) Development of EDA tools

[3] ASIP Solutions, Inc. (http://www.asip-solutions.com/)

Related professor : Professor Masaharu Imai, Osaka Univ. (Representative Director and CTO)

Description of business : (1) EDA Tool
(2) Design Service and Consultation
(3) IP Development

[4] Nanodesign Corporation (http://www.nanodesign.co.jp/)

Related professor : Professor Kazuyuki Nakamura, Kyushu Institute of Technology. (Representa-tive Director)

[5] A-R-Tec Corp. (http://www.a-r-tec.jp/)

Related professor : Professor Emeritus Atsushi Iwata, Hiroshima Univ. (Representative Direc-tor)

Description of business : (1) Measurement and analysis of LSI substrate noise
(2) Design of analog-RF mixed signal LSIs
(3) Training of analog design on the JOB method

I. 8 “Nanotechnology Platform”: Ultra Small Lithography and Nanometric Observation Site

VDEC is operating an open-use nanotechnology platform “Ultra Small Lithography and Nanometric Observation Site” together with the Institute of Engineering Innovation of Graduate School of Engineering. The site is supported by Japanese Ministry of Education (MEXT)’s Nanotechnology Platform grant. Any researchers in Japanese Universities, Laboratories, and Companies can take full advantage of The University of Tokyo’s cutting-edge nanotechnology apparatuses and know-hows. The accessible technology includes Lithography and Etching environment, Ultra High-Voltage Acceleration (1MV) transmission electron microscope (TEM) that is capable of visualizing upto light materials such as Nitrogen. VDEC takes part in the lithography at Takeda Sentanchi Super Cleanroom. Through VDEC’s key apparatus F5112+VD01 donated from Advantest Corporation, VDEC is supporting post-VLSI activities such as MEMS. The machine is capable of rapidly writing patterns on arbitrary-shaped targets sizing from 1cm-sqare chip to 8-inch round wafers. The performance is measured by the number of research reports and machine use. The University of Tokyo site has received 150 research reports including 9 from big companies, 3 from SMEs, 32 from other universities, 33 from UTokyo and external collaborators, 67 from UTokyo researchers (excluding VDEC), and 6 from public research institutes. The exposure count was 1,602 for 10 months (160.2/month). “Open ratio” , which is the number of days in which users outside the University of Tokyo came, divided by machine open days, was 99%.

URL:http://nanotechnet.t.u-tokyo.ac.jp/

Chapter 2 Activity Report of "D2T Research Division"

2. 1 Introduction of "D2T Research Division"

2. 1. 1 Aim of "D2T Research Division"

ADVANTEST D2T research division was established in VDEC in October 2007. It continued for 3 years. As the name of the research division indicates, it is financially supported by ADVANTEST Corporation. Through the kindness of ADVANTEST Corporation, the research division was renewed and the second phase of D2T research division started from October 2010.

The aim of D2T research division is to promote the research and education environment of VLSI testing in all universities and colleges in Japan. "D2T" means that we consider not only design but also test. As the results of our activities, we hope to provide the experts of design and test for industry. In addition, we are exchanging researchers with other universities or research institute in both Japan and overseas. Moreover, D2T research division is in a good environment to make collaboration with industry because testing of VLSI is one of the most practical research topics in industry. Based on those activities, our final goal is to become a center of excellence of VLSI Testing in Japan.

The first phase and the second phase of D2T activities had finished in September 2010 and September 2013, respectively. The third phase started at October 2013 through the courtesy of Advantest Corporation. This year was the first year of the third phase, so we have actively conducted researches, educations, and symposium in the area of design and test. In this year, we invited two visiting professors, Prof. Krishnendu Chakrabarty from Duke University and Prof. Subash Shankar from (City University of New York). They had made the big impact as members of D2T group.

2. 1. 2 Members of "Advantest D2T Research Division"

Staff

Project Associate Professor	Satoshi Komatsu
Project Assistant Professor	Rimon Ikeno
Project Researcher	James Tandon
Project Researcher	Nguyen Ngoc Mai Khanh
Researcher	Takahiro Yamaguchi (Advantest Laboratories Ltd.)
Researcher	Masahiro Ishida (Advantest Corporation)
Assistant Clerk	Makiko Okazaki

2.2 Report of “D2T Symposium”

“The 8th VDEC D2T Symposium” took place on October 24th, 2013 at Takeda Building. In the symposium, five outstanding researchers were invited to give the state-of-the-art researches in the field of cyberphysical systems, 2.5D/3D tests, yield enhancement of LSIs, and mixed-signal DFT. In addition to the invited talks, the members of “Advantest D2T Research Division” reported their activities. In the panel session titled “Challenges and Solutions for Future LSI Systems and Testing”, a variety of topics was actively discussed among panelists and audiences.

More than 100 researchers from industry as well as professors / students attended the symposium. We believe the symposium was very interesting and exciting one for all attendees. VDEC will continue to have the symposium in future and we hope for your joining the events.

Symposium Program

10:00	**Opening Remark**
	Kunihiro Asada (Director of VLSI Design and Education Center, University of Tokyo) Toshio Maruyama (Chairman of the Board and Representative Director, Advantest Corporation)
10:10	**Session 1**
	"Technologies and Platforms for Cyberphysical Systems" *Giovanni De Micheli (Ecole Polytechnique Federale de Lausanne)* "Test and Design-for-Testability Solutions for 2.5D/3D Integrated Circuits" *Krishnendu Chakrabarty (University of Tokyo / Duke University)* "Activities of VDEC Advantest D2T Research Division" *Satoshi Komatsu (University of Tokyo)*
12:05	**Lunch**
13:20	**Session 2**
	"Universal Methodology for Yield Enhancement of ULSIC's Employing Product Test, IC Layout and Comprehensive Suite of Characterization Vehicles" *Andrzej Strojwas (Carnegie Mellon University / PDF Solutions, Inc.)* "Signal and Noise: A Radical Perspective on Mixed-Signal Test Research and Education" *Mani Soma (University of Washington)* "A Stochastic Sampling Time-to-Digital Converter" *Takahiro J. Yamaguchi (Advantest Laboratories)*
15:15	**Coffee Break**
15:40	**Session 3**
	"Synthesis from Oracles" *Subash Shankar (University of Tokyo / City University of New York)* "Layout Design for Practical Application of Electron-Beam Lithography with Character Projection Technique" *Rimon Ikeno (University of Tokyo)* "Introduction of Multi-Purpose EB Lithography system F7000S" *Masahiro Takizawa (Advantest)*
17:00	**Panel Discussion** "Challenges and Solutions for Future LSI Systems and Testing"
	Moderator: Krishnendu Chakrabarty (University of Tokyo / Duke University) Panelists: Andrzej Strojwas (Carnegie Mellon University / PDF Solutions, Inc.) Giovanni De Micheli (Ecole Polytechnique Federale de Lausanne) Mani Soma (University of Washington) Takahiro J. Yamaguchi (Advantest Laboratories)
18:20	**Closing Remark**
18:30	**Reception**

2. 3 Research Activity Reports of "Advantest D2T Research Division"

On-chip Digitizer/On-chip Spectrum Analyzer

Takahiro Yamaguchi, James Tandon, Nguyen Ngoc Mai Khanh, Satoshi Komatsu, Kunihiro Asada

We introduced a stochastic time-to-digital converter (TDC) with 180-770fs tunable resolution, less than 0.6LSB INL, and selectable dynamic range offset. Previous arbiter-based TDCs had fine resolution but small dynamic range which was difficult to calibrate. Our approach uses comparators as decision elements to precisely control dynamic range offset.

We designed a test chip of the rail-to-rail analog-to-digital converter (ADC) core for the offset control, which is based on the flash ADC architecture with 63 clocked comparators giving 6-bit resolution at the output. It is our first test chip using 28 nm FD (fully depleted) SOI/CMOS process, and we plan to evaluate the impact of process variations to clocked comparator stability as well as the basic ADC performance.

Method for Testing Power Integrity Fault

Toru Nakura, Masahiro Ishida, Satoshi Komatsu, Kunihiro Asada

While a required power supply voltage has become lower due to the advanced miniaturization of the semiconductor process, the power supply current consumed by an LSI chip has increased because of the huge number of transistors integrated on a single chip. It may increase the power supply noise, and power integrity issues of the device under test in both an ATE and a practical operating environments.

In this research project, we proposed a power integrity fault testing method for detecting the power integrity faults, e.g. excessive fluctuations of the power supply voltage and excessive variations of the power supply impedance, at the on-chip power supply nodes of the device under test. The proposed method evaluates the power integrity faults by observing an operation of the device under test while controlling its power integrity with synchronizing to the device operation by using on-chip noise sources. Furthermore, it can test a tolerance of the device under test against power integrity in the on-chip power delivery network by judging Pass or Fail of the device under test while injecting controlled power supply noises into on-chip power supply nodes. In order to validate the concept of our method, we have fabricated a TEG chip with Rohm 0.18-um CMOS process.

Structural Test Technique for Analog Circuits

Satoshi Komatsu

In this research, we propose an effective test method for system LSIs by introducing structural test approaches used in digital testing for analog circuit tests. Both digital circuits and analog circuits are often integrated into a system LSI, so the final target of the research is to test analog circuits by using digital circuits using structural test manner. This year, we have investigated and analyzed observability and controllability of such system LSIs and conducted some experiments about the observability and controllability.

High-throughput and high-accuracy electron-beam direct writing (EBDW) strategy for wide range of EBDW applications

Rimon Ikeno, Satoshi Komatsu, Yoshio Mita, and Kunihiro Asada

Electron-beam direct writing (EBDW) lithography is widely used in fabrication of not only semiconductor devices but also MEMS and photonic devices, because it offers low-cost and short turn-around time (TAT) device fabrication opportunity with its maskless feature. On the other hand, EBDW is known as a low-throughput lithographic technology, despite some evolutional techniques have already been introduced and utilized such like Variable Shaped Beam (VSB) and Character Projection (CP) methods. In general, high-throughput means less e-beam shots. Then, in some cases, the lithographic results have poor accuracy against the intended layout shapes, or they show roughness on their edges, if the data decomposition from the original layouts to e-beam shots is not appropriately processed.

In 2013, we started a collaborative research with Advantest Corp. on the total solution of the high-speed and high-accuracy CP EBDW technique for wide range of EBDW applications like MEMS, photonics, and so on.

This year, we discussed with EBDW users in Takeda Super Clean Room, and extracted their past findings and future expectations through their device fabrication using EBDW. We investigated software framework for new layout-data conversion flow, and started implementing geometric routines and CAD-tool interfaces. We also designed a CP mask for our experiments to investigate efficient character sets for wide range of EBDW applications.

2. 4 Publications

Journals

[1] Rimon Ikeno, Takashi Maruyama, Satoshi Komatsu, Tetsuya Iizuka, Makoto Ikeda, Kunihiro Asada, "High-throughput Electron Beam Direct Writing of VIA Layers by Character Projection with One-dimensional VIA Characters," IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, Vol.E96-A, No.12, pp.2458-2466, Dec. 2013.

International Conferences/ Symposiums/Workshops

[1] James S. Tandon, Takahiro J. Yamaguchi, Satoshi Komatsu, and Kunihiro Asada, "A Stochastic Sampling Time-to-Digital Converter with Tunable 180-770fs Resolution, INL less than 0.6LSB, and Selectable Dynamic Range Offset," IEEE Custom Integrated Circuits Conference (CICC), September 2013.

[2] Takahiro. J. Yamaguchi, James S. Tandon, Satoshi Komatsu, and Kunihiro Asada, "A Novel Test Structure for Measuring Variance of Threshold Voltage in MOSFETs," 2013 IEEE International Test Conference, September 2013.

[3] S. Komatsu, "On-chip Measurement / Monitor Circuits Based-on Stochastic Approach," 2013 International Test Conference (Elevator Talk), September 2013.

Chapter 3 Research in VDEC

Asada, Nakura and Iizuka Laboratory

(http://www.mos.t.u-tokyo.ac.jp)

Supply Fluctuation Monitoring and Reduction Method

Kunihiro Asada, Toru Nakura, and Yoshitaka Yamauchi

While the supply voltage is lowering due to the scaling rule, the power supply current in the LSI is increasing because of the progress of integration. As a result, the supply fluctuation becomes more serious for practical operations and to ensure the power integrity of the LSI needs more cost. For example, much chip area is paid for decoupling capacitors on the chip to reduce di/dt noise and resonant noise.

To mitigate the chip area penalty for on-chip decoupling capacitors, a supply fluctuation cancellation method named active charge sharing has been proposed. This method aimed to reduce the supply fluctuation mainly caused by DVS. This year, we proposed a new supply fluctuation monitoring circuit to apply the cancellation to the supply fluctuation not only caused by DVS scheduled in OS but also caused in hardware levels. The monitoring circuit consists of TDC and DLL and detects average supply fluctuation in clock cycles by utilizing the gate delay dependence on the supply voltage. The behavior of the proposed circuit was checked by circuit simulations. A circuit design for an experimental verification was completed.

Reliability Improvement of LSIs with the fine pitch process

Kunihiro Asada, Toru Nakura, Tetsuya Iizuka,
Kevin Nagri, Kazuhiro Mori

It is believed that the time-domain resolution of a digital signal edge transition is superior to the voltage resolution of an analog signal in advanced CMOS processes. The reasoning behind this is that operating voltage has been reducing, making the signal more vulnerable to noise power due to scaling. On the other hand, in time domain, scaling has resulted to design of faster circuits, while also contributing to reduction of jitter. This paper aims at verifying the effectiveness of the time domain circuits over voltage-domain circuits in terms of their dynamic range performances, where It has been shown that for a given technology the time domain dynamic range is superior to the voltage domain dynamic range by a factor of $(\omega T=B)^2$ where ωT is the unity gain frequency and B is the bandwidth.

To accurately estimate the impact of aging on the circuit reliability, a simulation technique of NBTI degradation under the actual operating condition is essential. Thus, we also propose a faster circuit simulation method for NBTI degradation in this study. By use of circuit elements to express the physical phenomenon of NBTI degradation, the proposed scheme has achieved the estimation of NBTI degradation simultaneously with the circuit simulation. In addition, the proposed method can realize accelerated degradation test by tuning the parameters of the circuit elements.

CMOS Imaging Sensing in THz band

Kunihiro Asada, Toru Nakura, Tetsuya Iizuka,
Parit Kanjanavirokju, Shinichi Miura

The reason that THz Imaging system cannot be widely commercialized is lack of portable, high-power, and cheap source. Photonics source is always large because it requires cryogenic system for efficient operation. Thus it is crucial that electronics source is developed. CMOS, as a standard technology for mixed-signal circuit in microwave technology, has a very good potential for implementation of compact THz system in the near future. However, CMOS operation is limited by F_{max}, which is well below 1 THz. We developed ideas of high frequency pulse generation that is not limited by F_{max}. Instead, high frequency component is extracted from fast falling edge generated by CMOS technology, using passive transmission line network. The idea has been verified by simulation result. The edge generator circuit as a part of the transmission-line-based pulse generator was also fabricated on 0.18-μm CMOS and 28-nm CMOS.

Lack of high directivity source is also a limiting fac-

tor for CMOS 3D imaging system. We propose a novel coherent imaging system which is superior to the conventional one in size, cost, and mobility and evaluated it with numerical simulations. The model is based on Hygens'principle. The shape of an unknown object is estimated by varying the directivity patterns of Tx and Rx array antenna, which are implemented on the same plane, and measuring received power repeatedly. Since transmitted patterns are used, constrain on directivity of antenna is loosen. A simulation result shows that if we have SNR of at least 10 dB, this model can estimates shapes with one wavelength accuracy by using proper set of directivity patterns for measuring power.

Estimation of wire current utilizing surface magnetic field for LSI security

Kunihiro Asada, Toru Nakura, Tetsuya Iizuka,
Yoji Nakamura

Sophistication of LSI is advancing while company with own fabrication is decreasing. They are outsourcing the manufacturing of LSI to companies overseas. This enables Cutting the budget of manufacturing, however danger of malicious modification to the chip increases. Method to find out this modification is needed and method utilizing path delay, power consumption and other side channel signal is studied. In this research method to estimate wire current of LSI while functioning utilizing surface magnetic field is proposed. Evaluation of proposed method was done in simulation and relation between height of probe, noise figure of amplifier, duration of measurement and accuracy of estimation was studied.

Rectifier for RF Energy Harvesting

Kunihiro Asada, Toru Nakura, Tetsuya Iizuka,
Hiroaki Matsui

In RF energy harvesting, where using ambient and faint radio waves as energy sources, a rectifier is needed to convert AC radio waves to DC. Usually, Dickson charge pump is used as a rectifier of RF energy harvesting. That has two problems, one of those is about forward voltage drop of diodes, and the other is about reverse current. In order to overcome these problems, we proposed the rectifier based on Dickson charge pump, which utilizes both the threshold control method and the threshold compensation method. The threshold control method uses body bias effect and the threshold compensation method applies amplified voltage to gate terminals. We evaluated the performance of the proposed rectifier as a start-up rectifier. As a result, when using only one of the two methods, the performance of the rectifier is not good if the load resistance is large or small. In contrast to this, the proposed rectifier is always better than Dickson charge pump even if the load resistance is large or small. In addition to this, we proposed output voltage universal curves, which normalize the relation between two design parameters, the antenna resistance and the load resistance. By utilizing this, the simulation process of rectifiers, which is laborious due to a lot of transient analyses, can be shortened.

Time-Domain Signal Processing and its Application for PLL Design

Kunihiro Asada, Toru Nakura, Tetsuya Iizuka,
Toshiyuki Kikkawa, Norihito Tohge, Koji Sato, and
Tomohiko Yano.

In this research, we are engaged in the improvement of Pulse Width controlled Phase Looked Loop (PWPLL). First, we improve the automatic design flow for PWPLL. We renovated maintainability and extensibility of software and increased the number of variable parameters to enhance the process portability. We demonstrated its process portability by applying it for the new 28 nm FD-SOI process. Moreover, we considered the adaptability of PWPLL against the process variability. In order to improve this adaptability, we designed a variable ring oscillator which can dynamically change the number of stages according to the control signals. The control signal is generated by a lock detector which detects whether the PLL is locked within a certain period or not. By HSPICE simulation, the modified PWPLL showed correct operation under process variability.

Also, we are working for utilizing time-domain signal processing. We proposed a Pulse Width Accumulator (PWACC) circuit for time-domain analog signal processing. PWACC integrates input pulse width and represents integrated value as output pulse width. In order to hold time-domain information in the integrator, the PWACC utilizes pulse regeneration ring where two short pulses run around keeping some time differences. By changing the positional relation between the two

pulses in the ring according to the input pulse width, the output pulse width becomes the integration of the input pulse width. We applied the PWACC to a PWPLL and made zero phase-offset PWPLL. A prototype was fabricated by 180 nm standard CMOS process. Time-domain information was also utilized for on-chip transfer function measurement of PLL. In our proposed measurement scheme, phase modulation to obtain the transfer function is carried out by switching delay on reference clock of the PLL. Then, the response of the loop is also observed by TDC as time-domain information. We are trying to apply this time-domain information to optimize a bandwidth of PLL under variable conditions.

Improvement of Detection in Radiation Detector Utilizing Semiconductor Photodiode Based on Standard CMOS Technology

Kunihiro Asada, Toru Nakura, Tetsuya Iizuka, Zhu Hongbo, Yang Xiao, Masaki Ikegawa

Scintillation detectors and semiconductor detectors have received widespread attention since they can specify the nuclide of radiation and estimate the arrival angle. However, traditional detectors have two disadvantages. One is that they can not be carried easily, the other is that they do not have enough spatial resolution of radiation position. In prior research, they proposed the detector using the cube scintillator, SPAD (Single Photon Avalanche Diode) array image sensors, multi-coated materials, and pinholes. Distributions of the detected photons on the SPAD array are simulated in advance, and that distributions are compared with the actual detection results to estimate the trajectory of an electron emitting light. Simulation results verified that the proposed detector realizes a higher spatial resolution than that of the conventional detectors.

Fujita Laboratory

(http://www.cad.t.u-tokyo.ac.jp/)

Post-Silicon Validation Techniques

Masahiro FUJITA, Takeshi MATSUMOTO, Amir Masoud GHAREHBAGHI, Satoshi JO, Choudhary SHRIDHAR

Due to increase of the size of VLSI, it has become very hard to detect all design bugs in design phases before fabrication, which increases the number of bugs that escape verification processes before fabrication and are firstly detected by running a chip after fabrication. In addition, a risk of electrical errors is increasing as fabrication processes shrink. Post-silicon validation techniques are to validate VLSI chips if there are erroneous behaviors caused by such bugs or electrical errors, and useful to avoid the additional costs required for re-spins. In this topic, we propose (1) an efficient method to derive logic functions for programmable circuits inside designs, which are inserted to improve a chance of validation, and (2) a method to select a set of flip-flops in a circuit so that the number of states that can be restored is maximum. The first method enables us to rectify a buggy circuit using programmability. We confirmed that our proposed method can work for ISCAS benchmarks with up to 100 programmable circuits. The second method is based on a formulation with Pseudo-Boolean Optimization (PBO), which guarantees that a solution is optimum if any solution is found. We are evaluating how large circuits can be solved by PBO solvers.

Post-silicon Debugging of Designs at Transaction Level

Masahiro FUJITA, Amir Masoud GHAREHBAGHI

Modern System-on-Chips (SoCs) are becoming more complex as their number of cores increases. As a result, pre-silicon verification methods cannot guarantee implementation of a bug free system. Hence, some bugs may escape to prototype or even final system. In this research, we introduce a post-silicon debug method that employs transactions among cores in a SoC. Our method is based on monitoring the communication behavior of the cores (i.e. transactions that are sent/received) and using them to backtrack from the current state of the system to the previous states to find the cause of errors. Backtracking is performed in the transaction-level model of the system, assuming that the design of the system has started from that level. First, we extract a transaction-level state machine of the system. Then, we employ the chip transaction trace to find the execution path on the extracted state machine. By using formal methods, we check the design properties on the extracted path to find the bugs as well as the constraints that caused the error. To show the effec-

tiveness of our method, we have selected a distributed deadlock detection and resolution algorithm as our case study. We have implemented it at transaction-level on top of a network-on-chip (NoC). We show that using our method, we can successfully backtrack at transaction-level as well as finding constraints on the internal variables that has leaded to the error.

Interconnect Synthesis

Masahiro FUJITA, Jiayi ZHANG

The emerging many-core system-on-chip design requires high performance, high reliable interconnect system. Network-on-Chip (NoC) is one of the candidates which may meet this requirement best. By deploying the NoC, the next generation of the interconnect structure, system designer can reduces the design effort significantly. However, to design a NoC which is able to be compatible to the protocols of existing IPs, to efficiently utilize the bandwidth and to be reliable is still a challenge. We would like to ease the design challenge by developing a tool which will automate the design process. This tool uses the protocols of desired IPs and the specification of data flows among these IPs as input information. It is able to automatically output the optimal interconnect with mesh network-on-chip as back bone and insert protocol converters for the mismatched IP pairs.

Verification and Debugging of Processor Architectures

Masahiro FUJITA, Amir Masoud GHAREHBAGHI, Takeshi MATSUMOTO, Satoshi JO

Processor architectures are becoming more complicated by adopting various functionalities for higher performance and more reliability, such as pipelining, speculative execution, and error recovery. To ensure the correctness of complicated processor architectures, verification and debugging of processor architectures are a key issue. In this work, we have proposed a method for debugging and automatic rectification of bugs in microarchitecture of processors. The proposed method first identifies bug locations in circuits, and then, finds out a set of input patterns for which an erroneous signal needs to be changed (i.e. inverted), in order to make the entire behavior of a circuit under debugging correct. As a result, we can get a corrected logic function for the erroneous signal. We confirmed that our proposed method successfully rectifies a control circuit in an out-of-order pipelined processor with an error recovery functionality. Also, when the control circuit is implemented by programmable circuits, rectification can be achieved by re-programming those programmable circuits without changing place and route.

Low Latency Computing using FPGAs

Masahiro FUJITA, Takeshi MATSUMOTO, Naoki TAGUCHI

For applications which require very low latency operations, application-specific hardware implementations can achieve lower latency than software implementations running on general purpose processors. This is because, in application-specific hardware, we can utilize customized memory systems and arithmetic circuit modules for a target application, and those modules and memories can run in parallel. In this research, for a line-handler in stock trading systems as an example, we implemented it on FPGA in order to achieve lower latency. A line-handler is used in high frequency trading such as algorithmic trading. It accepts buy/sell orders from clients and sends them to a stock exchange after formatting them to a specified format by the stock exchange. By executing with our FPGA system, behaviors of the line-handler can be completed several micro seconds, while a software implementation spends more than 20 micro seconds for the same behavior. For further lower latency, we have a plant to implement TCP communication processing as customized hardware as well as the line-handler.

Hardware Acceleration of Neural Network Simulation

Masahiro FUJITA, Takeshi MATSUMOTO, Kosuke OSHIMA, Taro KAWAO

Recently, improving simulation speed of scientific simulation using FPGA or GPU draws much attention from researchers in various fields, as it can realize a high-speed simulation with a low cost. In this topic, we have developed a FPGA-based neural network simulation. Our simulation is based on DSSN (Digital Spiking Silicon Neuron) model. In this model, we need to calculate a weighted sum of all values that are input to one neuron from other neurons through synapse.

To improve simulation speed, we introduced a pipeline processing to calculate this weighted sum. Since the capacity of BRAM in FPGA is limited, it is impossible to store all intermediate data inside FPGA when the number of neurons is large. To solve this scalability problem, we utilized on-chip RAM and stored intermediate results to RAM. We have developed and evaluated several FPGA circuits for neural network simulation, and confirmed that 1000 neurons can be simulated on FPGA.

Design Debugging Support

Masahiro FUJITA, Takeshi MATSUMOTO, Kosuke OSHIMA, Qinhao WANG, Takashi TOI, Takefumi KOGA

In hardware designs, a considerable time is spent for design debugging. Therefore, automated design debugging techniques are essential to improve design efficiency. In this work, we propose three methods to support design debugging. One is a method to derive a correct circuit by replacing some gates in a circuit with Look-Up Tables (LUTs) and finding a logic function implemented by LUTs when a specification and a circuit under debugging is equivalent. However, correction may not be feasible, depending on how LUTs are inserted. In the case, we add an input of LUT and connect it with a selected signal which satisfies some requirement condition. The second method is static analysis of embedded program with interrupt. Since functions that are called and executed when the main program is interrupted are usually decided at the time of interrupt, it is difficult to include such functions in a dependence graph of programs. Therefore, we propose to explicitly link those functions with the main function and make a dependence graph including those functions. In the last work, we propose a new coverage metric considering to detect mistakes of order of conditional branches. The coverage is calculated by examining all combinations of orders of branches with a set of test patterns. If the output of a program is different from the original, we decided that the branch order is covered. We have confirmed that, in some cases, this new coverage is sensitive to bugs in conditions or branch orders, while conventional coverage metrics are not.

Efficient Topological Matching Among Multiple Circuits

Masahiro FUJITA, Amir Masoud GHAREHBAGHI, Hossein IZADI RAD

Recognizing similarities and differences among multiple circuits is very useful for managing and maintaining IP libraries. In this work, we address the problem of finding the maximum common subcircuit among two or more logic circuits. Given the gate-level netlists of the circuits, first we represent the circuits as graphs. Then, we try to find the largest common subgraph, following the common approaches that are used for identifying matched graphs. In the first step, we build a conflict graph from the circuit graphs. In the next step, we try to find the largest common subgraph by finding independent sets of the conflict graph, using our proposed near-linear approximation algorithm. Finally, we try to increase the size of the largest common subgraph by considering neighbors of the circuit graph nodes, step-by-step in a controlled manner. We have performed extensive experiments on ISCAS85 circuits as well as a number of IPs from OpenCores. Comparing our results to the optimum solution that is obtained by an exact algorithm, the average size of the identified common subcircuit is around 10 % smaller, but the average processing speed is two to three orders of magnitude faster.

Hideya Ochiai, Assistant Professor,

(http://www.hongo.wide.ad.jp/~jo2lxq/)

Facility management with IEEE1888 and embedded systems

Hideya Ochiai

To manage and control the facilities for Smart Grid applications, designing and implementing interfaces and protocols for embedded systems to communication servers over the Internet is necessary. We have developed IEEE1888 protocol, implemented it onto such systems, and demonstrated that it allows the management and control of the heating, ventilating and air-conditioning (HVAC) systems, light systems and other facilities.

Architecture of IP packet delivery for buildings

Hideya Ochiai

This work integrates many communication media used for facility networking in buildings onto the Internet Protocol (IP). We have focused on "IP over RS485"and "IP over DTN"architecture, and developed the platform that provides IP reachability to the end nodes of such facility networks.

Takamiya Laboratory

(http://icdesign.iis.u-tokyo.ac.jp/)

Energy Efficient Extremely Low Voltage VLSI Circuit Design

Makoto Takamiya, Takayasu Sakurai, Hiroshi Fuketa

Reducing the power consumption of every electronic device is required to mitigate the global warming. To meet the requirement, VLSI circuit design techniques including logic circuits, memory circuits, analog circuits, power management circuits, and wireless transceiver circuits operating with the 0.5-V power supply voltage are developed with 65/45 nm CMOS process to reduce the power consumption to 1/10 of the conventional VLSI's.

Design of Large Area Electronics with LSI's and Emerging Devices

Makoto Takamiya, Takayasu Sakurai, Hiroshi Fuketa, Takao Someya, Tsuyoshi Sekitani

Large area electronics is a new frontier in electronics where intelligent electronic devices are distributed on a flexible surface, 10 cm to 10 m on a side, for the human interface and the comfortable daily life. Flexible and low-cost organic FETs (OFETs) are suitable for large-area electronics and have great potential as a supplement of solid and expensive silicon MOSFETs for VLSI's. We have proposed and demonstrated several large area applications combining OFETs and VLSI's and the relevant circuits including Braille display, a wireless power transmission sheet, a communication sheet, an EMI measurement sheet, and a User Customizable Logic Paper (UCLP).

Mita Laboratory

(http://www.if.t.u-tokyo.ac.jp)

Study on LSI-MEMS integrated pond-skating robot for energy-autonomous distributed microsystems

Y. Mita, I.Mori, Y. Li, A. J. Walton (Univ. of Edinburgh)

As one example of integrated MEMS that is expected to open new research and industrial application fields, the authors are trying to show a top-down application of energy-autonomous distributed microrobots. The research belongs to the "top-down"research category and through the research the team looks forward to provide the "Engineered Nature"; the team does not intend to just copy how nature works in implementation level, but to realize with cutting-edge technologies what nature is aiming at in highly-functional level. Recent top-down activities include autonomous distributed mobile robot: "Pond Skater", which to date had not been realized by any other microsystems group. The availability of a leading low voltage technology at the Scottish Microelectronic Centre (SMC) the University of Edinburgh that could electrically change surfaces from hydrophobic to hydrophilic proved to be crucial to achieving this goal as was the previous involvement of SMC staff in wireless technology. The major challenge is propulsion, and it is clear that directly mimicking the pond skating insect's propulsion mechanism would be problematic. The idea that was developed was to propel the device using Electro-Wetting Of Dielectric (EWOD) to move air bubbles, which had the significant advantage that there we no moving mechanical parts, which simplified the construction and helped to minimize the weight which was important if the ponds-kating device was to float using surface tension. Based on the world's first wireless pond-skating propulsion, the team is developing VLSI control circuit and integration technology for continuous skating. In FY2013, supporting technology, which is on-chip energy source is developed. High-voltage generating photovoltaic cell is ameliorated.

LSI-MEMS integrated device by submicron-wide opening deep reactive ion etching technology

Y. Mita, T.N.Binh, T. Sawamura, I.Mori, A.Hirakawa, M. Kubota

Narrow and deep structures such as microholes

and trenches are playing key roles in modern electro and mechanical systems. In standard micro fabrication technology, patterns are composed of rectangles and vertically transferred to the depth direction, yielding long-cubic structures. However, just by thinking of lens shape, one can realize that cubic shape is not necessarily the optimum shape for all kinds of applications. Hence it can be said that the ideal micro fabrication technology must be capable of realizing surfaces having arbitral curvatures that are top-down requested by applications. The team aims at acquiring comprehensive study on such "arbitral curvature providing micro fabrication technologies" from three aspects: (1) Top-down concrete applications, (2) Enabling micro fabrication methods by cutting-edge technologies and ideas, and (3) non-destructive profiling method of such surfaces. Top-down applications published in FY 2013 include (1-5) thermal energy harvester that takes full advantage of profile control by DRIE tuning, as well as "high-voltage compatible IC out of standard CMOS process.

Smart Blocks II project–Development of UV pattenable polyimide microactuator

Y. Mita, J. Malapert (FEMTO-ST), K. Yasuda, M. Ataka, H. Fujita

In a framework of French national research project (ANR) "Smart BlocksII", Dr. Julien Malapert stayed in Mita Lab., to develop a brand-new thermal microactuator array and control circuit. The principle of microactuator is thermal bimorph actuator developed by Ataka *et. al*; however the process required O_2 plasma ashing for patterning with hardmask, yielding 6 process steps par layer. To improve process efficiency, the team adopted new material that is photo-sensitive polyimide for structure, thus was successful in reducing process step into half of original one. Following successful demonstration of the microactuator array with maximum displacement amplitude of 15 μm and cut-off frequency of 10 Hz, the team worked on the LSI circuit that controls the actuator.

An LSI probing system with CMOS-MEMS

Y. Mita, K. Hosaka, R. Matsui, Y.-T. Chen (ITRI), and M. Kubota

With Taiwan Industrial Technology Research Institute (ITRI), the team is developing a "MEMS" probe card for electron device testing such as VLSI. The originality is to integrate CMOS preprocessing circuit to provide high functionality. In the year 2013, demonstration with real optical device, which is in fact LED wafer with high curving due to internal stress, was successful. The originality of the probe is that one probe pin has two independent tip that can be used as an "electrical detection"of probe touch down. Then it is experimentally shown the possibility to perform 4-terminal (Kelvin) measurement; the uncertainty due to contact resistance is suppressed.

Design and Development of Micro-Latch Mechanism for Low-Power and Long-Life MEMS Memory

Y. Mita, K. Komeda, M. Kubota, A. Tixier-Mita

A low-power and long-life MEMS memory having data retention time over 1,000 years, write power under pico-Joule, and zero power for data retention. One of the application scenarios is cumulative hazard (such as total exposure to radioactivity and or chemicals) memory. The proposed multi-level memory stores the information in terms of mechanical energy stored in the MEMS spring that may yield low-power writing energy and stable data retention. In the year 2013, which is the second year of the project, precision in the process is acquired.

Right-Brain-Computing Integrated Circuits: Associative Processing Systems

B. Ka, N. Yamashita, Y. Mita

Digital computers are dedicated machines for vary fast execution of numerical calculations. However, their performance is extremely poor in such tasks like seeing, recognizing, and taking immediate actions, which are effortless tasks in our daily life. This research aims at building intelligent VLSI systems based on the psychological model of a brain. In our system past experience is stored as template vectors in non-volatile vast memories and the maximum-likelihood event to the current event is recalled in real time by a fully parallel processing. The key ingredient of the system is a new functional device called "Neuron MOS Transistor" (neuMOS or *v*MOS) which mimics the action of a nerve cell neuron at a single transistor level. Based on such architecture that "association"is the very comput-

ing primitive, we are pursuing human-like intelligence system implementation directly in silicon integrated circuits. Currently research is in progress for robust image recognition and classification processing including robust feature extraction. The sate-of-the-art silicon technology has been utilized to implement such associative processors in both analog and digital CMOS VLSI chips.

CMOS-MEMS Device that Interacts Five Senses of Human Being.

Y. Mita, M. Honda, T. Hiraki, E. Shi

It is believed that MEMS may open new application field, including sensor and actuator system that interacts five senses of human being. The team aims at developing compact VLSI-integrated microdevices. The device is then distributed into environment; cooperation of the devices makes functionality in an efficient way. The development includes wide-range MEMS microphone that has no moving part, integrated-to-human-body actuator to stimulate taste, and prospective device for identification of the sound-origin orientation "Tetra-Pentachan".

"Sixth Sense" Devices with CMOS-MEMS Technology

Y. Mita, M. Denoual (ENSI de Caen, France),
Eric Lebrasseur, Camille Gay (INSA de Lyon, France),
Jean-Bernard Pourciel (LAAS-CNRS, France),
Takahisa Masuzawa (professor emeritus UTokyo)

One of the most important application field of MEMS is "sixth sense", which means that sensors that can detect physical and chemical amount that cannot be sensed by human beings'sensors. The team aims at solving this issue by VLSI-integrated compact microdevice. The development includes an integrated bolometer that can detect infrared wave very rapidly and sensitively, and integrated system that can make profiling of very small holes.

Takagi-Takenaka Laboratory

(http://www.mosfet.k.u-tokyo.ac.jp/)

Ge Metal-Oxide-Semiconductor (MOS) FETs

S. Takagi, M. Takenaka, Rui Zhang, Yu Xiao, J. Rin, WuKang Kim, Katsuaki Tanaka

We have conducted the research on high-peformance Ge MOSFETs. We have investigated ECR plasma oxidation after depositing Al_2O_3 on Ge by the ALD to form high-quality Ge MOS interface. We have successfully formed high-quality gate stack on strained Ge grown on a Si substrate. We have achieved high-performance strained Ge p-MOSFETs using this gate stack. We have also conducted the research of reliability of Ge gate stacked formed by plasma oxidation. We have also investigated Ge condensation to form Ge-on-Insulator wafers. By using Sb doping from SOG, we have successfully demonstrated n-MOSFETs on the GOI wafer.

III-V compound semiconductor Metal-Oxide-Semiconductor (MOS) FET

S. Takagi, M. Takenaka, M. Yokoyama, S.H. Kim, Chih-Yu Chang

We have conducted the research on high-performance III-V MOSFETs. We have successfully demonstrated Ni-InGaAs metal S/D self-aligned InGaAs MOSFETs on the III-V-OI wafer fabricated by the direct wafer bonding. The well-behaved FinFET operation has been obtained even scaling the gate length down to 20 nm. We have also demonstrated GaSb-OI wafer by using a GaSb layer grown on an InAs wafer. By using InAs passivation, high-performance GaSb p-MOSFETs have been demonstrated.

Tunnel FET

S. Takagi, M. Takenaka, M. Kim, Sangmin Ji

For low-power application, tunnel FET, which can exhibit steep subthreshold slope have been investigated. We have developed Zn diffusion from Spin-on-Glass (SOG) for forming high-quality junction, and successfully demonstrated lateral InGaAs TFET exhibiting a subthreshold slope of approximately 60 mV/dec. Ge/Si hetero-junction TFETs have also been investigated. By using in-situ B doping in Ge, we have improved the TFET operation.

Ikeda Laboratory

(http://www.mos.t.u-tokyo.ac.jp)

Si CMOS photonics

M. Takenaka, S. Takagi, Y. Kim, J. Han, J. Kang

High-sensitivity Ge photodetectors (PDs) has been investigated. It is found that GeO2 surface passivation formed by plasma post-oxidation can reduce the surface leakage current of MSM Ge photodetectors by one order of magnitude. We have found the relationship between the surface potential and the dark current of Ge PDs. We have also investigated SiGe optical modulators. We have successfully demonstrated enhanced plasma dispersion effect in strained SiGe in the lateral PIN-junction SiGe optical modulators. SiGe MOS interfaces for modulator application have also been investigated. We have found that plasma post-nitridation can improve interface traps density of the SiGe MOS interface by one order of magnitude. By introduction high-k dielectric, the feasibility of EOT scaling of SiGe gate stack down to 1 nm is demonstrated.

III-V CMOS photonics

S. Takagi, M. Takenaka, Y. Chen, Y. Ikku,
Park Jinkwon, M. Kuramochi

High-performance electronic-photonic integrated circuits using III-V-OI wafer have been investigated. An InGaAsP photonic-wire optical switch driven by current injection has been demonstrated for the first time. The InGaAsP optical switch exhibited 1/10 time drive current as compared with Si owing to the large free-carrier effect in InGaAsP. We have also demonstrated low-crosstalk switching owing to the large free-carrier induced refractive index change. A waveguide InGaAs photodetector monolithically integrated with an InP photonic-wire waveguide is also demonstrated for the first time.

2D CMOS photonics

S. Takagi, M. Takenaka, T. Kayouda, K Sasaki

Graphene-based photonic devices have been investigated. For realizing Graphene optical modulators, we have investigated graphene-gate-metal MOS capacitors, revealing that the chemical potential in graphene can be modulated up to 0.5 eV. Thus, we can show the feasibility of the graphene optical modulators. We have also conducted the research of transistors based on 2D transition metal dichalcogenides such as MoS_2.

Self-Synchronous System Realization

M. Ikeda, A. Ito, M. Tamura, D. Sai, T. Nishibe, H. Li

To decrease the energy consumption of LSI, operating by low voltage is proposed. Variation decrease reliability in low voltage. We proposed using gate-level pipelined self-synchronous circuits for low voltage operations. We proposed gate-level dynamic body-bias control by utilizing activity ratio of completion detection signal in gate-level self-synchronous circuit. With this control, power consumption when gates are under condition of waiting of valid signals has reduced by 90% with delay increase less than 10%. We proposed design automation flow using logic synthesis and P&R for this gate-level self-synchronous circuits. Soft error due to the collision of neutron from cosmic rays may cause LSI operation to be unexpected situation. In this research we investigated SEU tolerance of self-synchronous circuits by analyzing the types and influences of SEU.

3D-range finding by Smart Image Sensors

M. Ikeda, X. Hu, H. Yabe, and T. Matsushima,
R. Ishikawa

Our research topics are about CMOS image sensors that are specialized on 3-D image acquisition based on light section. We proposed a CMOS image sensor that employs in-pixel maximum voltage circuit to detect the sheet light on the pixel array, thereby reducing the data transmission required for 3-D shape reconstruction of a target object. A 0.18 um CIS process was used for the design and simulation. We also investigated texture mapping of real objects with a chip equipped with two image sensors for simultaneous measurement of 2-D and 3-D, calculation corresponding point, and pasting 2-D images on 3-D polygons. Using a scan light used in light section method as a light source of 2-D photographing, we aim at 2-D and 3-D high-speed simultaneous measurement under the dark environment. For this photographing method, we redesigned dual core imager in CIS process (Mr. Mandai designed previous chip in 0.18 um Rohm process). In 3-D image acquisition with the light-section method, an image sensor can suppress

background illumination by the use of modulated light and correlation technique. However, a sensor needs correlation circuits and pixel size becomes very large if each pixel has a correlation circuit. Therefore, we study an image sensor which has correlation circuits in the outside of the pixel array. The sensor searches the region which light is projected on in each scan. So, it doesn't need many correlation circuits and obtains high resolution due to small pixels.

Near field communication system

M. Ikeda, and K. Miyazaki

We have studied wide-band spectrum capture systems for white-space searching for such like cognitive radio, which uses white space for the communication by detecting available channels. We have investigated a wide-band spectrum capture systems.

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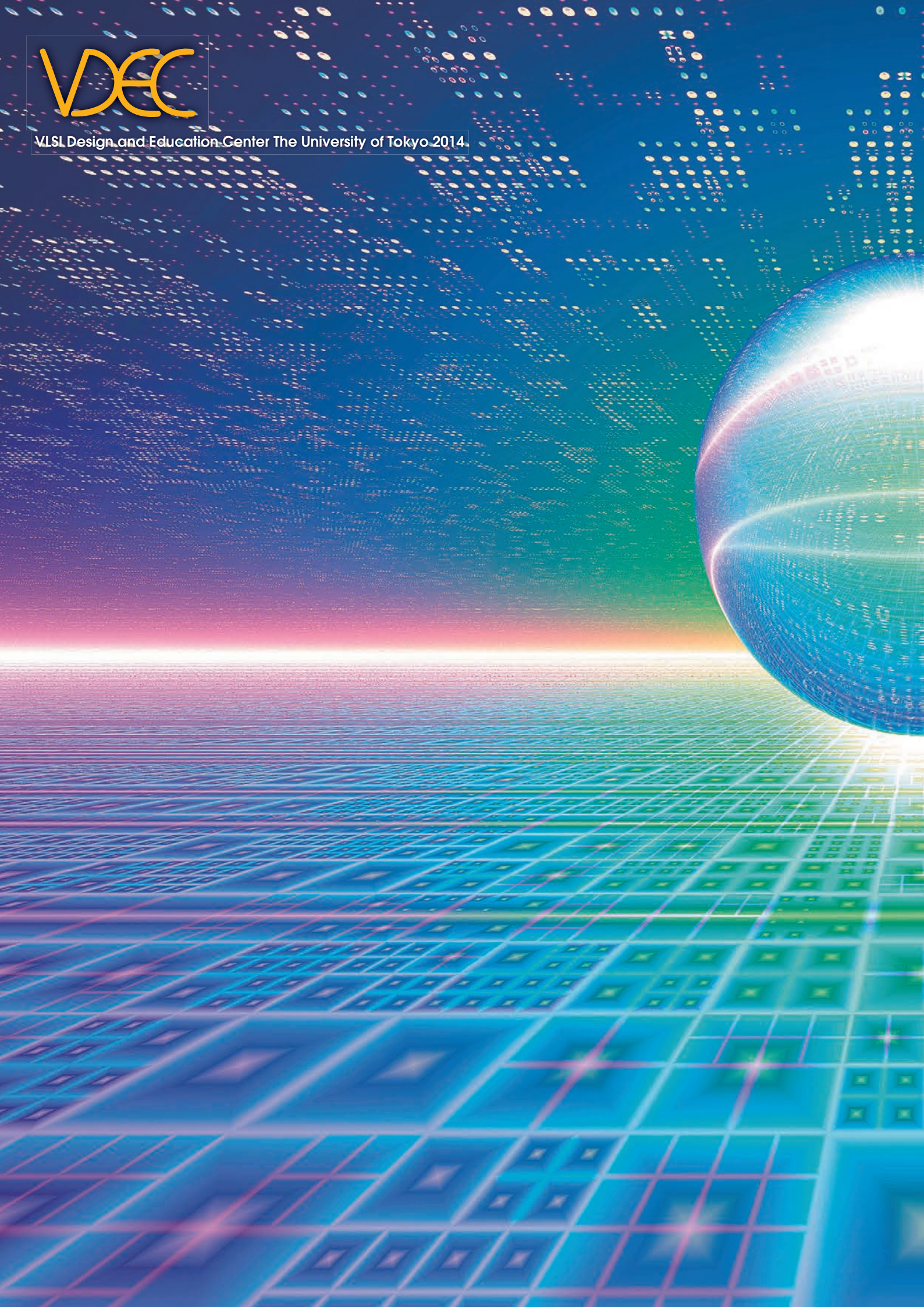
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