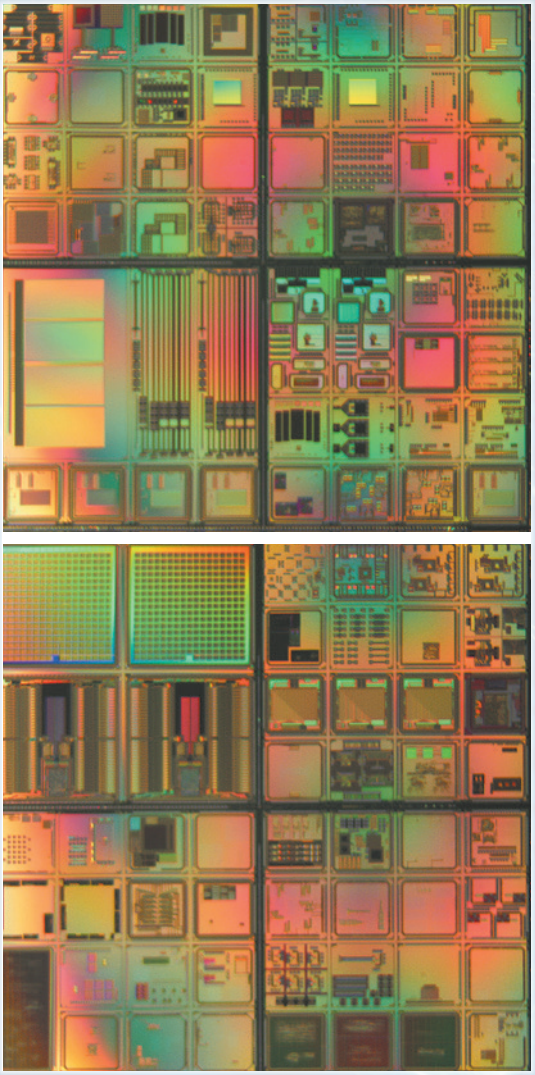
VDEC

平成28年度

東京大学
大規模集積システム設計教育研究センター
年 報

2016
VLSI Design and Education Center, The University of Tokyo Annual Report



VLSI Design and Education Center The University of Tokyo 2016

VLSI Design and Education Center
The University of Tokyo

This is the 2015 Annual Report of VDEC（VLSI Design and Education Center, University of Tokyo）.

In 2015 LSI chip design/implementation and processing of nano-fabrication facilities went well as previous years. This year, however, was the final year of the 6-year-plan of our University, so that a lot of time was spent on discussions about the next 6-year-plan. Our University decided to introduce the key process indicator (KPI) for the assessment of activities in Divisions. VDEC also decided a policy to define our KPIs. The basis of VDEC activities is LSI chip design/implementation and processing of nano-fabrication facilities, Our KPIs are numbers of new LSI chips and nano-fabrications. The former is now stable and the latter is still increasing. VDEC has also set new targets to be promoted in future, namely the internationalization and the industrialization, to which VDEC has been proceeding for several years.

Though instability of budget, due to KPI fluctuation, is not favorable for the stable inter-university collaborative projects, the major portion of the VDEC budget has been guaranteed as a stable budget thanks to understanding of the President of our University. However, the gradual reduction of the budget of 1-2% per year will continue for the next 6 years. Following intensive discussions at the VDEC Nationwide Advisory Board, VDEC decided to introduce a supplementary charge system from 2016. Each CAD user/laboratory will be requested to contribute 50k – 100k yen/year depending on the number of licenses, though CAD use for education purposes will be free of charge as it was. VDEC would like to ask for users' understanding. It is unavoidable in order to keep a stable VDEC CAD license system for future.

The CAD licenses of VDEC are restricted for the purpose of education and research in academia. These cannot be used for designs targeting industrial/commercial purpose. Because of the stagnant status of Japanese semiconductor industry, however, such cases are increasing as the national projects, where academia are requested to more actively contribute the information society in terms of IoT and AI, exceeding the restriction of the CAD licenses of VDEC. International collaborative researches with developing countries would be often in the same situation. The developing countries are aiming at industrialization of LSI designs. VDEC is recognizing the need of the new CAD environment bridging between academia and industry. VDEC is trying to realize it step by step, so that students/researchers trained by VDEC system can bring their design ability into full play.

As the annual event of the D2T (Design-to-Test) research division, donated by Advantest Corporation, the 10th symposium was successfully held on August 21st 2015, inviting distinguished lecturers from oversea and domestic institutes. We are scheduling the 11th symposium in September 21st this year, too. We would like to express our sincere thanks to invited lecturers, audiences and Advantest Corporation for the continuous support.

We will continue to do our best efforts for the original mission of VDEC, "promotion of education and research in LSI design by means of practical chip-design and implementations", in order to realize research and education for enhancing the value of the semiconductor technology. We thank you for your continuous supports again.

May 2016

VLSI Design and Education Center, University of Tokyo
Director　Kunihiro Asada

VLSI Design and Education Center, The University of Tokyo
Annual Report 2016

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Chapter 1 Activity Report of VDEC

1.1 Introduction of VDEC activities and activity report of FY2015

VLSI Design and Education Center(VDEC), University of Tokyo was established in May 1996. VDEC has been operating for the following 3 major roles: "spreading the latest information on VLSI design and education," "providing licenses of CAD tools," and "supporting on VLSI chip fabrications for academic use." The VDEC activity report of FY 2015 is described hereafter according to Fig. 1. 1.

The missions of VDEC are for advancement of researches and education on LSI design in public and private universities and colleges in Japan and send many distinguished VLSI designers into industry. After 19 years of VDEC establishment, educations on CAD software, LSI design and design flow in universities have been well established. On the other hand, advancement on nano-meter CMOS technologies forces design flow and CAD software complicated. We have been continuing CAD tool seminar by the lecturers from EDA vendors for twice a year. We hold the seminar in VDEC and provide distance learning through video streaming. We expect spread of the up-to-date LSI design methodology by using CAD tools.

We assume our LSI design flow seminars as educations on basic LSI design concepts and practical experience of LSI design with CAD tool chain. VDEC holds "LSI design education seminar", a.k.a. VDEC Refresh Seminar, once a year. This year we hold 3 courses, "Analog design course" and "RF design course", and initiated "MEMS design course" in May-July time frame. We invite experienced professors among universities as lecturers for the courses to conduct LSI design education courses with practical experience. We also hold "Transistor level design flow in VDEC" and "Digital design flow in VDEC EDA environment" for designers in universities. We started to charge these two LSI design education courses, as well as VDEC Refresh Seminars.

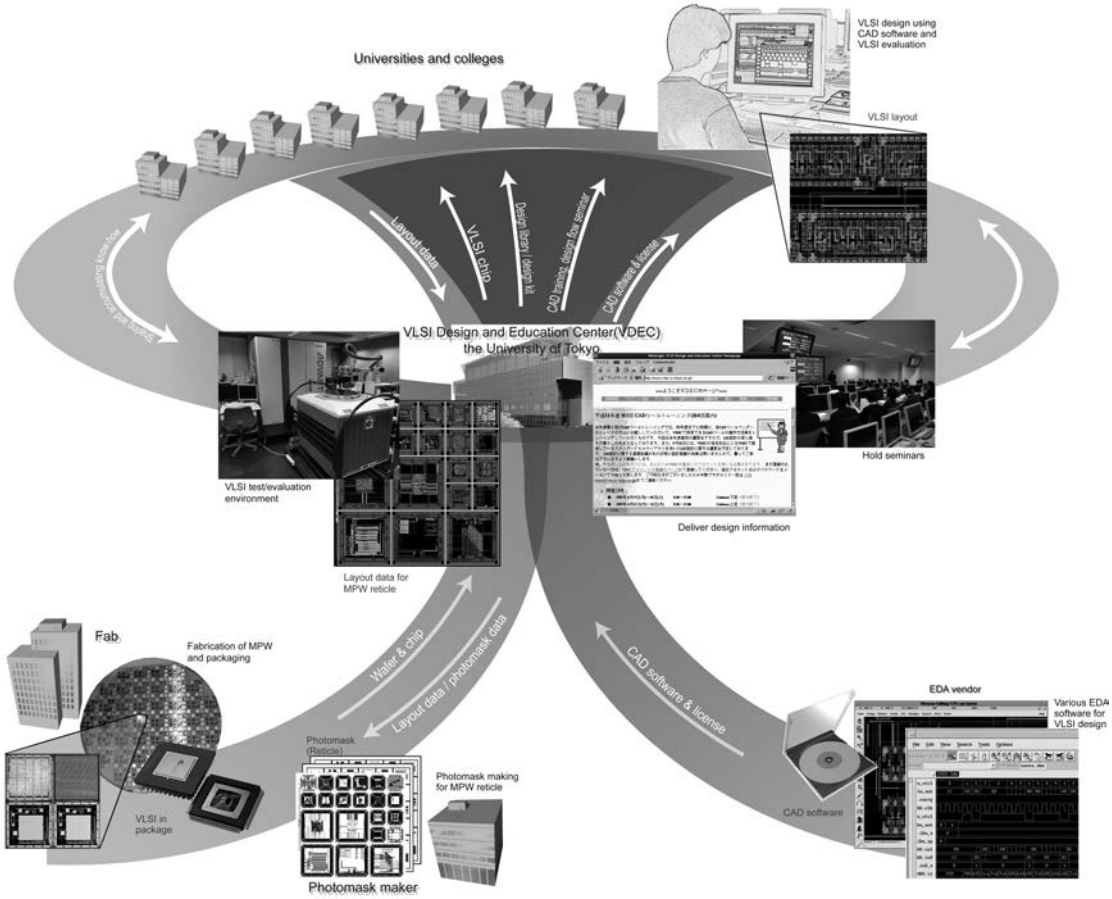


Fig. 1. 1 VDEC activities

In addition to the above seminars, we hold "VDEC Designer'Forum" among young professors and students annually. This is a workshop that the participants exchange their design examples with not only success stories but also their failure stories, in addition to invited talks. We expect students and professors who will start designs to learn kinds of know-hows. We have initiated "IEEE SSCS Japan Chapter VDEC Design Award" this year, and final examination and awarding have carried out during the "VDEC Designer'Forum". Mr. T. Ozaki (Kobe Univ.) is awarded as "IEEE SSCS Japan Chapter VDEC Design Award" winner, and Mr. H. Hayami (Nara Institute of Science and Technology (NAIST)), Mr. K. Nakata (Tokyo Institute of Techology (TITECH)), Mr. K. Kaiwa (Yamagata Univ.) are awarded as "the best VDEC Design Award", and Mr. H. Okuhara (Keio Univ.), Mr. R. Matsuzuka (Kobe Univ.), Mr. T. Kawajiri (Keio Univ.) are awarded as the "VDEC Design Award."

LSI designers come up against various difficulties during actual LSI design scene, even after the basic educations through various seminars and the forum. One of the biggest problems for beginners is the setup of CAD softwares. Many of them also get confused by "Esoteric messages" come out from CAD softwares, even after they successfully setup CAD tools. In such situations, VDEC mailing-lists make significant contributions. VDEC users can register to VDEC mailing-lists on CAD tools, and process dependent groups through VDEC web pages, and can ask questions and helps on their facing issues. It is not a responsibility for the registrant of such mailing-lists to give answers to questions, however, in most cases, replies are given by the experienced users of CAD tools and experienced designers within a couple of hours to a couple of days. Moreover, emails are accumulated and are open to the VDEC users, as shown in Fig. 1. 2, who have registered VDEC accounts, as the important educational assets. We expect all the VDEC users to make the full use of this mechanism to help solve problems.

We continue chip fabrication services on FDSOI CMOS 28 nm by ST Microelectronics, 0.18 μm CMOS by Rohm and 0.8 μm CMOS by On-semi Sanyo Semiconductor. And started chip fabrication services on SOTB CMOS 65 nm by Renesas Electronics.

Our donated division "Design To Test(D2T)", which was founded by donation from Advantest in Oct. 2008, focuses on enrichment of education on LSI testing and bridging between design and testing.

Fig. 1. 4 shows trends of number of papers through VDEC activities. Number of papers is increasing, which means researches in the field of VLSI design have been encouraged after VDEC establishment.

Fig. 1. 5 shows number of papers related to CAD usage, chip fabrications and VDEC facility usages. CAD tools are widely used to write papers. CAD tools are used not only chip designs themselves but also used for preparation of chip fabrication and they contribute to verify fundamental ideas of researches. Advanced CMOS processes are preferred for publications, and not only papers with 65 nm/40 nm CMOS chips, but also with 32 nm CMOS, 22 nmCMOS and 14 nmCMOS are emerging in the world. We would like to prepare chip fabrication services for the advanced CMOS processes. In addition, we would like to setup chip fabrication services related to CMOS/MEMS to fulfill the researches for "More than Moore". We also

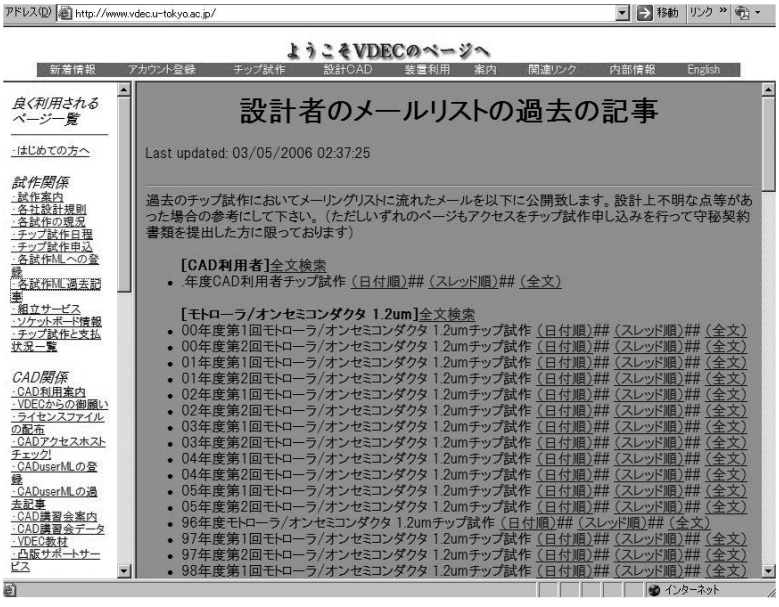


Fig. 1. 2 Archives of emails of VDEC mailing-list.

encourage researchers to fully use of VDEC facilities such like LSI testers, FIB systems and EB writer for the wide spread of research purposes.

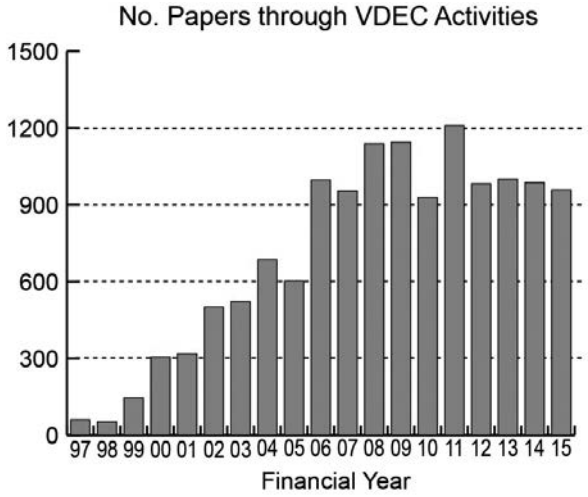


Fig. 1. 3 Trends of number of papers through VDEC activities.

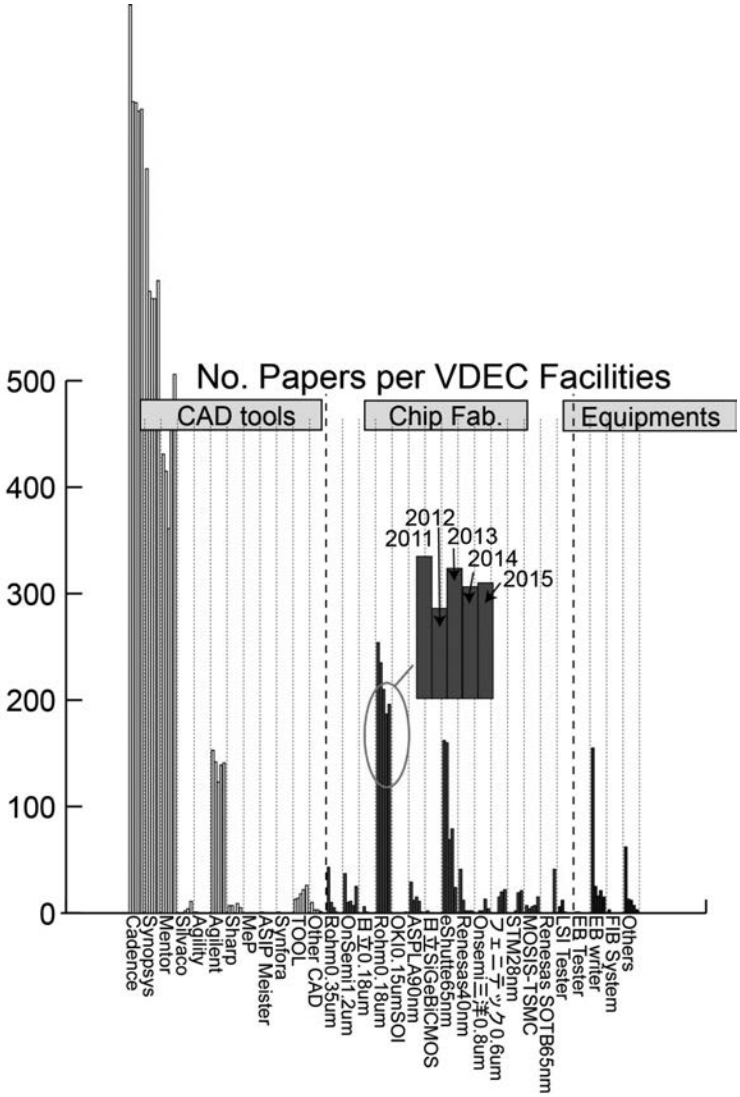


Fig. 1. 4 Number of papers related to VDEC facilities.

1. 2 VDEC CAD Tools

Since 1996, VDEC has provided CAD software licenses to the registered researchers in universities and colleges in Japan. The CAD tools we p-rovided in 2016 are shown in Table 1. 2. 1. The researchers can use those CAD tools when their local machines, whose IP addresses are registered in advance, are authorized by one of VDEC license server located in the ten VDEC subcenters shown in Figure 1. 2. 1. For each CAD tool, VDEC provides 10-100 floating licenses. Those CAD tools can be utilized only for research and education activities in national universities, other public universities, private universities, and colleges.

When one is going to use VDEC CAD tools and chip fabrication service (the details are described in Section 1-3), some faculty member of his/her research group in a university or a collage needs to do user registration. Figure 1. 2. 2 shows (a) the number of registrants, (b) the number of distinguished universities/colleges of the registrants, and (c) the number of registrants who applied VDEC CAD tools.

Table 1. 2. 1 VDEC CAD tools

Name	Function	Vendor
Cadence tool set	Verilog-HDL/VHDL entry, Simlation, Logic synthesis, Test pattern generation, Cell-based (including macros) place, route, and back-annotation, Interactive schematic and layout editor, Analog circuit simulation, Logic verification, Circuit extraction	Cadence Design Systems, Inc.
Synopsys tool set	Verilog-HDL/VHDK simulation, Logic synthesis, Test pattern generation, Cell-based (including macros) place, route, and back-annotation, Circuit simulation, Device simulation	Synopsys, Inc.
Mentor tool set	Layout verification, Design rule check	Mentor Graphics Co. Ltd.
Silvaco tool set	Fast circuit simulation	Silvaco
ADS/Golden Gate	Design and verification of high-frequency circuits	Keysight Technologies
Bach system	BachC-based design, synthesis, and verification	Sharp
LAVIS	Layout visualization platform	TOOL

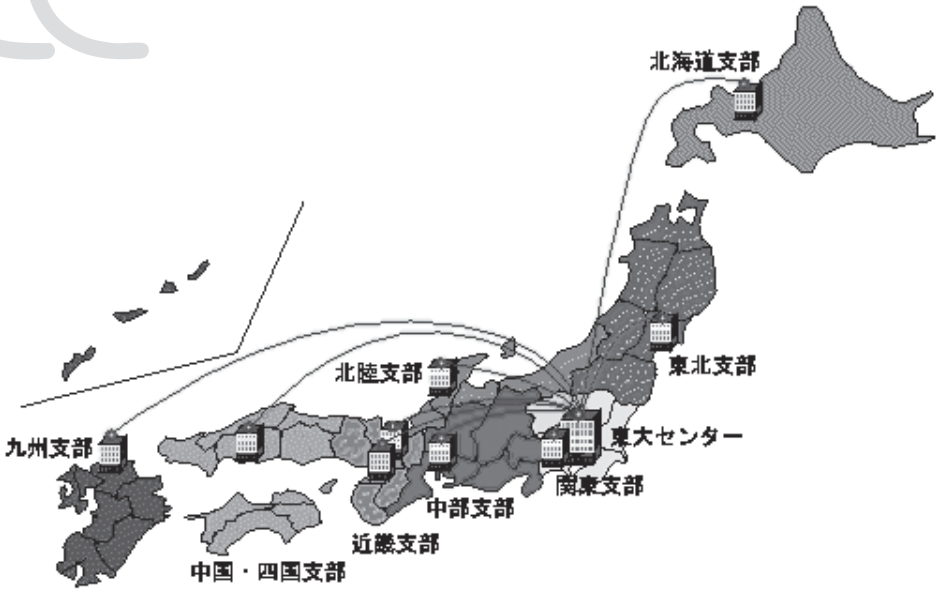
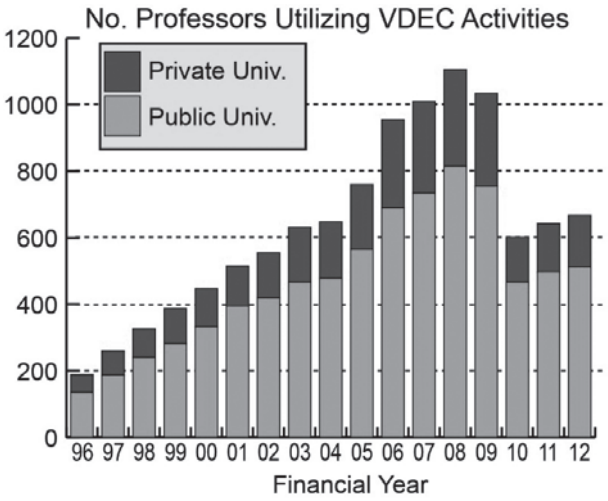
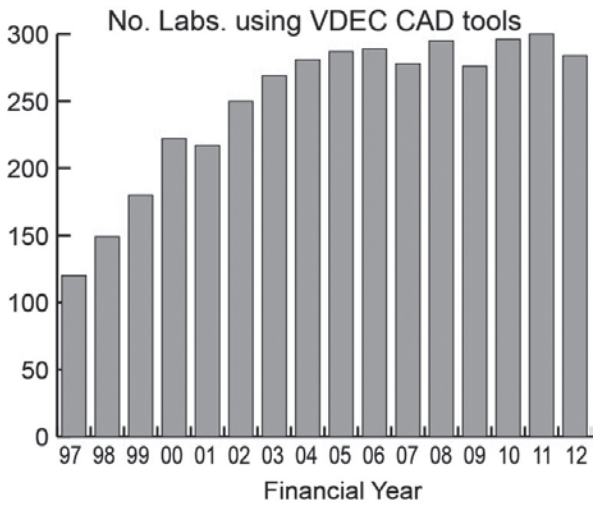


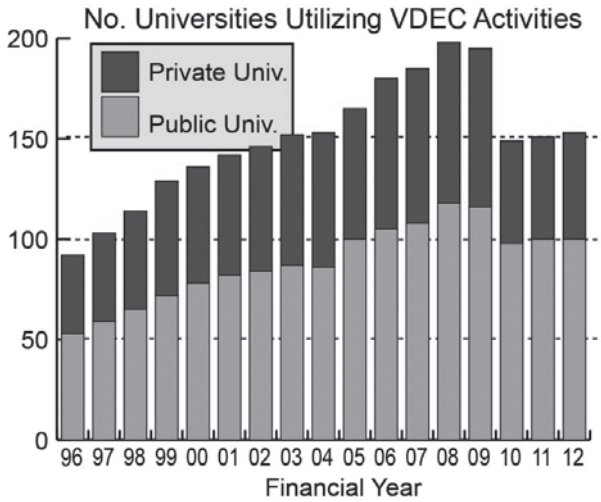
Fig. 1. 2. 1 VDEC Subcenters



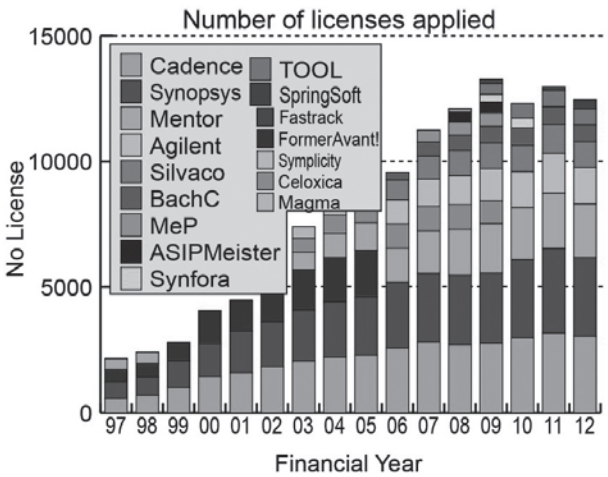
(a) The number of registrants



(c) The number of research group applied CAD tools



(b) The number of universities colleges of the registrants



(d) The number of applied licenses of all CAD tools

Fig. 1. 2. 2 The numbers of VDEC CAD Applications

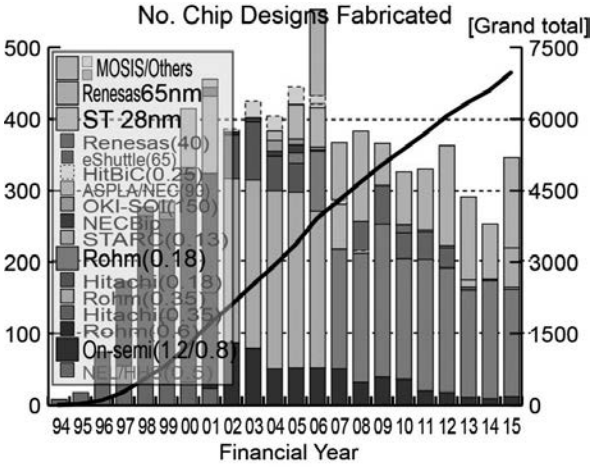
1. 3 VLSI Chip Fabrication

1. 3. 1 Trends of VLSI Chip Fabrication Services

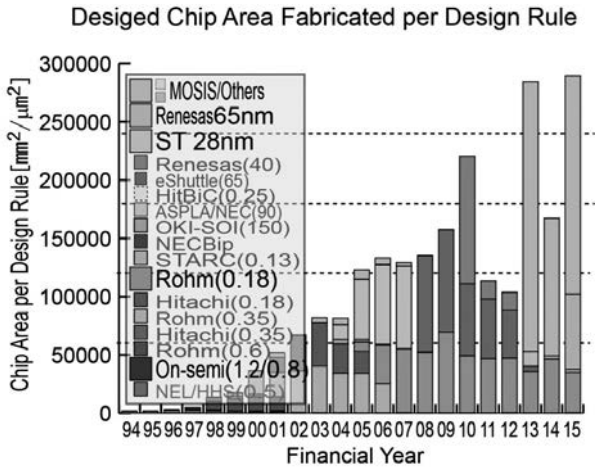
Fig. 1. 3. 1 shows a trend of number of designed chips for VDEC chip fabrication services, including pilot project prior to VDEC establishment.

VLSI chip fabrication is limited to 0.5 μm CMOS provided by NTT Electronics during the pilot project in 1994 and 1995. VDEC chip fabrication had started in 1996 with 1.2 μm CMOS provided by Motorola Japan, which is now On-Semiconductor as well as the 0.5 μm CMOS. In 1997, VDEC received cooperation from Rohm and has started 0.6 μm CMOS process. In 1998, VDEC started chip fabrication services of 0.35 μm CMOS by Hitachi, and in 1999, VDEC started 0.35 μm CMOS by Rohm. We had a test chip fabrication of 0.13 μm CMOS by STARC through "IP development project" in 2001. We added 0.18 μm CMOS by Hitachi into our chip fabrication menu in 2001. From 2002, we started VDEC-MOSIS chip fabrication program initiated by Prof. Iwata of Hiroshima University. Under this program, VDEC member can access to TSMC and IBM processes with lower price. We also started Bipolar chip fabrication by NEC Compound Semiconductor Devices. In 2004, we started 0.15 μm SOI-CMOS chip fabrication by Oki Electric as test chip fabrications. In the same year we started 90 nm CMOS chip fabrication by ASPLA/STARC. In 2006, we started 0.18 μm CMOS by Rohm and 0.25 μm SiGeBiCMOS by Hitachi. In 2008, we started 65 nm CMOS process by eShuttle, after closure of 90 nm CMOS chip fabrication in 2007. In 2010, we started 40 nm CMOS process by Renesas Electronics through "Next Generation Semiconductor Circuits & Architecture" project between METI and STAR. On the other hand, 1.2 μm CMOS chip fabrication program came to end by the September 2011. 40 nm CMOS by Renesas Electronics and 65 nm by eShuttle also come to end by Oct. 2012 and Aug. 2013, respectively. We started CMOS 0.8 μm in Oct. 2012 by On-semiconductor-Sanyo as a test chip fabrication and opened it as the regular chip fabrication menu in 2012. We started FD-SOI 28 nm CMOS by ST-Microelectronics through CMP, France, as the advanced CMOS process in 2013. We started SOTB 65 nm CMOS by Renesas Electronics in 2015.

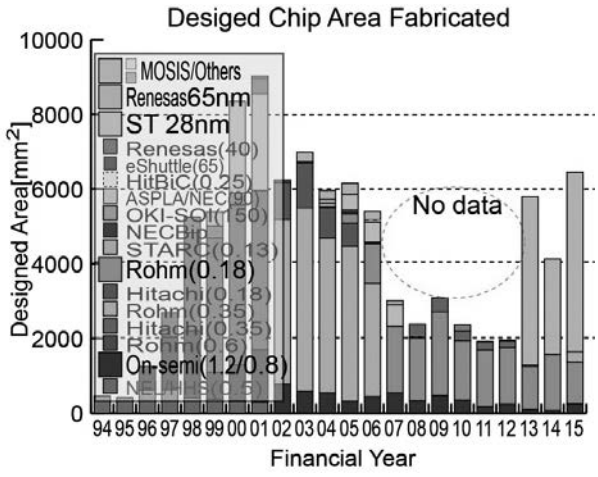
Fig. 1. 3. 1(a) shows trends of number of chip designed for VDEC chip fabrication. For the first 6 years until 2001, the number of designed chips shows steady increase, which means drastic improve of the effectiveness researches and education of LSI design, and we assume drastic increase of number of students related to LSI chip



(a) Trend of number of designs fabricated.



(b) Trend of designed area.



(c) Trend of designed area normalized by design rule.

Fig. 1. 3. 1 Trend of number of designs and designed chip area.

design and education. During few years of stable number around 400 chip designs per year, we can see transition of designs toward finer process. In 2007, we saw a large drop, which was caused by sudden process transition from 0.35 μm CMOS to 0.18 μm CMOS, and in 2008, we also saw another drop by process transition from 90 nm CMOS to 65 nm CMOS.

Fig. 1. 3. 1(b) shows trends of designed chip area, which shows much clear trends of drop by process migration. On the other hand, Fig. 1. 3. 1(c) shows trends of designed chip area normalized by design rule, which assume to be strong relation with design efforts. Coming from the fact that the normalized chip area is still growing, we assume the major reason for decrease of number of chips and designed area is increase of design effort per chip and per unit area due to process scaling.

Fig. 1. 3. 2 shows trends number of professors and universities fabricated chip. Number of professors who have contracted NDA for process technologies to access design rules and design libraries are, 64, 274, and 36, respectively, for 65 nm CMOS, 0.18 μm CMOS, and 0.8 um CMOS.

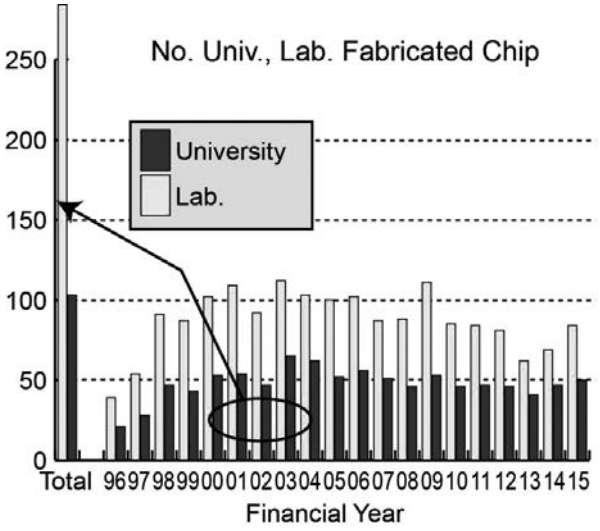


Fig. 1. 3. 2 Trend of number of processors and universities fabricated chip.

1. 3. 2 Overview of chip fabrication in 2015

Table 1. 3. 1 lists chip fabrication schedule in 2015. Please refer to list in Chapter 2 for details of designers and contents of chip designed.

Table 1. 3. 1 Chip fabrication schedule in 2015

○ **0.8 μm CMOS (On-Semiconductor - Sanyo)**

	Chip application deadline	Design deadline	Chip delivery
2015 #1	2015/ 7/ 6	2015/ 9/28	2015/12/13
2015 #2	2015/12/29	2016/ 3/22	2016/ 6/24

○ **0.18 μm CMOS (Rohm)**

	Chip application deadline	Design deadline	Chip delivery
2015 #5	2014/11/ 3	2015/ 1/26	2015/ 5/21
2015 #2	2015/ 4/13	2015/ 7/ 6	2015/10/21
2015 #3	2015/ 6/ 1	2015/ 8/24	2015/12/ 4
2015 #4	2015/ 8/24	2015/11/16	2016/ 2/26
2015 #5	2015/11/ 2	2016/ 1/25	2016/ 6/22

○ **28 nm CMOS (STMicro/CMP)**

	Chip application deadline	Design deadline	Chip delivery
2015 Nov.		2015/10/E	2016/ 6/17
2016 March		2016/ 3/B	2016/ 9

1. 3. 3 Libraries and design flows

VDEC have been working to prepare design libraries and design flows for digital design and PDKs for analog design. Table 1. 3. 2 lists libraries available now.

Table 1. 3. 2 Libraries available for VDEC chip fabrication

Technology	Name	Author	Contents
0.18 μm CMOS (Rohm)	Rohm library	Rohm Library Std. Cells, IO cells, RAM (Distributed with CDROM)	Synthesis(Synopsys)
			Simulation(VerilogXL)
			P&R(LEF/DEF)
	Kyodai Library	Onodera Lab., Kyoto University	Synthesis(Synopsys)
			Simulation(VerilogXL)
			P&R(Astro)
	Todai Library	VDEC Design flow based on library prepared by Onodera Lab., Kyoto University	Synthesis(RTL Compiler)
			Simulation(VerilogXL)
			P&R(Encounter)
	PDK	VDEC	PDK(IC6.1)

1.4 Seminar

Seminar is indispensable for the improvement of LSI design technology. Some seminar and forums, such as technical seminar for CAD use, refreshing seminar for working people, designer's forums for young professors and students were held in 2011.

【Technological seminar for CAD use】

In a technological seminar for CAD use, VDEC invites lecturer from each tool vender, such as Cadence, Synopsys and Agilent, to hold the CAD operation course. Moreover, the course concerning the design flow in the VDEC environment was held by the VDEC staff. A technological seminar for CAD use for the beginner was held in The University of Tokyo VDEC in August and September at the year 2015. This seminar took 4 days for 2 kinds of Cadence tools, 4 days for 3 kinds of Synopsys tools, 1 days for 1 kind of Keysight tool. In addition, VDEC teachers gave lecturers on transistor level circuit design course, and digital circuit design course under the VDEC EDA environment. Teachers and students up to 40 people attended a lecture in each course, and master the use of each tool for VLSI design flow that uses the VDEC library. Moreover, another technical seminar for CAD use for matured teachers and students was held in March by Cadence 3 kind and 5 days, Synopsys 4 kinds and 4 days (Table 1. 4. 1). The demand for these CAD technological seminars is very large, and VDEC has maintained the mechanism of a large-scale CAD technological seminar holding corresponding to this situation. So far, the seminar was held at the University of Tokyo OR other VDEC branch, however, we started to distribute the lecture using Web streaming, so that students around VDEC branch can take the seminar at the branch school.

Table 1. 4. 1 CAD technological seminar in summer of the year 2013

2015/07/27	Cadence ADE Seminar	Univ. of Tokyo	13
2015/07/27	Cadence ADE Seminar	Hokkaido Univ.	5
2015/07/27	Cadence ADE Seminar	Tohoku Univ.	4
2015/07/27	Cadence ADE Seminar	Kanazawa Univ.	1
2015/07/27	Cadence ADE Seminar	Nagoya Univ.	7
2015/07/27	Cadence ADE Seminar	Nagasaki Univ.	5
2015/07/29-31	Cadence Virtuoso Seminar	Univ. of Tokyo	21
2015/07/29-32	Cadence Virtuoso Seminar	Hokkaido Univ.	5
2015/07/29-33	Cadence Virtuoso Seminar	Tohoku Univ.	3
2015/07/29-34	Cadence Virtuoso Seminar	Kanazawa Univ.	1
2015/07/29-35	Cadence Virtuoso Seminar	Nagoya Univ.	3
2015/07/29-36	Cadence Virtuoso Seminar	Kyoto Univ.	4
2015/07/29-37	Cadence Virtuoso Seminar	Hiroshima Univ.	2
2015/07/29-38	Cadence Virtuoso Seminar	Nagasaki Univ.	5
2015/09/09	Synopsys DesignCompiler+PowerCompiler Seminar	Univ. of Tokyo	15
2015/09/09	Synopsys DesignCompiler+PowerCompiler Seminar	Tohoku Univ.	4
2015/09/09	Synopsys DesignCompiler+PowerCompiler Seminar	Osaka Univ.	5
2015/09/09	Synopsys DesignCompiler+PowerCompiler Seminar	Hiroshima Univ.	4
2015/09/11	Keysight GoldenGate Seminar	Univ. of Tokyo	10
2015/09/11	Keysight GoldenGate Seminar	Tohoku Univ.	1
2015/09/14	Synopsys VCS-AMS Seminar	Univ. of Tokyo	13

2015/09/14	Synopsys VCS-AMS Seminar	Hokkaido Univ.	1
2015/09/14	Synopsys VCS-AMS Seminar	Tohoku Univ.	6
2015/09/14	Synopsys VCS-AMS Seminar	Osaka Univ.	7
2015/09/17-18	Synopsys IC Compiler+Milkyway Seminar	Univ. of Tokyo	28
2015/09/17-20	Synopsys IC Compiler+Milkyway Seminar	Tohoku Univ.	4
2015/09/17-23	Synopsys IC Compiler+Milkyway Seminar	Osaka Univ.	6

2016/03/09	Synopsys StarRCXT Seminar	Univ. of Tokyo	11
2016/03/09	Synopsys StarRCXT Seminar	Hokkaido Univ.	5
2016/03/09	Synopsys StarRCXT Seminar	Tohoku Univ.	3
2016/03/09	Synopsys StarRCXT Seminar	Kyoto Univ.	2
2016/03/09	Synopsys StarRCXT Seminar	Hiroshima Univ.	1
2016/03/10	Synopsys Tetra Max Seminar	Univ. of Tokyo	8
2016/03/10	Synopsys Tetra Max Seminar	Kyoto Univ.	2
2016/03/10	Synopsys Tetra Max Seminar	Hiroshima Univ.	2
2016/03/11	Synopsys Milkyway Seminar	Univ. of Tokyo	10
2016/03/11	Synopsys Milkyway Seminar	Tohoku Univ.	1
2016/03/11	Synopsys Milkyway Seminar	Kyoto Univ.	2
2016/03/11	Synopsys Milkyway Seminar	Osaka Univ.	3
2016/03/11	Synopsys Milkyway Seminar	Hiroshima Univ.	1
2016/03/23	Synopsys Prime Time Seminar	Univ. of Tokyo	4
2016/03/23	Synopsys Prime Time Seminar	Hokkaido Univ.	2
2016/03/23	Synopsys Prime Time Seminar	Tohoku Univ.	1
2016/03/23	Synopsys Prime Time Seminar	Kyoto Univ.	2
2016/03/23	Synopsys Prime Time Seminar	Hiroshima Univ.	2
2016/03/24	Cadence Verilog-A Seminar	Univ. of Tokyo	14
2016/03/24	Cadence Verilog-A Seminar	Tohoku Univ.	6
2016/03/24	Cadence Verilog-A Seminar	Osaka Univ.	7
2016/03/24	Cadence Verilog-A Seminar	Hiroshima Univ.	3
2016/03/24	Cadence Verilog-A Seminar	Miyazaki Univ.	2
2016/03/28	Cadence Stratus Seminar	Univ. of Tokyo	11
2016/03/28	Cadence Stratus Seminar	Hokkaido Univ.	3
2016/03/28	Cadence Stratus Seminar	Tohoku Univ.	1
2016/03/28	Cadence Stratus Seminar	Kyoto Univ.	4
2016/03/28	Cadence Stratus Seminar	Hiroshima Univ.	6
2016/03/15-16	Cadence Skill Language Programming Seminar	Univ. of Tokyo	18
2016/03/15-17	Cadence Skill Language Programming Seminar	Hokkaido Univ.	1
2016/03/15-18	Cadence Skill Language Programming Seminar	Osaka Univ.	5

【Refresh Seminar for Working People】

Teachers of universities and designers in the first line of the enterprise were invited to the lecturer at "VLSI design refresh seminar" was held aiming at the latest, advanced knowledge and technical learning concerning VLSI design as a refreshing education for working people involved in the integrated circuit industry (Table 1. 4. 2). Though this seminar started chiefly in year 1998 under the support of Ministry of Education Technical Education Division to give practicing education of the latest VLSI design technology, it continues under many supports from many societies.

Course A: analog integrated circuit design (6/22 -24), Course M1: MEMS design (6/9-10), Course M2:MEMS fabrication (6/29-7/1), and Course R: RF circuit design (5/21-22). Teachers from industry and universities involved in the integrated circuit research and the education were invited as the lecturer, and they introduced a state-of-the-art VLSI design technology including the practice using a lecture concerning VLSI design and the latest CAD tool. The participants for the course A, M1, M2, R were 15, 12, 8, 13, respectively.

Fig. 1. 4. 1 Refresh Seminar at VDEC seminar room at the University of Tokyo, VDEC.

Table 1. 4. 2 Refresh Seminar

Course A: Analog Circuit Design (3 days)
Analog Circuit Design and simulation Integrated Circuits Verification (LVS, DRC)
Masahiro Sugimoto (Chuo Univ.), Hidetoshi Onodera (Kyoto Univ.), Koji Kotani (Tohoku Univ.)

Course M1: MEMS Design (2 days)
MEMS Basic 1: Fabrication Process MEMS Basic 2: Operation Principle Structual Design Layout Design
Yoshio Mita (Univ. of Tokyo)

Course M2: MEMS Fabrication (3 days)
CAD Design and Analysis Lithography, Etching, Release Vibration measurement and analysis
Yoshio Mita (Univ. of Tokyo)

Course R: CMOS-RF Circuit Design (3days)
Modulation/Demodulation, Cascaded connection Basic Performace, Tranceiver Architecture Circuit Element, Design Flow
Hiroyuki Ito (Tokyo Institute of Technology)

【Designer's forum for young teachers and students】

VDEC LSI designer forum intended for students and young teachers has been held. The VDEC LSI designer forum has aimed to sharing information that cannot be obtained at a society and a academic society, for example, the failure case and the solution in which LSI designer has a hard time, the inside story of CAD industry, the construction method in the design milieu in the laboratory, and so on. This year, we had the meeting in Yamashiro Hot Spring, in August. No less than 48 participants were flourishing at the gathering.

Table 1. 4. 3 Program of Designers Forum in 2015

8/28 (Fri)

Time	
10:30-11:00	Reception
11:00-12:00	Prenary Talk Hiroki Morimura (NTT) Role and Expectation for LSI Technologies in IoT Ara.
12:00-13:00	lunch
13:00-15:00	Ph.D session Strongest Laboratories that I Think
14:30-15:20	VDEC Design Award Finalist Presentation
	break
18:00-20:00	VDEC Design Award award ceremony

8/29 (Sat)

Time	
10:00-12:00	VDEC Design Award Idea Contest Presentation
12:00-12:30	VDEC Design Award Idea Contest award ceremony

1.5 Facilities

The VDEC has provided the big facilities for universities in Japan from its establishment (1996). Big facilities refer to those which are impossible to acquire and or maintain by an individual research unit. Table 1.5.1 shows the available facilities of VLSI testers and some process machines, which are placed at the tester room and the super clean room of the Takeda building. In 2004, the VLSI tester (T2000) and the EB lithography machine (F5112+VD01) were donated to the VDEC by the ADVANTEST. In the year 2012, VDEC joined MEXT (Ministry of Education)'s Nanotechnology platform to enforce its multi-use capability. (For Nanotechnology Platform refer section 1.8). From April 2015 to March 2016, the EB lithography machine F5112 has been used 1406 times. The reason of decrease of number since last year (439 times less from 1845 in 2014) was unexpected trouble of vacuum pump controller that was no more available in a market. However exposure count of the new apparatus (F7000S-VD02) was increased up to 709 times, that is +509 increase from last year (201 exposures in 2014). Total exposure number of EB machines have therefore increased from 2074 (2014) to 2115.

The facilities can be used by user himself, after a couple of times'training by attendance of licensed users; also, by presence of licensed persons, a new user can readily use the machine.

Table1. 5. 1 Available facility list

Facility	Equipment name	Description	Status	Contact
Logic LSI test System	EB tester: IDS10000	The chip surface voltage during operation can be measured with the LST tester. The digital circuit with 384 pins, 1GHz can be tested.	Available	nanotech@ sogo.t.u-tokyo.ac.jp
	LSI tester: ADVANTEST T2000	The digital circuit with 256 pins, 512MHz can be tested. Analog test is optional.	Available	nanotech@ sogo.t.u-tokyo.ac.jp
	Auto prober: PM-90-A	Automated prober for testing LSI wafers, which can be used with the LSI testers. The probe card for LSIs with the VDEC standard pin connections is available.	Available	nanotech@ sogo.t.u-tokyo.ac.jp
Analog/RF measurement system	Analog/RF measurement system: HP4156B, HP4284, etc	DC parameter measurement, Capacitance measurement, Network analyzer, Spectrum analyzer, etc.	Available	nanotech@ sogo.t.u-tokyo.ac.jp
	Low-noize manual prober: Cascade Microtec	6 inch wafer can be measured with six DC probles and two RF probes upto 50 GHz.		
	Low-noize, temperature controlled semi-auto prober: Süss Microtec	8inch wafer can be measured. The chip temperature range is -50 to 200°C.		
Nanotechnology Platform Apparatuses	Mask lithography, Direct lithography: F5112+VD01	Minimum linewidth: 50nm. Lithography for 5 inch photomask (thickness: 2.3 mm), 2-8 inch wafers, and chips is possible.	Available	nanotech@sogo. t.u-tokyo.ac.jp
	Rapid Mask and Direct lithography: F7000S-VD02	Minimum linewidth: 1xnm. Lithography for 5 inch photomask (thickness: 2.3 mm), 2-8 inch wafers, and chips is possible. Stencil character projection of non-square shapes such as circle, triangle is possible.	Available	

	Chlorine ICP plasma etcher CE-S	High density plasma etching with Cl and BCl is possible.	Available	
	Silicon DRIE MUC-21 ASE-Pegasus	High speed, high aspect ratio etching of silicon is possible	Available	
FIB system	FIB: SII XVision200TB	Repairment of photomask, sample etching, etc. (Through Nanotech. Platform and LCNet)	Available	
Chip Bonding System	Wedge Bonder: Westbond 7476D	25 μm ϕ Al or Au wire wedge bonding machine.	Available	
	Epoxy Die Bonder Westbond7200C	Precision Manupilator system. Epoxy and or Ag paste chip bonding and or glued wiring.		
	Semi-Auto Bonder Westbond4700E	18～25 μm ϕ Au Ball bonding or bump creation.		
	Precision Manual Flip-Chip Bonder Finetech Fineplacer Lambda	Face-to-face bonding up to 15mm square chips. Alignment is through video camera. Bonding is by heating chips with TV camera. (Ultrasonic Unit can additionally be purchased.) XY ± 0.5 μm, and θ =1mrad precision.		

1.6 Activity plan for 2015

VDEC will continue activities on chip fabrication services, CAD tool support, dispatching design related information and donated division "D2T", as has been previous years.

【Design related information dispatching/Seminar】

We will continue holding the following seminars: (1) CAD tools seminars which have been continued since 1997, (2) "Refresh seminar" since 1998, (3) "Designer'Forum" since 1997. We will also continue seminars for LSI tester usage at VDEC and sub-centers, workshops on LSI testing technologies initiated by D2T.

【CAD tool support】

We will continue Cadence tools, Synopsys tools and Mentor tools as the main stream design tools. We will continue analog RF design environment, GoldenGate and ADS by Agilent, C-based design environment, BachC by Sharp. In addition, we continue trial of several CAD tools, such as layout platform, Lavis by TOOL. Design debugging platform from SpringSoft has merged into Cadence tools and will be continued. SmartSpice by Silvaco, will be also continued.

【Chip fabrication services】

We will continue chip fabrication services for SOTB 65 nm CMOS by Renesas Electronics, 0.18 μm CMOS by Rohm, FD-SOI 28 nm CMOS by ST Microelectronics through CMP and 0.8 μm CMOS by On-semiconductor-Sanyo as the regular services.

Table 1. 7. 1 Chip fabrication schedule

【CMOS 1.2 μm 2P2M】 On-Semiconductor (Former Motorola Japan)

	Chip application deadline	Design deadline	Chip delivery
2016#1	2016/ 7/ 8	2016/ 9/30	2016/12/23
2016#2	2016/12/30	2017/ 3/24	2016/ 6/20

【CMOS 0.18 μm 1P5M (+MiM)】 Rohm

	Chip application deadline	Design deadline	Chip delivery
2016 #1	2016/ 3/ 7	2016/ 5/30	2016/ 9/16
2016 #2	2016/ 5/ 2	2016/ 7/25	2016/11/11
2016 #3	2016/ 6/28	2016/ 9/20	2016/12/27
2016 #5	2016/11/28	2017/ 2/20	2017/ 6/16

【FD-SOI CMOS 28 nm 1P10M】ST Microelectronics

Based on the chip fabrication schedule through CMP.

【SOTB CMOS 65 nm】 Renesas Electronics

	Chip application deadline	Design deadline	Chip delivery
2016 #1	2016/ 5/23	2016/ 7/4	2016/12/15
2016 #2	2016/12/12	2017/ 1/23	2017/ 7/ 6

1.7 Venture companies related to VDEC

Some professors related to VDEC started venture companies. The following is a list of the venture companies related to VDEC.

[1] AIL Co.,Ltd. (http://www.ailabo.co.jp/)

Related professor : Professor Kazuo Taki, Kobe Univ. (President-Director)

[2] Synthesis Corporation (http://www.synthesis.co.jp/)

Related professor : Professor Emeritus Isao Shirakawa, Osaka Univ. (Director)

Description of business : (1) Hardware/software co-design
(2) System LSI design, design services
(3) Development and sales of IPs
(4) Development of EDA tools

[3] Nanodesign Corporation (http://www.nanodesign.co.jp/)

Related professor :Professor Kazuyuki Nakamura, Kyushu Institute of Technology. (Representative Director)

[4] A-R-Tec Corp. (http://www.a-r-tec.jp/)

Related professor : Professor Emeritus Atsushi Iwata, Hiroshima Univ. (Representative Director)

Description of business : (1) Measurement and analysis of LSI substrate noise
(2) Design of analog-RF mixed signal LSIs
(3) Training of analog design on the JOB method

[5] Ishijima Electronics (http://ishi.main.jp/)

Description of business : (1) Electronic circuit development
(2) Software development
(3) Consulting

1.8 "Nanotechnology Platform": Ultra Small Lithography and Nanometric Observation Site

VDEC is operating an open-use nanotechnology platform "Ultra Small Lithography and Nanometric Observation Site" together with the Institute of Engineering Innovation of Graduate School of Engineering. The site is supported by Japanese Ministry of Education (MEXT)'s Nanotechnology Platform grant. Any researchers in Japanese Universities, Laboratories, and Companies can take full advantage of The University of Tokyo's cutting-edge nanotechnology apparatuses and know-hows. The accessible technology includes Lithography and Etching environment, Ultra High-Voltage Acceleration (1MV) transmission electron microscope (TEM) that is capable of visualizing upto light materials such as Nitrogen. VDEC takes part in the lithography at Takeda Sentanchi Super Cleanroom. Through VDEC's key apparatus F5112+VD01 donated from Advantest Corporation as well as F7000S-VD02 purchased by national budget, VDEC is supporting post-VLSI activities such as MEMS. The machine is capable of rapidly writing patterns on arbitrary-shaped targets sizing from 1cm-sqare chip to 8-inch round wafers. The performance is measured by the number of research reports and machine use. The University of Tokyo site has received 159 research reports including 22 from big companies, 4 from Small and Medium-size Enterprises (SMEs), 29 from other universities, 100 from UTokyo researchers (including external collaboration but excluding VDEC), and 4 from public research institutes. The exposure count was 2115 for 12 months (176.3/month), which is the record since beginning of existing statistics (460 for FY 2000). As shown in the Fig. 1, usage is monotonously increasing. "Open ratio", which is the number of days in which users outside the University of Tokyo came, divided by machine open days, was 99%. Due to the strong support of nanotech. Platform, even a novice user can obtain fine lithography result by using the apparatuses with the Platform engineering staffs of VDEC.

URL:http://nanotechnet.t.u-tokyo.ac.jp/

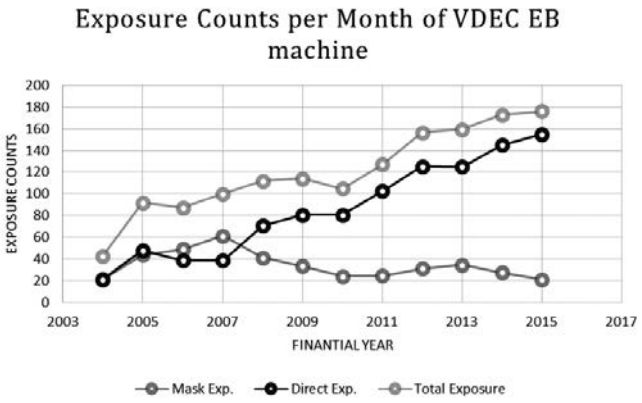


Fig. 1 Monthly Average Exposure Count of EB Machine (s).

2. Activity Report of "ADVANTEST D2T Research Division"

2. 1 Introduction of "ADVANTEST D2T Research Division"

2.1.1 Aim of the establishment of "ADVANTEST D2T Research Division"

ADVANTEST D2T research division was established in VDEC in October 2007. As the name of the research division indicates, it is financially supported by ADVANTEST Corporation.

The aim of establishment of ADVANTEST D2T research division is to promote the research and education environment of VLSI testing in all universities and colleges in Japan. "D2T" means that we consider not only design but also test. As the results of our activities, we hope to provide the experts of design and test for industry. In addition, we are exchanging researchers with other universities or research institute in both Japan and overseas. Moreover, D2T research division is in a good environment to make collaboration with industry because testing of VLSI is one of the most practical research topics in industry. Based on those activities, our final goal is to become a center of excellence of VLSI Testing in Japan.

The first phase and the second phase of D2T activities had finished in September 2010 and September 2013, respectively. We are currently in its third phase that started in October 2013 through the courtesy of ADVANTEST Corporation. We are approaching the last year of the third phase with very fruitful achievements in research, education, symposium organization, and so on. We also invited Professor Mehdi B. Karlsruhe Institute of Technology from August to December 2015, and leveraged research collaborations between KIT and VDEC, other research institutes and companies.

Details of our group's activities are presented in the following sections.

2.1.2 Members of "ADVANTEST D2T Research Division"

Project Professor	Mehdi Baradaran Tahoori (Aug. 2015–Dec. 2015)
Project Lecturer	Rimon Ikeno
Assistant Professor	Nguyen Ngoc Mai Khanh
Researcher	Takahiro Yamaguchi (ADVANTEST Laboratories Ltd.)
Researcher	Masahiro Ishida (ADVANTEST Corporation)
Assistant Clerk	Makiko Okazaki

2. 2. Report of “10th D2T Symposium”

“The 10th D2T Symposium” was held on August 21st, 2015 at Takeda Building with more than 160 participants.

Under its main theme: “Reliability for automotive and other applications”, the symposium had valuable lecturers by distinguished researchers invited from both overseas and domestic institutes, latest achievement reports by VDEC researchers, and a panel discussion by the lecturers and guest panelists.

The invited lecturers were Takashi Setoya from Toshiba Corporation, Professor Subhasish Mitra from Stanford University, Professor Mehdi B. Tahoori from Karlsruhe Institute of Technology and The University of Tokyo, and Professor Tibor Grasser from TU Wien. At the panel discussion whose theme was “Reliability / dependability of industrial standards for automotive systems”, we invited two guest panelists, Professor Tomohiro Yoneda from National Institute for Informatics and Takao Futagami from Toyo Corporation, in addition to the invited lecturers. Highly-reliable electronics systems for automotive applications and its standardization were discussed lively. We sincerely appreciate every participant for their contribution at the symposium.

9th D2T Symposium Program

10:00	**Opening Remarks** Kunihiro Asada (Director, VDEC, The University of Tokyo) Shinichiro Kuroe (President and CEO, ADVANTEST Corporation)
10:15	**Session 1** (Chairman: Toru Nakura, The University of Tokyo) *"High reliability and process control technique of LSI for Automotive product"* [Invited] Takashi Setoya (Toshiba Corporation, JEITA) *"Cross-layer Resilient Design for Automotive Electronics"* [Invited] Mehdi B. Tahoori (Karlsruhe Institute of Technology)
11:45	**Lunch**
13:00	**Session 2** (Chairman: Shinichi Takagi, The University of Tokyo) *"Robust Systems: Overcoming Complexity and Reliability Challenges"* [Invited] Subhasish Mitra (Stanford University) *"Advanced Modeling and Characterization of Bias Temperature Instabilities and Hot Carrier Degradation"* [Invited] Tibor Grasser (TU Wien)
14:30	**Coffee Break**
15:00	**Session 3** (Chairman: Makoto Ikeda, The University of Tokyo) *"Activities of VDEC Advantest D2T Research Division"* Rimon Ikeno (The University of Tokyo) *"FET-R-C Circuits: A Unified Treatment"* Tetsuya Iizuka (The University of Tokyo) *"A Novel Circuit for Transition-Edge Detection"* Takahiro Yamaguchi (ADVANTEST Laboratories) *"Dynamic Power Integrity Control of ATE for Eliminating Overkills and Underkills"* Masahiro Ishida (ADVANTEST Corporation)
16:25	**Break**
16:40	**Panel Discussion** Theme: *"Reliability / dependability of industrial standards for automotive systems"* Moderator: Masahiro Fujita (VDEC, The University of Tokyo) Panelists: Tomohiro Yoneda (National Institute for Informatics) Takao Futagami (Toyo Corporation / SESSAME) Mehdi B. Tahoori (Karlsruhe Institute of Technology) Subhasish Mitra (Stanford University)
18:00	**Closing**
18:15	**Reception**

2. 3. Research Activity Reports of "ADVANTEST D2T Research Division"

On-chip Stochastic Data Converter/On-chip Spectrum Analyzer

Takahiro Yamaguchi, Nguyen Ngoc Mai Khanh,
Rimon Ikeno, Kunihiro Asada

In the research toward on-chip digitizer systems utilizing stochastic comparator groups, comparator circuit and its measurement methodology are studied.

We progressed theoretical study of the stochastic comparators based on the measurement data of comparator groups that had been designed by Dr. James S. Tandon in 65 nm CMOS technology with single-ended circuitry.

We are also pursuing a differential comparators for better noise immunity and improved symmetry in the offset variation. Test chips in 180 nm CMOS and 65 nm SOTB CMOS processes were designed. DC measurement methodology for such differential-signal circuits were investigated to realize low-noise and high-resolution measurement.

Power Integrity Evaluation Method

Masahiro Ishida, Naoki Terao, Toru Nakura,
Rimon Ikeno, Kunihiro Asada

While a required power supply voltage has become lower due to the advanced miniaturization of the semiconductor process, the power supply current consumed by a semiconductor device has increased because of the huge number of transistors integrated on a single chip. It may increase the power supply noise, and power integrity issues of the device under test in both an ATE and a practical operating environments.

The purposes of this research project are to develop a method for evaluating power integrity at on-chip power supply nodes in semiconductor devices (power delivery network modeling method) and a new power integrity control method which is more suitable for the ATE than our conventional method.

This year, for the power delivery network modeling, we have investigated an algorithm for calculating a simple circuit model of the on-chip power delivery network based on measurements of currents supplied from power supplies to the device, and evaluated its feasibility by using an actual laid out power delivery network with computer simulations. Furthermore, for the power integrity control method, we have developed a new method which can emulate any power supply characteristics based on the feedback control and demonstrated the concept and feasibility of the proposed method by experiments using actual hardware including FPGA.

High-throughput and high-accuracy electron-beam direct writing (EBDW) strategy for wide range of EBDW applications

Rimon Ikeno, Satoshi Maruyama, Yoshio Mita,
Makoto Ikeda, Kunihiro Asada

Maskless lithography by Electron-Beam Direct Writing (EBDW) lithography is expected as a low-cost and short turn-around time (TAT) lithography technology, but it also has some drawbacks like low process throughput and low accuracy against the intended layout shapes. We are pursuing high-speed and high-accuracy EBDW strategy utilizing Character Projection (CP) method to overcome these concerns and to boost EBDW use in arbitrary fields like MEMS, photonics, and so on.

This year, we applied our layout-data conversion methodology for high-accuracy CP exposure of arcs and oblique edges to our lithography experiments of the practical device structures like light wave guides. We introduced a high-resolution EB resist material, and established a total process and observation flow to see the relationship between the data-conversion parameters and the resultant device quality like line edge roughness (LER).

2. 4. Publications

Journal papers

[1] Masahiro Ishida, Toru Nakura, Takashi Kusaka, Satoshi Komatsu, and Kunihiro Asada, "Dynamic Power Integrity Control of ATE for Eliminating Overkills and Underkills in Device Testing," to be published on *Journal of Electronic Testing: Theory and Applications*, 2016.

International Conferences, Symposiums, Workshops

[1] Takahiro J. Yamaguchi, Katsuhiko Degawa, Masayuki Kawabata, Masahiro Ishida, Kouichiro Uekusa, and Mani Soma, "A new method for measuring alias-free aperture jitter in an ADC output," in *Proceedings of IEEE International Test Conference*, Anaheim, CA, October 6-8, 2015.

[2] Masahiro Ishida, Toru Nakura, Akira Matsukawa, Rimon Ikeno, and Kunihiro Asada, "A Technique for Analyzing On-chip Power Supply Impedance," *Asian Test Symposium (ATS) 2015*, 6B-1, November 2015.

[3] Rimon Ikeno, Satoshi Maruyama, Yoshio Mita, Makoto Ikeda, and Kunihiro Asada, "Electron beam lithography with character projection exposure for throughput enhancement with line-edge quality optimization," *Proceedings of SPIE 9781, Design-Process-Technology Co-optimization for Manufacturability X*, 978110, March 2016.

[4] Md. Maruf Hossain, Tetsuya Iizuka, Toru Nakura and Kunihiro Asada, "Analytical design optimization of sub-ranging ADC based on stochastic comparator," 5.7.3, *Design, Automation and Test in Europe (DATE) 2016*, March 2016.

Domestic Conferences, Workshops, etc.

[1] Rimon Ikeno, "Advanced electron beam direct writing technique for arbitrary layout figures using the latest EB lithography apparatus in VDEC," *Joint Workshop of Nanofabrication and Advanced Characterization Platforms in The University of Tokyo, Nanotechnology Platforms of the Ministry of Education, Culture, Sports, Science and Technology (MEXT)*, Japan, Nov. 2015.

Patent

[1] Masahiro Ishida, Takashi Kusaka, Rimon Ikeno, Kunihiro Asada, Toru Nakura, and Naoki Terao, "Apparatus and method to emulate impedance characteristics of power supply network," Patent application (Japan) 2016-014282, Jan. 28th, 2016.

Chapter 3 Research in VDEC

Asada, Nakura and Iizuka Laboratory

(http://www.mos.t.u-tokyo.ac.jp)

Supply Fluctuation Monitoring, Analysis and Reduction Method

Kunihiro Asada, Toru Nakura, Tetsuya Iizuka, Masahiro Kano, Satoshi Matsukawa, Naoki Terao

As miniaturization of semiconductor process increases, power supply voltage fluctuation due to its parasitic impedance has become serious concern.

Passive decap is one of the most popular method used for supply noise reduction, however, this requires large silicon area for large capacitance. Then, we focused on the active charge injection method in order to realize both noise reduction and silicon area reduction. Previous works of this method did not mention the amount of charge injected into supply line, therefore we analyzed this method under certain assumptions and designed the circuits (voltage drop detector, injection controller circuit and canceling capacitor circuit) to realize the analyzed charge injection. We simulated these circuits with post-layout parasitic wire capacitance and realized about 30% noise reduction and about 70% area reduction.

Also, the parasitic impedance on supply line and power supply voltage fluctuation do not affect only the inside of LSI chip.Generally, LSI undergoes test after manifuctured to see if it will work normally. However, impedance mismatch between ATE and customer environment will degrade reliability of the test.

We proposed and designed power supply system for ATE which has an ability to adjust its impedance to any one by using feedback system with compensation current source, so it can emulate customer environment. We are currently successfull of changing impedance using compensation current but voltage fluctuation waveform is still not exactly the same as expected, so more adjustment will be needed.

PLL circuit with Time-Domain control

Kunihiro Asada, Toru Nakura, Tetsuya Iizuka, Toshiyuki Kikkawa, Takashi Toi, and Meikan Chin.

In this research, we have applied time-domain control methods to PLL circuit and its measurement. A Pulse-Width Controlled PLL (PWPLL) is a new type of PLL whose oscillator is controlled by a pulse width. The PWPLL is implementable in a very small area, on the one hand, its operating conditions are sensitive to the several variations. For example, a lock range of the PWPLL tends to be narrower than that of other PLLs.

Therefore, we proposed two methods to improve a tolerance of the PWPLL especially against process-variations. As the first method, we employed a variable-length ring oscillator where the number of the ring stages is controllable. Also, we tried to control the load-capacitance of the oscillator. We fabricated two prototype chips and their measurement results show an enhancement of the lock range and reduction of the rms jitter.

We also demonstrated a PWPLL compiler which generates GDS data from performance specification. The inputs of the compiler are standard cell libraries, SPICE parameters and the target specification file including the output frequency, the division ratio and the Process, Voltage, and Temperature (PVT) corner conditions. The PLL compiler calculates rough values of the design parameters, runs SPICE simulations, analyses the waveform files to adjust the design parameters, considering the variation of the PLL characteristics with the given PVT variation. When the waveform satisfies the specification, the compiler generates a verilog netlist and a GDS is designed by the netlist.

Furthermore, we proposed a measurement method of PLL frequency characteristics not through analog measurement but through digital interface in order to reduce the test cost. The proposed method utilizes Digital-to-Time Converter (DTC) as an integrated stimulus generator, and Time-to-Digital Converter (TDC) as an integrated response analyzer. Since both the DTC and the TDC are composed of the same delay cells in our proposed method, the measurement result is robust against the PVT variations. The robustness of our proposed method is demonstrated by HSPICE sim-

ulations. We also worked on a PLL bandwidth control as an application of the proposed measurement method.

Time Domain CDR and TDC Designs

Kunihiro Asada, Toru Nakura, Tetsuya Iizuka, Norihito Tohge, Takehisa Koga, Tomohiko Yano

While digital circuits directly benefit by advanced process technologies, analog circuits suffer from negative effects such as small voltage headroom. Time-mode circuits, where analog signals are represented by digital signal edge transitions, could be a solution of analog circuits in a nanometer process. In this research, time-mode analog signal accumulator is proposed as a fundamental building block of analog circuits. The proposed accumulator holds the time variable by the time interval of two pulses which propagate on a single delay-line ring consisting of gated inverters, eliminating drift error due to the delay mismatch between the two pulses.

In addition to that circuit, time-to-digital circuit (TDC) is known as one of representative time domain circuits. TDC converts a time difference between two signals into a digital code by using delay elements. We dealt with an issue of conventional pulse-shrinking TDC, one of the architectures of TDCs, which is a tradeoff between linearity of the conversion and the performances of sampling rate, power consumption, and jitter. We designed new scheme so as to solve that problem, and validated the performances of higher sampling frequency, lower power consumption, and more precise single shot than conventional ones.

TDC can be applied for various applications, for example the following research. In the realm of serial communication systems, it has been emphasized to increase data rate or power consumption per bit, however, total amount of power consumption include both in stand-by state and in operational state. However, especially for optimizing energy consumption of serial communication systems which operate only intermittently, it is important that not only increasing power consumption rate in their operational state but also minimizing power consumption of stand-by state and maximizing the period of stand-by state by launching quickly. A Clock-and-Data Recovery Circuit which is based on Cycle Lock Gated Oscillator has been proposed to realize that. However, frequency mismatch resulted from its feed-forward architecture and quantization noise of the oscillator has been a big issue. We resolved the problem by introducing a feed-back architecture with a digital controller and Fractional Delay Control Scheme.

Radiation Detector Utilizing Semiconductor Photodiode

Kunihiro Asada, Toru Nakura, Tetsuya Iizuka, Yang Xiao, Kai Xu

Scintillation detectors and semiconductor detectors have received wide spread attention since they can specify the nuclide of radiation and estimate the arrival angle. Former research proposed a detector using the cube scintillator, SPAD (Single Photon Avalanche Diode) array image sensors, multi-coated materials, and pinholes and verified the technique to detect the locus of the lighting electron by this detector. However the detect and estimate costs plenty of time. This research proposed a technique to detect the location of the electron emitting light in high speed utilizing the periodicity of the arrangement of the pinholes and SPADS. The result of the simulation verified that by using this technique the location of the electron emitting light in a scintillator could be detected with a spatial resolution of 20 um within 20-40 seconds. About the structures of SPADs we have tested, the p-well/deep-n-well with poly gate SPAD shows the lowest DCR. A 31x31 SPAD sensor featuring breakdown pixels extraction architecture for efficient data readout has been fabricated, and it's ability of capturing a short laser pulse (40 ns) has been proved by measurements.

Surface magnetic field modeling for LSI security

Kunihiro Asada, Toru Nakura, Tetsuya Iizuka, Yuki Oda, Tomohiro Hirata

The test of modern circuit is becoming more difficult because its structure is getting smaller and more complex. Fast, cost-effective and accurate test method is highly in demand. Magnetic probe testing method is focused in this paper.

Magnetic emission of circuit board is measured by probe, and current distribution is estimated with obtained magnetic field map. Estimated current distribution can be used for non-destructive circuit test method. The accuracy of current estimation is evaluated by calculating thermal noise of probe and condition number of trans-impedance matrix. We validated this

method by using electromagnetic field simulation.

CMOS Based Sub-Millimeter Sensing System Using Time-Domain Spectroscopy Technique

Kunihiro Asada, Tetsuya Iizuka, Nguyen Ngoc Mai-Khanh, Parit Kanjanavirojkul,Yudai Suzuki, Mitsuki Nakamura,and Taiki Sugiyama

The target of this research is to implement sub-millimeter wave (THz) transceivers for sensing applications, based on time-domain spectroscopy (TDS) technique. A wideband pulse generator realized by CMOS integrated on glass substrate is proposed. The pulse generator features zero stand-by power, quick starting time, high efficiency. In addition, it is suitable for high frequency generation, and not limited by CMOS Fmax.

On the receiver side, sampling-based pulse receiver is studied. Equivalent sampling, detection method of Time Domain Spectroscopy(TDS), is used for this receiver to detect and obtain waveform of received pulse. The sampling-based detector switches matching and mismatching states between antenna and mixer impedance with NMOS (used as a Voltage Controlled Resistor) and sampling pulse (inputted to NMOS'gate).

Array antenna for the system is also studied. Even though, on-chip millimeter-wave band array antenna has been developed in recent years, it is difficult to realize sharp directivities because of the timing constraints and limited aperture length. The method proposed and evaluated, can estimate the position and reflection intensity of every look angle using set of receiving electric field when sending pulses with unsharp directivities.

For future applications, transmission properties of THz through material are also examined. Fundamental property of terahertz time domain spectrometer was measured, and after that, measuring terahertz absorption property of submillimeter wave filter was attempted. As a result, it became clear that terahertz time domain spectrometer can be used to measure terahertz absorption property of submillimeter wave filter.

VLSI Reliability Improvement in nano-meter process technologies

Kunihiro Asada, Toru Nakura, Tetsuya Iizuka, and Kazunori Mori

Recent process miniaturization causes reliability problems such as NBTI degradation on digital circuit. For designing circuit of avoiding NBTI, we need accurate and fast simulation of NBTI. Thus, we propose an accurate simulation method with calculation of potential NBTI. In this study, we record the states of potential NBTI by calculation of NBTI phenomena.

In addition, for quick variation of NBTI on circuit operation, the proposed method can realize high-speed calculation by high accuracy approximate based on frequency dependence of NBTI.

High-performance A-D Converters

Kunihiro Asada, Toru Nakura, Tetsuya Iizuka, Maruf Hossain, Takaaki Ito, Ryosuke Saito

A performance model for Analog to Digital Converter (ADC) based on stochastic comparator has been proposed by analyzing the random variation in comparator offset voltage. Probability Density Function (PDF) has been formulated to establish the relation among different design parameters and the resolution of a stochastic comparator. This PDF is used to calculate the yield of the ADC and the correlation among the analog steps of the ADC output code is ignored for simplicity. The validity of our model is then verified by performing Monte Carlo simulation and it is shown that the model is precise for a practical value of yield > 0.8. This model is then applied to a sub-ranging ADC based on stochastic comparator to find out the optimal resource distribution between the conventional deterministic architecture and the novel stochastic approach.

Sample and Hold Circuit used in an ADC generates nonlinear distortion, and it worsens ADC's accuracy. Distortion analysis has already been conducted, and it is known that distortion can be controlled by changing Sample and Hold Circuit parameters. To verify the accuracy of distortion analysis, we want to design a Sample and Hold Circuit and measure its distortion. Recently, we checked by simulation that it is possible to measure the distortion and designed the distortion measurement chip.

Fujita Laboratory

(http://www.cad.t.u-tokyo.ac.jp/)

Efficient Topological Matching Among Multiple Circuits

Masahiro FUJITA, Amir Masoud GHAREHBAGHI, Hossein IZADI RAD

Recognizing similarities and differences among multiple circuits is very useful for managing and maintaining IP libraries as well as merging circuits, fraud detection, reverse engineering, and redundancy checking. In this work, we address the problem of finding the maximum common subcircuit among two or more logic circuits. Given the gate-level netlists of the circuits, first we represent the circuits as graphs. Then, we try to find the largest common subgraph with a new approach based on signature generation and matching. We have defined a signature based on topology of the fanin cones of the circuit elements. Given two circuits, first we find all the circuit elements with unique signature between the two input circuits. After that, we try to expand the matching area by our expansion rules as much as possible. We iteratively find the unique matches and expand the matching area until no further matching is possible. Our experiments on IWLS2005

benchmark suite show that our method is able to find the perfect matching between two 160,000-gate IP in 5 minutes. In addition, our method is more than two order of magnitude faster than our previous graph-matching based method, while the size of the matched area is comparable or larger.

Acceleration of Calculation with FPGA

Masahiro FUJITA, Amir Masoud GHAREHBAGHI, Taro KAWAO

Dedicated hardware is generally faster and more energy-efficient than a general hardware. A circuit optimized for specific calculation can be obtained without chip fabrication using a Field Programmable Gate Array (FPGA), which is a programmable circuit. In this work, we have considered acceleration of simulation of neural network and analysis of electromagnetic field.

Neural network is a mathematical model of the mechanism of a brain. We implemented a highly pipelined circuit on a FPGA to simulate the network composed of 1024 spiking neurons and we could accelerate the simulation by 47x compared to real time calculation on a general purpose processor. This circuit is designed to be scalable to the number of neurons. In the future work, we will use multi-FPGA network to simulate tens of thousands of neurons.

Continuous miniaturization and performance improvement of electronic equipment causes more serious electromagnetic interference problems than before. Insufficient performance of current simulators lead to depending on real testing equipment with higher cost. To tackle this problem, we have implemented a fast simulator using FPGA for 2D and 3D simulation. The original program can simulate around 100 MCell/Sec. The multi-core version of the program can run up to 2 times faster than the single-core version. Our FPGA implementation runs more than 5 times faster than the multi-core version of the program (1130 MCell/Sec)

High-Level ECO Through Mapping with Gate-Level Design

Masahiro FUJITA, Amir Masoud GHAREHBAGHI, Qinhao WANG

In the hardware design flow, there are often the situations that the bugs or the specification need to be changed quite late in the design flow. Designers do not want re-run the whole design flow from beginning since the cost and time-consuming. Engineering Change Order (ECO) may happen in a design due to a bug fix or a change in the original specification. ECO is expected to be a small change.

High-level design methodology is used for implementing new algorithms since it can increase the design abstraction and reduce the time to market. However, little change from high-level description will have a great impact on circuit structure after high-level synthesis. In this work, we proposed a method for high level ECO. First, the original topological (part of data flow graph) is fixed, and then we replace partial operations (nodes of DFG) by programmable datapath. This transform the ECO to an equivalent problem, and then get the solution by SMT solver automatically. We also extend the problem to the situation when the design specification is not given. Experimental results show that this method can solve several practical examples of high-level ECO.

Debugging Electrical Bugs using Trace Buffers

Masahiro FUJITA, Amir Masoud GHAREHBAGHI, Kentarou IWATA

As VLSI becomes denser and place and route stage becomes more difficult, more electrical bugs can occur, which are caused by thermal change, drop in supply voltage or crosstalk. It is difficult to reproduce because these bugs occur randomly. So debugging is time-consuming. Therefore, we use trace buffers as on-chip memory to record partial values of flip-flops repeatedly. Furthermore, past state values are restored from those values in order to find a location of electrical bugs. A major problem is to identify whether recorded values are correct or not because the location and time of occurrence of electrical bugs are unknown.

HW/SW Co-Verification of embedded system

Masahiro FUJITA, Yusuke KIMURA

As embedded software becomes more complex nowadays, verification technique for its verification becomes more important. Interruption service routine (ISR) is one of the characteristic functions of embedded system, and we focused on verification method considering ISR in this topic. We suggested to use constraints generated from real system's in-out data for verification in order to reduce the number of execution paths that are used for test. We additionally implemented the variable dependencies solving method and the number of execution paths for testing becomes less than last year's. We successfully verified an industrial example in reasonable time.

SW Synthesis

Masahiro FUJITA, Yusuke KIMURA, Kuntarou ISHIYAMA

In order to debug the software efficiently, we researched about the software synthesis method using small number of input-output patterns. Without specifying whole input-output patterns, the tool can generate the program by asking appropriate outputs for some inputs. This technique can apply for the debugging when error localization is finished and for the synthesis for the place where it is difficult for human to write code manually, for example bit calculation.

Reverse Engineering of gate level circuit

Masahiro FUJITA, Yusuke KIMURA

This research topic's aim is to suggest the correspondence between high-level description and synthesized gate-level description. Gate-level circuits usually have state machines, and it is one of the causes of difficulty in analyzing the correspondence. We suggested the tentative method for extracting flip-flops related to state machine from gate level circuit. By analyzing the state transition of the flip-flops, we can get the correspondence between the state of high-level description and of gate-level circuit.

Takamiya Laboratory

(http://icdesign.iis.u-tokyo.ac.jp/)

Integrated Power Management Circuits and Systems towards Energy Autonomous Electronic Devices

Makoto Takamiya and Takayasu Sakurai

Requirements for IoT sensor nodes, wearable healthcare devices, and implanted medical devices are the wearing-unconsciousness and the maintenance-free operation. To enable the wearing-unconsciousness, mechanically flexible or small-size devices with the wireless connection are required. To enable the maintenance-free operation, energy autonomous devices are required. The energy autonomy is achieved by both the energy efficient operation and the energy harvesting.

Large Area and Flexible Electronics with Organic Transistors

Makoto Takamiya, Takao Someya, and Takayasu Sakurai

Large area electronics is a new frontier in electronics where intelligent electronic devices are distributed on a flexible surface, 10 cm to 10 m on a side, for the human interface and the comfortable daily life. Flexible and low-cost organic FETs (OFETs) are suitable for large-area electronics and have great potential as a supplement of solid and expensive silicon MOSFETs for VLSI's. We have proposed and demonstrated several large area and flexible applications including a surface electromyogram measurement sheet for prosthetic hand control, a flexible wet sensor sheet for biomedical applications, and a fever alarm armband.

Ikeda Laboratory

(http://www.mos.t.u-tokyo.ac.jp)

Current Research Projects

High-performance Cryptographic Engine Design

M. Ikeda, M. Tamura, T.Ikeda

We have studied about the implementation of cryptographic engines. We implemented elliptic curve digital signature algorithm (ECDSA) using 65 nm SOTB CMOS. We have proposed pipelined high radix Montgomery multiplier for critical path delay minimization. We realized 1.6x throughput than the conventional Montgomery multiplier and minimize signature generation time for ECDSA. Measurement results shows signature generation time and energy consumption of 330 us and 13.9 uJ, respectively at the nominal power supply of 1.1V, and those of 2.3 ms and 1.68uJ, respectively at energy minimum operating condition of power supply voltage of 0.3V. The area of this circuit is 1.92 mm^2. We also implemented 1024 bit RSA cryptographic engine showing area-delay tradeoffs for radix 2 to 1024 of Montgomery multiplier. The results of logic synthesis with 65 nm SOTB CMOS library shows the fastest 1024 bit RSA encryption of 81 us by using 1024 bit multipliers.

SEU resistivity of Self-Synchronous System based on Dynamic Circuits

M. Ikeda, D. Sai

Self-Synchronous Controlling by hand-shaking based on gate-level completion detection is regarded as reliable controlling mechanism under large process variation and large power supply bounce, especially for lower voltage operations. Dynamic circuits are, however, assumed to be vulnerable against SEU by neutron injection for the advanced process with lower operating voltage. In this study, we have studied SEU probability estimation method by injecting charges into nodes for standard cells comprising the self-synchronous basic cells. SEU probability estimation is carried out by charge injection timing, time domain probability, and simplified area estimation, special domain probability, for circuits nodes. We extracted the most SEU tolerant cell by exhaustive calculation of SEU error probabilities for possible netlist of a function, and possible transistor placements.

Digital control for an Electrostatic Micro Actuator with CMOS circuit

M. Ikeda, S. Maruyama

Control of MEMS devices are usually done by analog domain, however, in this study, we tried to study digital domain control of MEMS devices. We applied PWM control pulses to micro-actuator with electro-static control with higher frequency than the electro-mechanical resonance of the actuator, and at the same time, we carried out measurement of MEMS displacement by capacitance measurement. With this scheme, we evaluated control of delta-sigma modulator for the electrostatic micro actuator in the digital domain.

3D-range finding by Smart Image Sensors

M. Ikeda, U. Kim, D. Uehara, J. Imabayashi, M. Tanibuchi

We have studied smart image sensors for 3-D range-finding with back-ground illumination rejection capability by utilizing modulated light projection. Common-mode rejection circuit is introduced to lock-in type pixel to enhance back-ground illumination rejection. In addition, we have studied faster range-finding technique by utilizing de Bruijn sequence.

Mita Laboratory

(http://www.if.t.u-tokyo.ac.jp)

Study on LSI-MEMS integrated pond-skating robot for energy-autonomous distributed microsystems

Y. Mita, I. Mori, Y. Okamoto Y. Li, S. Smith, A.J. Walton (Univ. of Edinburgh)

As one example of integrated MEMS that is expected to open new research and industrial application fields, the authors are trying to show a top-down application of energy-autonomous distributed microrobots. The research belongs to the "top-down" research category and through the research the team looks forward to provide the "Engineered Nature"; the team does not intend to just copy how nature works in implementation level, but to realize with cutting-edge technologies what nature is aiming at in highly-functional level. Recent top-down activities include autonomous distributed mobile robot: "Pond Skater", which to date had not been realized by any other microsystems group. The

availability of a leading low voltage technology at the Scottish Microelectronic Centre (SMC) the University of Edinburgh that could electrically change surfaces from hydrophobic to hydrophilic proved to be crucial to achieving this goal as was the previous involvement of SMC staff in wireless technology. The major challenge is propulsion, and it is clear that directly mimicking the pond skating insect's propulsion mechanism would be problematic. The idea that was developed was to propel the device using Electro-Wetting Of Dielectric (EWOD) to move air bubbles, which had the significant advantage that there we no moving mechanical parts, which simplified the construction and helped to minimize the weight which was important if the pondskating device was to float using surface tension. Based on the world's first wireless pond-skating propulsion, the team is developing VLSI control circuit and integration technology for continuous skating. In FY2015, CMOS-Post-processed HV generating photovoltaic process has become so reliable that top-down applications can rely on it. As one practical advantage, wavelength modulation control scheme has been experimentally verified; by sending lights of two different wavelength, the device can intentionally charge and discharge MEMS devices with sufficiently short time. High frequency (around resonant frequency) has become possible.

Smart BlocksII Project–A higher alignment accuracy MEMS air-flow actuator local fluidics optimization

Y. Mita, K. Kawahara, and Y. Okamoto

The PI has received a French National Research Center (ANR) grant on behalf of host professor of CNRS laboratory in the Institute of Industrial Science (LIMMS, CNRS-IIS, UMI 2820), together with FEMTO-ST Laboratory. The objective is "an actuator system that can auto-reconfigure as well as make conveyance function". In the last year, a microactuator system with higher alignment accuracy was developed. Past devices have suffered from turbulence of ejected air, yielding relatively low alignment accuracy. By carefully designing local air fluidics, we have demonstrated highly accurate conveyance of micro objects, both experimentally and in FEM simulation.

Top-down fabrication of small-gap electrode devices by Fine E-Beam writing and MEMS process

Y. Mita, Y.Takeshiro, N. Washizu, A. Takada,
M. Fujiwara, T. Sawamura, R. Ikeno, and K. Asada

Towards the goal of production of brand-new sensor devices with higher sensitivity and functionality, the team is working on small-gap electrode fabrication process. The team takes full advantage of newly-acquired (2013) rapid electron beam writer F7000S-VD02. The capability of high electron dose and sharp edge due to cell (character) projection machine configuration is used for fabrication process. The target of first year is reliable sub 100 nm gap electrode fabrication, as well as microactuator-integrated nanogap system.

University-Industry collaborative research on highly-functional system by MEMS post-process of CMOS-VLSI

Y. Mita, R. Sekiguchi (Canon Research Laboratory),
Y. Nakayama (Konica Minolta)

The research targets are new sensor devices, made by post-process at clearnrooms such as VDEC Takeda Supercleanroom and others, of VLSI wafer made through VDEC. The important finding has been that VLSI wafer acquired just after transistor fabrication could sustain processes even with heat treatment, such as deposition, ion implantation, and drive-in. In 2015, an integrated Teraherz wave receiver has been fabricated and successfully demonstrated. Also, a VLSI devices made on Silicon-on-Insulator (SOI) wafer was successfully Deep-RIE processed. The industrial interest is its versatility–many different types of application devices, which differ one from another according to request of market, can be fabricated by using the same technology. More and more companies are interested in the scheme and are working on the technology on the collaborative research project.

An LSI probing system with CMOS-MEMS

Y. Mita, R. Setoguchi and Y. Okamoto

The team is developing a "MEMS" probe card for electron device testing such as VLSI. The originality is to integrate CMOS circuit to provide high functionality. In the year 2014, a piezo-resistive stress measurement circuit was developed to quantify real stress put on the probe. A company-made polysilicon resistor, made

by post-processing commercial CMOS 0.6 μm 1P2M circuit, was integrated into cantilever and responded to the stress with good gauge factor (around 20). The technology has been standardized and could be applied to other groups'research work. Also, to have reliable microprocess, a test structure to visualize end-point of Deep-RIE process is developed.

Right-Brain-Computing Integrated Circuits: Associative Processing Systems

B. Ka, N. Yamashita, Y. Mita

Digital computers are dedicated machines for vary fast execution of numerical calculations. However, their performance is extremely poor in such tasks like seeing, recognizing, and taking immediate actions, which are effortless tasks in our daily life. This research aims at building intelligent VLSI systems based on the psychological model of a brain. In our system past experience is stored as template vectors in non-volatile vast memories and the maximum-likelihood event to the current event is recalled in real time by a fully parallel processing. The key ingredient of the system is a new functional device called "Neuron MOS Transistor" (neuMOS or *v*MOS) which mimics the action of a nerve cell neuron at a single transistor level. Based on such architecture that "association" is the very computing primitive, we are pursuing human-like intelligence system implementation directly in silicon integrated circuits. Currently research is in progress for robust image recognition and classification processing including robust feature extraction. The sate-of-the-art silicon technology has been utilized to implement such associative processors in both analog and digital CMOS VLSI chips, and was published.

Micro Wireless Resonant Power Transfer that Enables Metabolism of Fragile MEMS Actuator.

Y. Mita, N. Sakamoto, B. Stefenelli, A. Kaiser (ISEN/IEMN-CNRS)

The most severe problem of MEMS in which microactuators are exposed to the external world, such as SmartBlocksII demonstrators, is that fragile microactuators are little by little broken during usage, and finally the entire system become unusable. The team proposes a "Metabolism MEMS" concept–the system is composed with detachable two parts: One is fragile MEMS and the other is robust VLSI. The fragile MEMS are replaceable so that the system can have always a "fresh" surface. The key enabling technology is wireless energy and command transfer, with on electrical wiring in between. For that purpose the team tries to use resonance power transfer method in the submillimeter-scale, 1 GHz-range carrier. By Phenitec Semiconductor VDEC run LC oscillator was fabricated. Magnetic power coupling experiments were successful in between the LSI and power receiver with ciliary motion MEMS actuator. The method was experimentally applied to both "voltage driven (=electrostatic)" and "current driven" microactuators; the same circuit could drive both types of microactuators.

"Zeolite-Electronics-Nanostructure (ZEN)" integrated chemical sensor

Y. Mita, S. Inoue, M. Denoual (ENSI de Caen, France), Tixier Mita Agnès, Eric Lebrasseur, Hussein Awala (ENSI de Caen, France), Julien Grand (ENSI de Caen, France), Sveltana Mintova (ENSI de Caen, France)

One of the most important application field of MEMS is sensors that can detect physical and chemical amount that cannot be sensed by human beings. Following a long history of the group's research, the team was appointed in 2015 as a JSPS-CNRS bilateral cooperative research project grant. The goal of the research is to develop a chemical sensor by integrating Zeolite material that is new to VLSI, and applying post-process on it. Within one year, the team already have successfully demonstrated two types of devices: a zeolite chemical sensor by resonant frequency shift detection, and by thermal capacity change detection according chemical concentration.

Takagi-Takenaka Laboratory

(http://www.mosfet.k.u-tokyo.ac.jp/)

III-V/Ge Metal-Oxide-Semiconductor (MOS) FETs

S. Takagi, M. Takenaka, Cai Weili, Yu Xiao, WuKang Kim, Chang Chih-Yu, Ke Mengan, Liao Chenyu, Aya Shimada

We have conducted the research on high-peformance III-V/Ge MOSFETs.

We have investigated InGaAs gate stack technologies by using La_2O_3/InGaAs MOS interfaces. We have shown that La_2O_3 deposted by ALD enable superior

MOS interfaces for InGaAs. We have also fabricated extremeley-thin body Ge-on-Insulator MOSFETs by using wafer-bonded GeOI wafers. We have revealed the physical mechanism which degrades hole mobility in the ultra-thin Ge channel.

Tunnel FET

S. Takagi, M. Takenaka, Min-Soo Kim, Takahiro Gotow, Daehwan An, Takumi Kato, Yoon Sanghee

We have investigated tunnel FETs (TFETs) which can exhibit steep subthreshold slope for low-power operation. Lateral InGaAs TFETs and GaAsSb/InGaAs hetro-junction TFETs have been explored. By growing GaAsSb/InGaAs hetrostructure by MBE, we have demonstrated vertical GaAsSb/InGaAs TFETs. We have also investigated Ge/s-Si TFET for high Ion operation.

Si CMOS photonics

M. Takenaka, S. Takagi, Y. Kim, J. Han, J. Kang, K. Takeuchi

We have proposed Ge CMOS photonics platform by using wafer-bonded GeOI wafers on which Ge CMOS and Ge photonic-wire devices are monolithically integrated. We have successfully demonstrated Ge photonic-wire waveguide operated at mid-infrared wavelengths on the GeOI wafer. Optical modulation by carrier injection into the Ge waveguide was also demonstrated for the first time. For strained SiGe optical modulators, we have proposed MOS-based optical modulators fabricated by wafer bonding. We have established the void-less wafer bonding technology by using Al_2O_3/HfO_2 interfacial layer for wafer bonding.

III-V CMOS photonics

S. Takagi, M. Takenaka, Y. Chen, J. Park, S. Takashima, N. Sekine

We have investigated the III-V CMOS photonics platform by using III-V on insulator wafer. On the III-V-OI wafer, III-V MOSFETs and III-V photonics can be monolithically integrated. We have successfully integrated an InP grating coupler with waveguide InGaAs photodetector (PD) on the III-V CMOS photonics platform. We have also revealed that a depletion-based InGaAsP optical modulator exhibits 4 times higher modulation efficiency than Si. We have also clarified the mechanism of quantum well intermixing on the III-V-OI wafer. In addition, the bandgap wavelength shift of more than 100 nm has been demonstrated, enabling active-passive integration on the III-V CMOS photonics platform.

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