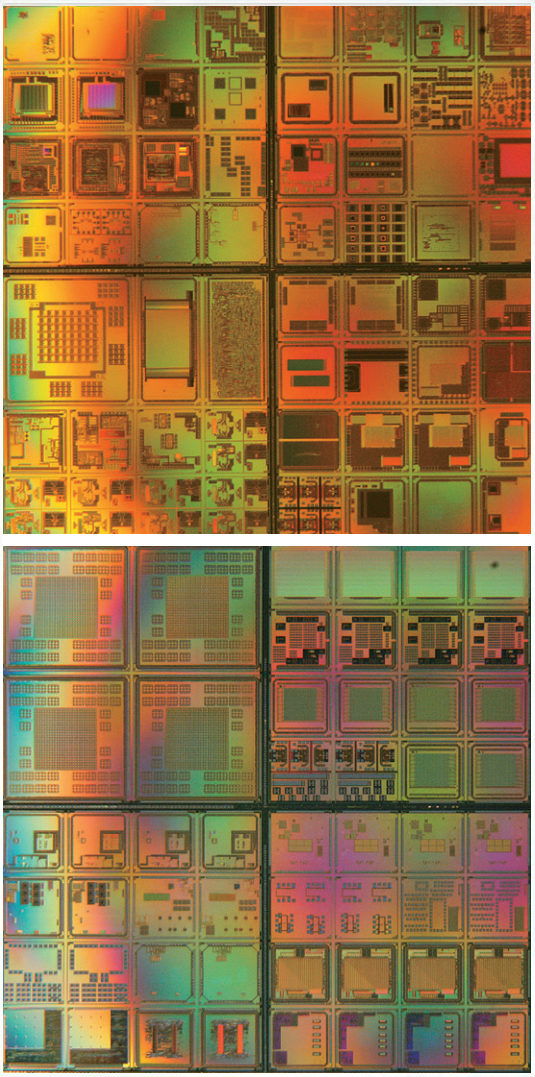
VDEC

平成29年度

東京大学
大規模集積システム設計教育研究センター
年 報

2017
VLSI Design and Education Center, The University of Tokyo Annual Report



VLSI Design and Education Center The University of Tokyo 2017

VLSI Design and Education Center
The University of Tokyo

This is the 2016 Annual Report of VDEC（VLSI Design and Education Center, University of Tokyo）.

Since VDEC was established in 1996, we held "The VDEC 20th Anniversary Symposium" on January 20th this year. After many warm addresses and messages from representatives of Government, industry and academia including oversee, successful researches and educations were reported from VDEC user universities. We also invited speakers on attractive resent topics in LSI fields. We made a fresh resolve to continue our activities. We also looked back changes in the semiconductor technology and economic situation in the past 20 years, which is almost a half of the LSI history. We thank again many attendees and speakers for success of the symposium.

LSI chip design/implementation in 2016 went well as previous years in general. The use of the 0.8 um CMOS, however, remained low and the use of the 0.18 um CMOS showed decreasing tendency, though the 65 nm SOTB was fine. We decided to reschedule the 0.18 um fabrication runs. We apologize for any inconvenience caused by the schedule change. After this we will guarantee two runs per year for each of 0.8 um and 0.18 um CMOS by restructuring VDEC budget plan for this purpose. And every time when incomes from users reach the cost of another run, we will schedule an additional run. The third run of 0.18 um would be possible so far as the user demands do not decrease so much. The demand of 0.8 um CMOS, however, seems hard to recover. For the time being VDEC will use the chip area for user designs as well as "master slices for QTAT CMOS gate array." This is one week TAT gate array with one metal programing. Though users need a small cost, it is easy to design and will be suitable for student labs. It has been used for the 3rd year education in the EE department of our University for long time. Its PDK is ready for use and we will soon make an announcement.

Number of users of the VDEC nano-fabrication facilities is still increasing. The rate of facilities operation and the occupancy of cleanroom are almost 100%. It is a result of a positive feedback that "good conditions of facilities attract new users and new users help to keep good conditions." We will keep the feedback by an appropriate budget to the cleanroom. One of the basis of the budget is "MEXT-JST nanotech-platform project." It is at the turn of the ten-year project. We want to keep the good reputation of the VDEC activities, so as to continue to the next project, too.

VDEC introduced "the cost-sharing system for VDEC academic CAD licenses" last year. The income will be used to partially compensate the constant decrease of VDEC budget from Government for the last 20 years. Now the academic CAD licenses will be provided stably for years. We thank CAD users for understanding. Recent year, however, researches targeting commercial developments are becoming active in academia. The academic CAD licenses are not applicable for these purposes. VDEC has been looking for a possible way to support them. Thanks to understanding of CAD vendors, VDEC could introduce "extended academic CAD licenses" last year, which can be used for the above purposes. The first examples were NEDO projects. We would like to support other industry-academia joint projects, too.

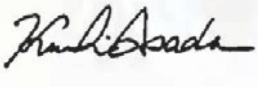
The D2T (Design-to-Test) research division, donated by Advantest Corporation, was renewed last October (the 4th term). The 11th D2T symposium was successfully held on September 21st 2016 and the next symposium is scheduled on September 28st of this year. We would like to express our sincere thanks to Advantest Corporation for the continuous support.

We will continue to do our best for the original mission of VDEC, "promotion of education and research in LSI design by means of practical chip-design and implementations", in order to realize research and education for enhancing the value of the semiconductor technology. We thank you for your continuous supports again.

VLSI Design and Education Center, University of Tokyo

Director Kunihiro Asada

June, 2017



VLSI Design and Education Center, The University of Tokyo
Annual Report 2017

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Chapter 1 Activity Report of VDEC

1.1 Introduction of VDEC activities and activity report of FY2016

VLSI Design and Education Center(VDEC), University of Tokyo was established in May 1996. VDEC has been operating for the following 3 major roles: "spreading the latest information on VLSI design and education," "providing licenses of CAD tools," and "supporting on VLSI chip fabrications for academic use." The VDEC activity report of FY 2016 is described hereafter according to Fig. 1. 1. 1.

The missions of VDEC are for advancement of researches and education on LSI design in public and private universities and colleges in Japan and send many distinguished VLSI designers into industry. After 19 years of VDEC establishment, educations on CAD software, LSI design and design flow in universities have been well established. On the other hand, advancement on nano-meter CMOS technologies forces design flow and CAD software complicated. We have been continuing CAD tool seminar by the lecturers from EDA vendors for twice a year. We hold the seminar in VDEC and provide distance learning through video streaming. We expect spread of the up-to-date LSI design methodology by using CAD tools.

We assume our LSI design flow seminars as educations on basic LSI design concepts and practical experience of LSI design with CAD tool chain. VDEC holds "LSI design education seminar", a.k.a. VDEC Refresh Seminar, once a year. This year we hold 3 courses, "Analog design course" and "RF design course", and initiated "MEMS design course" in July-September time frame. We invite experienced professors among universities as lecturers for the courses to conduct LSI design education courses with practical experience. We also hold "Transistor level design flow in VDEC" and "Digital design flow in VDEC EDA environment" for designers in universities. We started to charge these two LSI design education courses, as well as VDEC Refresh Seminars.

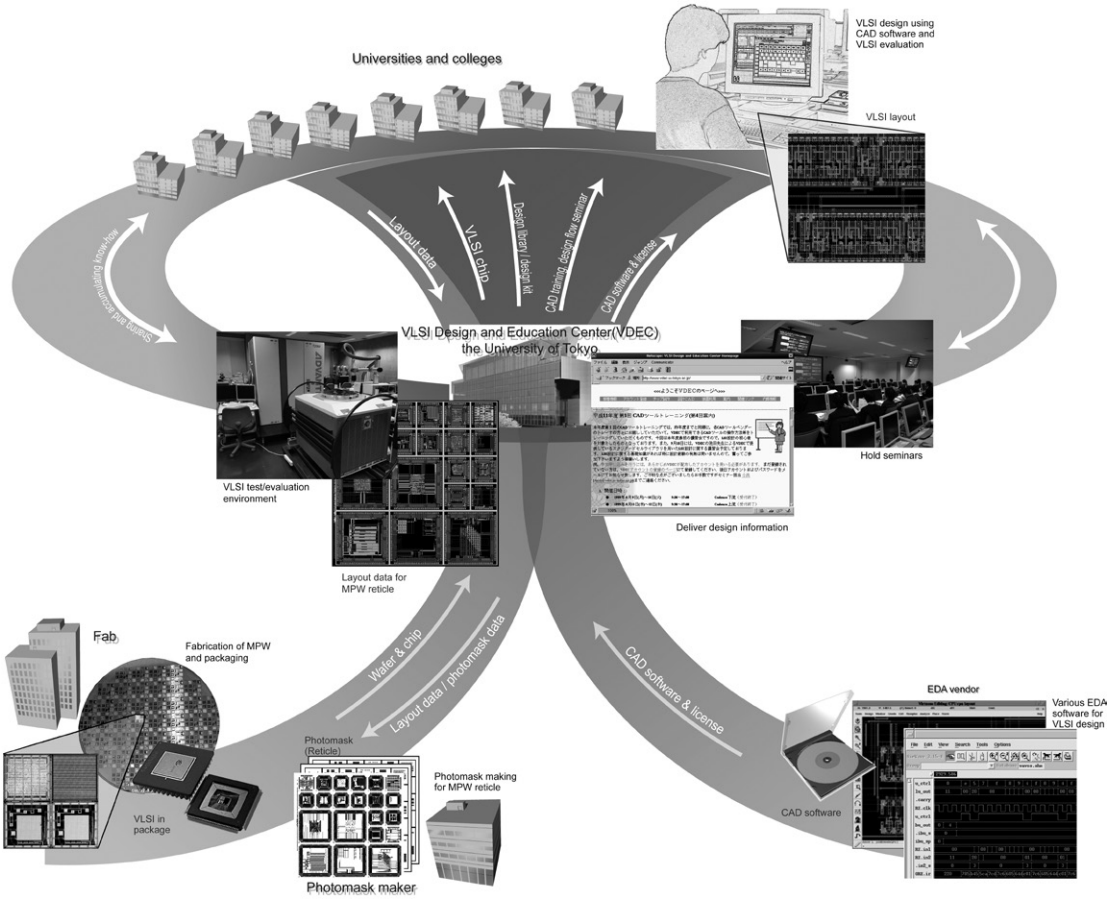


Fig. 1. 1. 1 VDEC activities

In addition to the above seminars, we hold "VDEC Designer'Forum" among young professors and students annually. This is a workshop that the participants exchange their design examples with not only success stories but also their failure stories, in addition to invited talks. We expect students and professors who will start designs to learn kinds of know-hows. We have initiated "IEEE SSCS Japan Chapter VDEC Design Award" this year, and final examination and awarding have carried out during the "VDEC Designer'Forum". Mr. H. Shiomi(Kyoto Univ.) is awarded as "IEEE SSCS Japan Chapter VDEC Design Award" winner, and Mr. M. Tamura(Univ. of Tokyo), Mr. A. Yoshimura (Nara Institute of Science and Technology), Mr. T. Asano (Kobe Univ.) are awarded as "the best VDEC Design Award", and Mr. T. Kaan (Tokyo Tech), Mr. S. Imanishi (Shizuoka Univ.), Dr. K. Parit (Univ. of Tokyo) are awarded as the "VDEC Design Award." Also Mr. Y. Sato (Shizuoka Univ.), Mr. H. Hayami (NAIST), and W. Nattakarn (NAIST) are awarded as the "VDEC Design Award."

LSI designers come up against various difficulties during actual LSI design scene, even after the basic educations through various seminars and the forum. One of the biggest problems for beginners is the setup of CAD softwares. Many of them also get confused by "Esoteric messages" come out from CAD softwares, even after they successfully setup CAD tools. In such situations, VDEC mailing-lists make significant contributions. VDEC users can register to VDEC mailing-lists on CAD tools, and process dependent groups through VDEC web pages, and can ask questions and helps on their facing issues. It is not a responsibility for the registrant of such mailing-lists to give answers to questions, however, in most cases, replies are given by the experienced users of CAD tools and experienced designers within a couple of hours to a couple of days. Moreover, emails are accumulated and are open to the VDEC users, as shown in Fig. 1. 1. 2, who have registered VDEC accounts, as the important educational assets. We expect all the VDEC users to make the full use of this mechanism to help solve problems.

We continue chip fabrication services on FDSOI CMOS 28 nm by ST Microelectronics, 0.18 mm CMOS by Rohm and 0.8 μm CMOS by On-semi Sanyo Semiconductor. And started chip fabrication services on SOTB CMOS 65 nm by Renesas Electronics.

Our donated division "Design To Test(D2T)", which was founded by donation from Advantest in Oct. 2008, focuses on enrichment of education on LSI testing and bridging between design and testing.

Fig. 1. 1. 3 shows trends of number of papers through VDEC activities. Number of papers is increasing, which means researches in the field of VLSI design have been encouraged after VDEC establishment.

Fig. 1. 1. 4 shows number of papers related to CAD usage, chip fabrications and VDEC facility usages. CAD tools are widely used to write papers. CAD tools are used not only chip designs themselves but also used for preparation of chip fabrication and they contribute to verify fundamental ideas of researches. Advanced CMOS processes are preferred for publications, and not only papers with 65 nm/40 nm CMOS chips, but also with 32 nm CMOS, 22 nm CMOS and 14 nm CMOS are emerging in the world. We would like to prepare chip fabrication services for the advanced CMOS processes. In

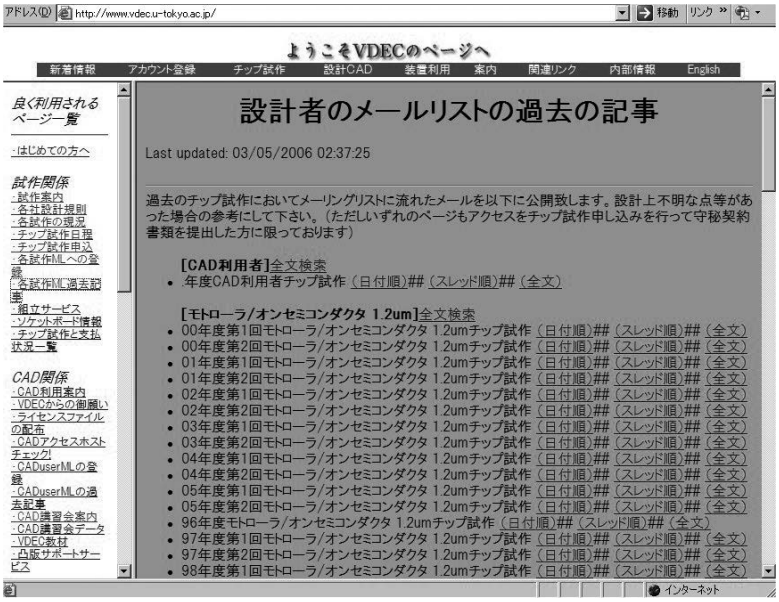


Fig. 1. 1. 2 Archives of emails of VDEC mailing-list.

addition, we would like to setup chip fabrication services related to CMOS/MEMS to fulfill the researches for "More than Moore". We also encourage researchers to fully use of VDEC facilities such like LSI testers, FIB systems and EB writer for the wide spread of research purposes.

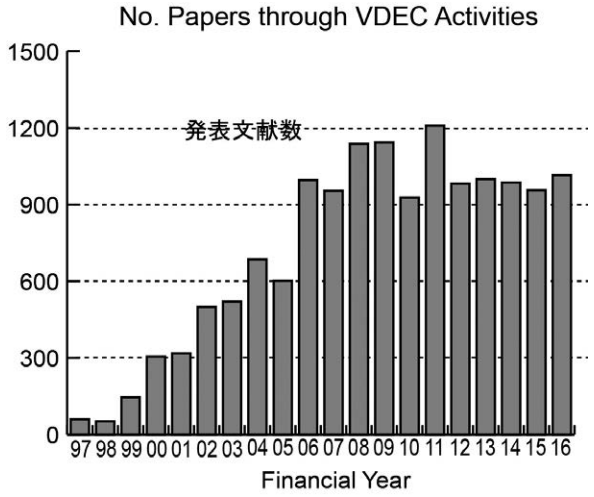


Fig. 1. 1. 3 Trends of number of papers through VDEC activities.

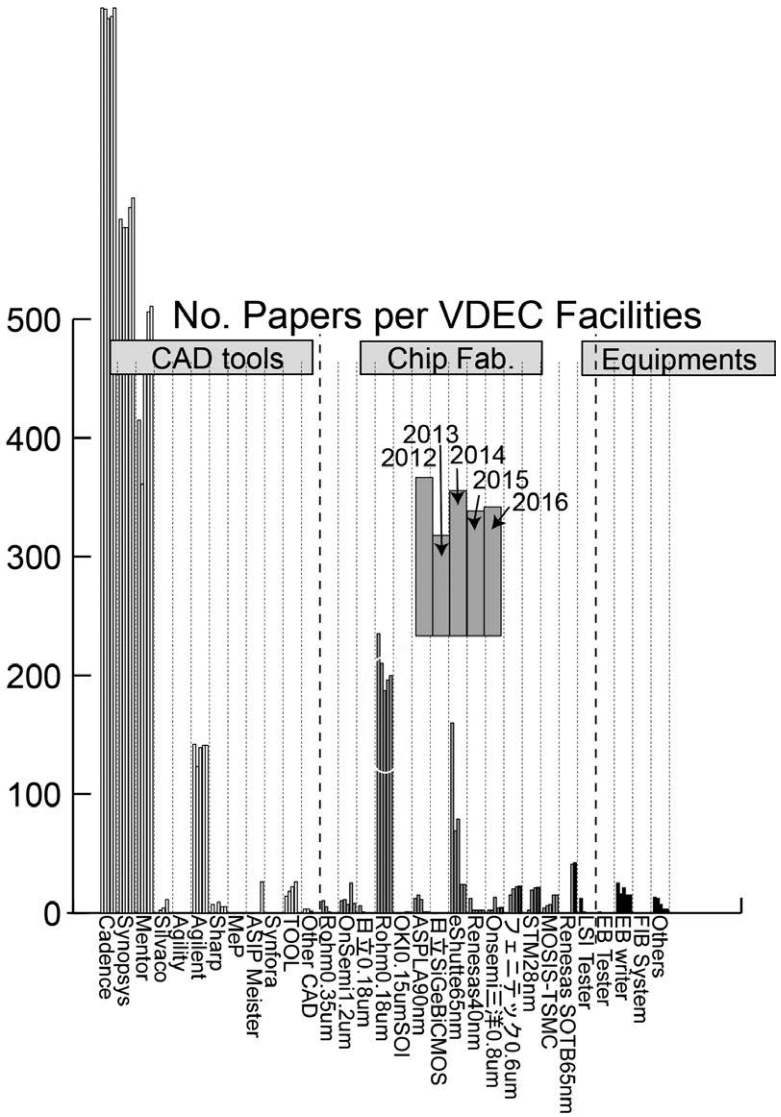


Fig. 1. 1. 4 Number of papers related to VDEC facilities.

1. 2 VDEC CAD Tools

Since 1996, VDEC has provided CAD software licenses to the registered researchers in universities and colleges in Japan. The CAD tools we provided in 2017 are shown in Table 1. 2. 1. The researchers can use those CAD tools when their local machines, whose IP addresses are registered in advance, are authorized by one of VDEC license server located in the ten VDEC subcenters shown in Fig. 1. 2. 1. For each CAD tool, VDEC provides 10-100 floating licenses. Those CAD tools can be utilized only for research and education activities in national universities, other public universities, private universities, and colleges.

When one is going to use VDEC CAD tools and chip fabrication service (the details are described in Section 1-3), some faculty member of his/her research group in a university or a collage needs to do user registration. Fig. 1. 2. 2 shows (a) the number of registrants, (b) the number of distinguished universities/colleges of the registrants, and (c) the number of registrants who applied VDEC CAD tools.

Table 1. 2. 1 VDEC CAD tools

Name	Function	Vendor
Cadence tool set	Verilog-HDL/VHDL entry, Simlation, Logic synthesis, Test pattern generation, Cell-based (including macros) place, route, and back-annotation, Interactive schematic and layout editor, Analog circuit simulation, Logic verification, Circuit extraction	Cadence Design Systems, Inc.
Synopsys tool set	Verilog-HDL/VHDK simulation, Logic synthesis, Test pattern generation, Cell-based (including macros) place, route, and back-annotation, Circuit simulation, Device simulation	Synopsys, Inc.
Mentor tool set	Layout verification, Design rule check	Mentor Graphics Co. Ltd.
Silvaco tool set	Fast circuit simulation	Silvaco
ADS/Golden Gate	Design and verification of high-frequency circuits	Keysight Technologies
Bach system	BachC-based design, synthesis, and verification	Sharp
LAVIS	Layout visualization platform	TOOL

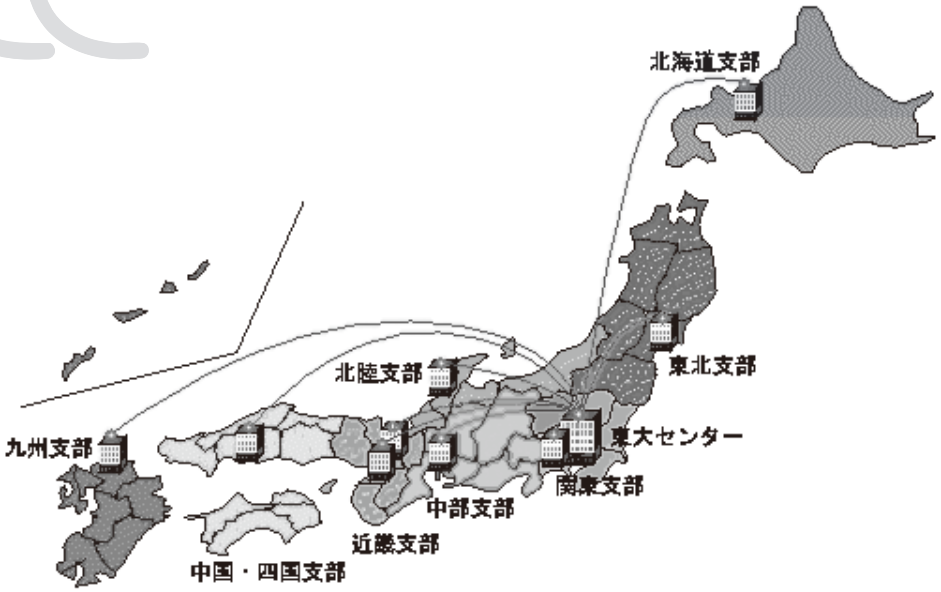
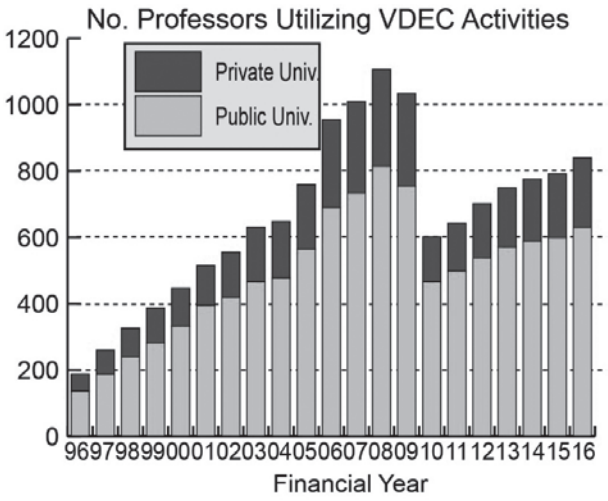
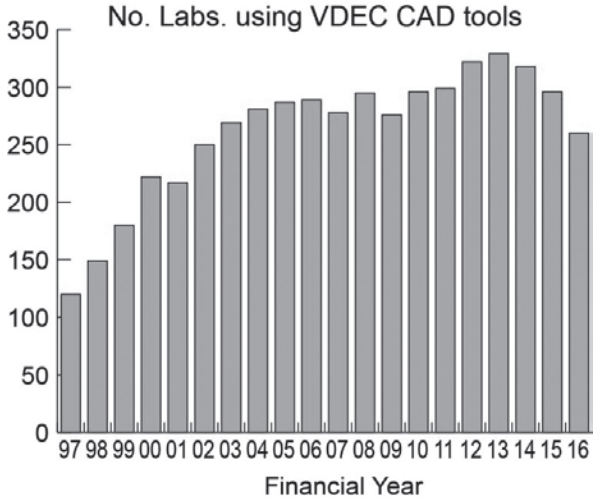


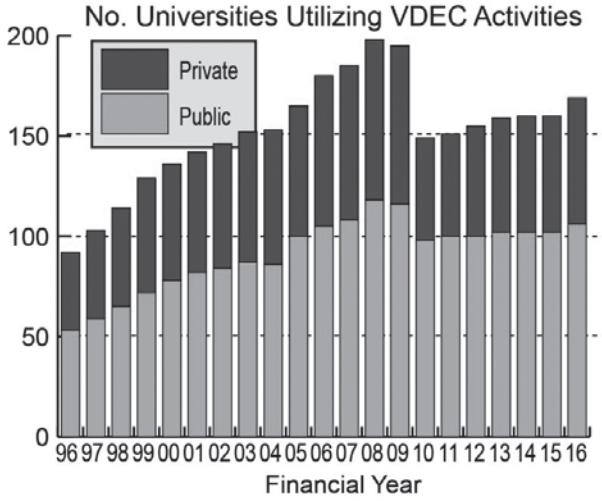
Fig. 1. 2. 1 VDEC Subcenters



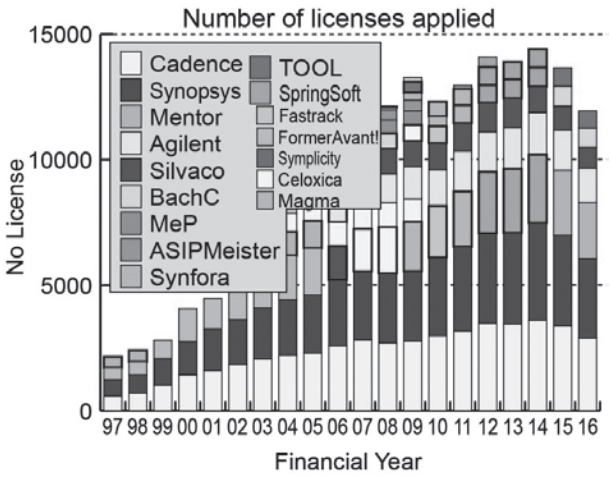
(a) The number of registrants



(c) The number of research group applied CAD tools



(b) The number of universities colleges of the registrants



(d) The number of applied licenses of all CAD tools

Fig. 1. 2. 2 The numbers of VDEC CAD Applications

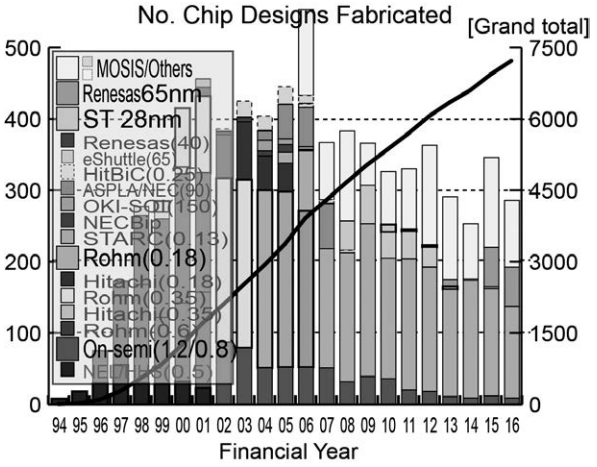
1. 3 VLSI Chip Fabrication

1. 3. 1 Trends of VLSI Chip Fabrication Services

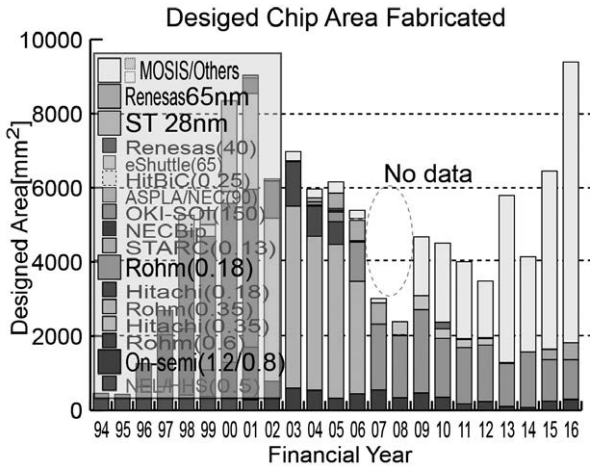
Fig. 1. 3. 1 shows a trend of number of designed chips for VDEC chip fabrication services, including pilot project prior to VDEC establishment.

VLSI chip fabrication is limited to 0.5 mm CMOS provided by NTT Electronics during the pilot project in 1994 and 1995. VDEC chip fabrication had started in 1996 with 1.2 mm CMOS provided by Motorola Japan, which is now On-Semiconductor as well as the 0.5 mm CMOS. In 1997, VDEC received cooperation from Rohm and has started 0.6 mm CMOS process. In 1998, VDEC started chip fabrication services of 0.35 mm CMOS by Hitachi, and in 1999, VDEC started 0.35 mm CMOS by Rohm. We had a test chip fabrication of 0.13 mm CMOS by STARC through "IP development project" in 2001. We added 0.18 mm CMOS by Hitachi into our chip fabrication menu in 2001. From 2002, we started VDEC-MOSIS chip fabrication program initiated by Prof. Iwata of Hiroshima University. Under this program, VDEC member can access to TSMC and IBM processes with lower price. We also started Bipolar chip fabrication by NEC Compound Semiconductor Devices. In 2004, we started 0.15 mm SOI-CMOS chip fabrication by Oki Electric as test chip fabrications. In the same year we started 90 nm CMOS chip fabrication by ASPLA/STARC. In 2006, we started 0.18 mm CMOS by Rohm and 0.25 mm SiGeBiCMOS by Hitachi. In 2008, we started 65 nm CMOS process by eShuttle, after closure of 90 nm CMOS chip fabrication in 2007. In 2010, we started 40 nm CMOS process by Renesas Electronics through "Next Generation Semiconductor Circuits & Architecture" project between METI and STAR. On the other hand, 1.2 mm CMOS chip fabrication program came to end by the September 2011. 40 nm CMOS by Renesas Electronics and 65 nm by eShuttle also come to end by Oct. 2012 and Aug. 2013, respectively. We started CMOS0.8 μm in Oct. 2012 by On-semiconductor-Sanyo as a test chip fabrication and opened it as the regular chip fabrication menu in 2012. We started FD-SOI 28 nm CMOS by ST-Microelectronics through CMP, France, as the advanced CMOS process in 2013. We started SOTB 65 nm CMOS by Renesas Electronics in 2015.

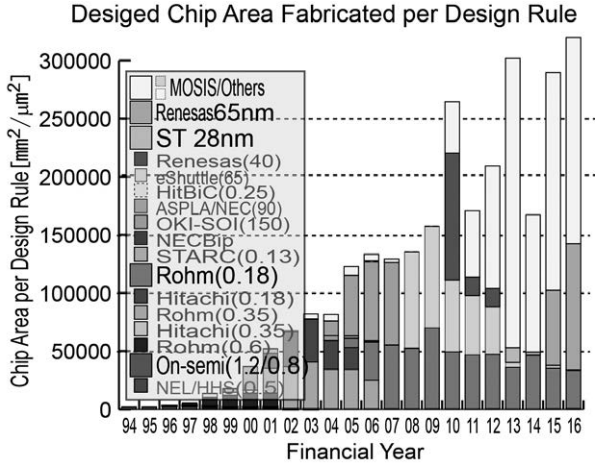
Fig. 1. 3. 1(a) shows trends of number of chip designed for VDEC chip fabrication. For the first 6 years until 2001, the number of designed chips shows steady increase, which means drastic improve of the effectiveness researches and education of LSI design, and we assume drastic increase of number of students related to LSI chip



(a) Trend of number of designs fabricated.



(b) Trend of designed area.



(c) Trend of designed area normalized by design rule.

Fig. 1. 3. 1 Trend of number of designs and designed chip area.

design and education. During few years of stable number around 400 chip designs per year, we can see transition of designs toward finer process. In 2007, we saw a large drop, which was caused by sudden process transition from 0.35 mm CMOS to 0.18 mm CMOS, and in 2008, we also saw another drop by process transition from 90 nm CMOS to 65 nm CMOS.

Fig. 1. 3. 1(b) shows trends of designed chip area, which shows much clear trends of drop by process migration. On the other hand, Fig. 1. 3. 1(c) shows trends of designed chip area normalized by design rule, which assume to be strong relation with design efforts. Coming from the fact that the normalized chip area is still growing, we assume the major reason for decrease of number of chips and designed area is increase of design effort per chip and per unit area due to process scaling.

Fig. 1. 3. 2 shows trends number of professors and universities fabricated chip. Number of professors who have contracted NDA for process technologies to access design rules and design libraries are, 72, 274, and 38, respectively, for 65 nm CMOS, 0.18 mm CMOS, and 0.8 um CMOS.

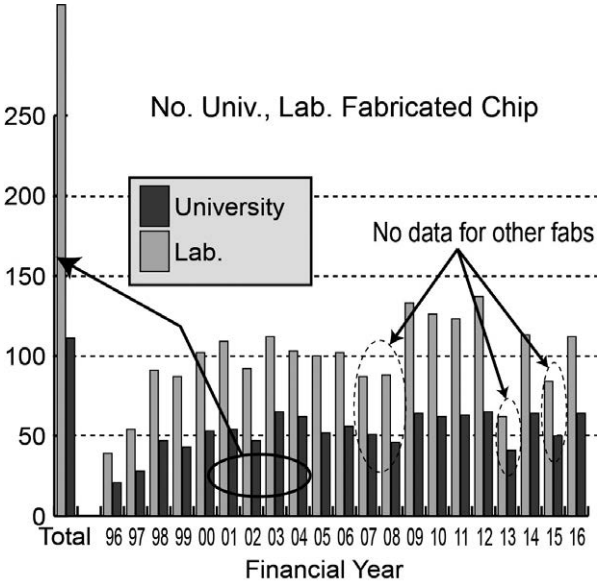


Fig. 1. 3. 2 Trend of number of processors and universities fabricated chip.

1. 3. 2 Overview of chip fabrication in 2015

Table 1. 3. 1 lists chip fabrication schedule in 2015. Please refer to list in Chapter 2 for details of designers and contents of chip designed.

Table 1.3.1 Chip fabrication schedule in 2016

○ 0.8 mm CMOS (On-Semiconductor - Sanyo)

	Chip application deadline	Design deadline	Chip delivery
2016 #1	2016/ 7/ 8	2016/ 9/30	2017/ 2/ 9
2016 #2	2016/12/30	2017/ 3/24	2016/ 6/20

○ 0.18 mm CMOS (Rohm)

	Chip application deadline	Design deadline	Chip delivery
2016 #1	2016/ 3/ 7	2016/ 5/30	2016/ 9/20
2016 #2	2016/ 5/ 2	2016/ 7/25	2016/11/14
2016 #3	2016/ 6/28	2016/10/17	2016/12/27
2016 #4	2016/11/28	2017/ 2/20	2017/ 6/16

○ SOTB 65 nm CMOS

	Chip application deadline	Design deadline	Chip delivery
2016 #1	2016/ 5/23	2016/ 7/ 4	2017/ 2/20
2016 #2	2016/12/12	2017/ 1/23	2017/ 8M

1. 3. 3 Libraries and design flows

VDEC have been working to prepare design libraries and design flows for digital design and PDKs for analog design. Table 1. 3. 2 lists libraries available now.

Table 1. 3. 2 Libraries available for VDEC chip fabrication

Technology	Name	Author	Contents
0.18 mm CMOS (Rohm)	Rohm library	Rohm Library Std. Cells, IO cells, RAM (Distributed with CDROM)	Synthesis(Synopsys)
			Simulation(VerilogXL)
			P&R(LEF/DEF)
	Kyodai Library	Onodera Lab., Kyoto University	Synthesis(Synopsys)
			Simulation(VerilogXL)
			P&R(Astro)
	Todai Library	VDEC Design flow based on library prepared by Onodera Lab., Kyoto University	Synthesis(RTL Compiler)
			Simulation(VerilogXL)
			P&R(Encounter)
	PDK	VDEC	PDK(IC6.1)

1.4 Seminar

Seminar is indispensable for the improvement of LSI design technology. Some seminar and forums, such as technical seminar for CAD use, refreshing seminar for working people, designer's forums for young professors and students were held in 2016.

【Technological seminar for CAD use】

In a technological seminar for CAD use, VDEC invites lecturer from each tool vender, such as Cadence, Synopsys and Agilent, to hold the CAD operation course. Moreover, the course concerning the design flow in the VDEC environment was held by the VDEC staff. A technological seminar for CAD use for the beginner was held in The University of Tokyo VDEC in August and September at the year 2016. This seminar took 5 days for 2 kinds of Cadence tools, 3 days for 2 kinds of Synopsys tools, 1 days for 1 kind of Keysight tool. In addition, VDEC teachers gave lecturers on transistor level circuit design course, and digital circuit design course under the VDEC EDA environment. Teachers and students up to 40 people attended a lecture in each course, and master the use of each tool for VLSI design flow that uses the VDEC library. Moreover, another technical seminar for CAD use for matured teachers and students was held in March by Cadence 2 kind and 5 days, Synopsys 3 kinds and 4 days (Table 1. 4. 1). The demand for these CAD technological seminars is very large, and VDEC has maintained the mechanism of a large-scale CAD technological seminar holding corresponding to this situation. So far, the seminar was held at the University of Tokyo OR other VDEC branch, however, we started to distribute the lecture using Web streaming, so that students around VDEC branch can take the seminar at the branch school.

Table 1. 4. 1 CAD technological seminar in summer of the year 2016

2016/08/02	Keysight Empro Seminar	Univ. of Tokyo	13
2016/08/02	Keysight Empro Seminar	Hokkaido Univ.	2
2016/08/02	Keysight Empro Seminar	Kanazawa Univ.	1
2016/08/03-04	Synopsys DesignCompiler+PowerCompilerSeminar	Univ. of Tokyo	9
2016/08/03-04	Synopsys DesignCompiler+PowerCompilerSeminar	Hokkaido Univ.	2
2016/08/03-04	Synopsys DesignCompiler+PowerCompilerSeminar	Tohoku Univ.	4
2016/08/03-04	Synopsys DesignCompiler+PowerCompilerSeminar	Osaka Univ.	5
2016/08/30-31	Cadence Virtuoso ADE Seminar	Univ. of Tokyo	16
2016/08/30-31	Cadence Virtuoso ADE Seminar	Hokkaido Univ.	3
2016/08/30-31	Cadence Virtuoso ADE Seminar	Tohoku Univ.	5
2016/08/30-31	Cadence Virtuoso ADE Seminar	Kanazawa Univ.	2
2016/08/30-31	Cadence Virtuoso ADE Seminar	Kyoto Univ.	2
2016/08/30-31	Cadence Virtuoso ADE Seminar	Hiroshima Univ.	3
2016/09/01	Synopsys HSPICE Seminar	Univ. of Tokyo	12
2016/09/01	Synopsys HSPICE Seminar	Hokkaido Univ.	2
2016/09/01	Synopsys HSPICE Seminar	Tohoku Univ.	4
2016/09/01	Synopsys HSPICE Seminar	Kanazawa Univ.	2

2016/09/01	Synopsys HSPICE Seminar	Kyoto Univ.	3
2016/09/01	Synopsys HSPICE Seminar	Osaka Univ.	3
2016/09/01	Synopsys HSPICE Seminar	Hiroshima Univ.	2
2016/09/05-07	Cadencee Virtuoso Layout Seminar	Univ. of Tokyo	26
2016/09/05-07	Cadencee Virtuoso Layout Seminar	Hokkaido Univ.	3
2016/09/05-07	Cadencee Virtuoso Layout Seminar	Tohoku Univ.	3
2016/09/05-07	Cadencee Virtuoso Layout Seminar	Kanazawa Univ.	2
2016/09/05-07	Cadencee Virtuoso Layout Seminar	Osaka Univ.	3
2016/09/05-07	Cadencee Virtuoso Layout Seminar	Hiroshima Univ.	1

2017/03/01-02	Cadence Allegro Design Entry Front to Back Seminar	Univ. of Tokyo	11
2017/03/01-02	Cadence Allegro Design Entry Front to Back Seminar	Hokkaido Univ.	1
2017/03/01-02	Cadence Allegro Design Entry Front to Back Seminar	Tohoku Univ.	4
2017/03/08	Synopsys XA-VCS CoSim Seminar	Univ. of Tokyo	10
2017/03/08	Synopsys XA-VCS CoSim Seminar	Hokkaido Univ.	1
2017/03/08	Synopsys XA-VCS CoSim Seminar	Osaka Univ.	2
2017/03/08	Synopsys XA-VCS CoSim Seminar	Hiroshima Univ.	1
2017/03/09-10	Synopsys IC Compiler Seminar	Univ. of Tokyo	14
2017/03/09-10	Synopsys IC Compiler Seminar	Hokkaido Univ.	1
2017/03/09-10	Synopsys IC Compiler Seminar	Osaka Univ.	1
2017/03/09-10	Synopsys IC Compiler Seminar	Hiroshima Univ.	2
2017/03/15	Synopsys HSPICE+VerilogA Seminar	Univ. of Tokyo	17
2017/03/15	Synopsys HSPICE+VerilogA Seminar	Hokkaido Univ.	2
2017/03/15	Synopsys HSPICE+VerilogA Seminar	Kyoto Univ.	5
2017/03/15	Synopsys HSPICE+VerilogA Seminar	Hiroshima Univ.	1
2017/03/27-29	Cadence Encounter Digital Implementation Seminar	Univ. of Tokyo	7
2017/03/27-29	Cadence Encounter Digital Implementation Seminar	Hokkaido Univ.	1
2017/03/27-29	Cadence Encounter Digital Implementation Seminar	Osaka Univ.	3

【Refresh Seminar for Working People】

Teachers of universities and designers in the first line of the enterprise were invited to the lecturer at "VLSI design refresh seminar" was held aiming at the latest, advanced knowledge and technical learning concerning VLSI design as a refreshing education for working people involved in the integrated circuit industry (Table 1. 4. 2). Though this seminar started chiefly in year 1998 under the support of Ministry of Education Technical Education Division to give practicing education of the latest VLSI design technology, it continues under many supports from many societies.

Course A: analog integrated circuit design (7/11 -13), Course M1: MEMS design (7/4-5), Course M2:MEMS fabrication (7/25-7/27), and Course R: RF

circuit design (7/27-28). Teachers from industry and universities involved in the integrated circuit research and the education were invited as the lecturer, and they introduced a state-of-the-art VLSI design technology including the practice using a lecture concerning VLSI design and the latest CAD tool. The participants for the course A, M1, M2, R were 18, 8, 6, 7, respectively.

Fig. 1. 4. 1 Refresh Seminar at VDEC seminar room at the University of Tokyo, VDEC.

Table 1. 4. 2 Refresh Seminar

Course A: Analog Circuit Design (3 days)
Analog Circuit Design and simulation Integrated Circuits Verification (LVS, DRC)
Masahiro Sugimoto (Chuo Univ.), Hidetoshi Onodera (Kyoto Univ.), Koji Kotani (Tohoku Univ.)

Course M1: MEMS Design (2 days)
MEMS Basic 1: Fabrication Process MEMS Basic 2: Operation Principle Structual Design Layout Design
Yoshio Mita (Univ. of Tokyo)

Course M2: MEMS Fabrication (3 days)
CAD Design and Analysis Lithography, Etching, Release Vibration measurement and analysis
Yoshio Mita (Univ. of Tokyo)

Course R: CMOS-RF Circuit Design (3days)
Modulation/Demodulation, Cascaded connection Basic Performace, Tranceiver Architecture Circuit Element, Design Flow
Hiroyuki Ito (Tokyo Institute of Technology)

【Designer's forum for young teachers and students】

VDEC LSI designer forum intended for students and young teachers has been held. The VDEC LSI designer forum has aimed to sharing information that cannot be obtained at a society and a academic society, for example, the failure case and the solution in which LSI designer has a hard time, the inside story of CAD industry, the construction method in the design milieu in the laboratory, and so on. This year, we had the meeting in Takeda Hall in The University of Tokyo, in August. No less than 50 participants were flourishing at the gathering.

Table 1.4.3 Program of Designers Forum in 2015

8/25(Thu)

Time	
9:30-10:00	Reception
10:00-11:00	Prenary Talk Kazuhiko Takagawara (NTT) Vital Sensing Technology by Wearable Devices.
11:00-12:00	VDEC Design Award Presentation
12:00-13:00	lunch
13:00-15:00	VDEC Design Award Presentation
15:00-15:20	break
15:20-18:20	VDEC Design Award Presentation
19:00-	VDEC Design Award award ceremony

8/26(Fri)

Time	
9:00-12:00	Ph.D Session
12:00-13:00	lunch
13:00-15:00	VDEC Design Award Idea Contest Presentation
15:00-15:20	break
15:20-16:50	VDEC Design Award Idea Contest Presentation
17:00-	VDEC Design Award Idea Contest award ceremony

1.5 Facilities

The VDEC has provided the big facilities for universities in Japan from its establishment (1996). Big facilities refer to those which are impossible to acquire and or maintain by an individual research unit. Table 1.5.1 shows the available facilities of VLSI testers and some process machines, which are placed at the tester room and the super clean room of the Takeda building. In 2004, the VLSI tester (T2000) and the EB lithography machine (F5112+VD01) were donated to the VDEC by the ADVANTEST. In the year 2012, VDEC joined MEXT (Ministry of Education)'s Nanotechnology platform to enforce its multi-use capability. (For Nanotechnology Platform refer section 1.8). From April 2015 to March 2016, the EB lithography machine F5112 has been used 1317 times. The reason of slight decrease of number since last year (89 times less from 1406 in 2015) can be attributed to user shift to new EB apparatus. The exposure count of the new apparatus (F7000S-VD02) was increased to 1042 times that is +333 increase from last year (709 exposures in 2015). Total exposure number of EB machines have therefore increased from 2115 (in 2015) to 2359 (+244).

The facilities can be used by user himself, after a couple of times'training by attendance of licensed users; also, by presence of licensed persons, a new user can readily use the machine.

Table1. 5. 1 Available facility list

Facility	Equipment name	Description	Status	Contact
Logic LSI test System	EB tester: IDS10000	The chip surface voltage during operation can be measured with the LST tester. The digital circuit with 384 pins, 1 GHz can be tested.	Available	nanotech@ sogo.t.u-tokyo.ac.jp
	LSI tester: ADVANTEST T2000	The digital circuit with 256 pins, 512 MHz can be tested. Analog test is optional.	Available	nanotech@ sogo.t.u-tokyo.ac.jp
	Auto prober: PM-90-A	Automated prober for testing LSI wafers, which can be used with the LSI testers. The probe card for LSIs with the VDEC standard pin connections is available.	Available	nanotech@ sogo.t.u-tokyo.ac.jp
Analog/RF measure-ment system	Analog/RF measurement system: B1500A, 4156B, HP4284, etc	DC parameter measurement, Capacitance measurement, Network analyzer, Spectrum analyzer, etc.	Available	nanotech@ sogo.t.u-tokyo.ac.jp
	Low-noize manual prober: Cascade Microtec	6 inch wafer can be measured with six DC probles and two RF probes upto 50 GHz.		
	Low-noize, temperature controlled semi-auto prob-er: Süss Microtec	8inch wafer can be measured. The chip tem-perature range is −50 to 200° C.		

Nanotechnology Platform Apparatuses	Mask lithography, Direct lithography: F5112+VD01	Minimum linewidth: 50nm. Lithography for 5 inch photomask (thickness: 2.3 mm), 2-8 inch wafers, and chips is possible.	Available	nanotech@sogo.t.u-tokyo.ac.jp
	Rapid Mask and Direct lithography: F7000S-VD02	Minimum linewidth: 1xnm. Lithography for 5 inch photomask (thickness: 2.3 mm), 2-8 inch wafers, and chips is possible. Stencil character projection of non-square shapes such as circle, triangle is possible.	Available	
	Chlorine ICP plasma etcher CE-S	High density plasma etching with Cl2 and BCl3 is possible.	Available	
	Silicon DRIE MUC-21 ASE-Pegasus	High speed, high aspect ratio etching of silicon is possible	Available	
FIB system	FIB: SII XVision200TB	Repair of photomask, sample etching, etc. (Through Nanotech. Platform and LCNet)	Available	
LSI FIB system	FIB: FEI V400ACE	Repair of VLSI from both frontside and backside, with CAD navigation and / or IR camera is possible. W/SiO2 deposition is possible.	Available	
Chip Bonding System	Wedge Bonder: Westbond 7476D	25 μm ϕ Al or Au wire wedge bonding machine.	Available	
	Epoxy Die Bonder Westbond7200C	Precision Manupilator system. Epoxy and or Ag paste chip bonding and or glued wiring.		
	Semi-Auto Bonder Westbond4700E	18 ～ 25 μm ϕ Au Ball bonding or bump creation.		
	Precision Manual Flip-Chip Bonder Finetech Fineplacer Lambda	Face-to-face bonding up to 15 mm square chips. Alignment is through video camera. Bonding is by heating chips with TV camera. (Ultrasonic Unit can additionally be purchased.) XY ± 0.5 μm, and θ =1mrad precision.		

1.6 Activity plan for 2017

VDEC will continue activities on chip fabrication services, CAD tool support, dispatching design related information and donated division "D2T", as has been previous years.

【Design related information dispatching/Seminar】

We will continue holding the following seminars: (1) CAD tools seminars which have been continued since 1997, (2) "Refresh seminar" since 1998, (3) "Designer'Forum" since 1997. We will also continue seminars for LSI tester usage at VDEC and sub-centers, workshops on LSI testing technologies initiated by D2T.

【CAD tool support】

We will continue Cadence tools, Synopsys tools and Mentor tools as the main stream design tools. We will continue analog RF design environment, GoldenGate and ADS by Agilent, C-based design environment, BachC by Sharp. In addition, we continue trial of several CAD tools, such as layout platform, Lavis by TOOL. Design debugging platform from SpringSoft has merged into Cadence tools and will be continued. SmartSpice by Silvaco, will be also continued.

【Chip fabrication services】

We will continue chip fabrication services for SOTB 65 nm CMOS by Renesas Electronics, 0.18 mm CMOS by Rohm, FD-SOI 28 nm CMOS by ST Microelectronics through CMP and 0.8 mm CMOS by On-semiconductor-Sanyo as the regular services.

Table 1. 7. 1 Chip fabrication schedule

【CMOS 1.2 μm 2P2M】 On-Semiconductor(Former Motorola Japan)

	Chip application deadline	Design deadline	Chip delivery
2017 #1	2017/ 7/10	2017/10/ 2	2017/12/25
2017 #2	2018/ 1/15	2018/ 3/26	2018/ 6/25

【CMOS 0.18 μm 1P5M(+MiM)】 Rohm

	Chip application deadline	Design deadline	Chip delivery
2017 #1	2017/ 4/ 3	2017/ 6/26	2017/10/13
2017 #2	2017/ 8/ 7	2017/10/30	2018/ 2/16
2017 #3	2017/11/27	2018/ 2/19	2018/ 6/ 8

【FD-SOI CMOS 28 nm1P10M】 ST Microelectronics

Based on the chip fabrication schedule through CMP.

【SOTB CMOS 65 nm】 Renesas Electronics

	Chip application deadline	Design deadline	Chip delivery
2017 #1	2017/ 6/19	2017/ 7/31	2018/ 1/18
2017 #2	2017/12/18	2018/ 1/29	2018/ 7/12

1.7 Venture companies related to VDEC

Some professors related to VDEC started venture companies. The following is a list of the venture companies related to VDEC.

[1] AIL Co.,Ltd. (http://www.ailabo.co.jp/)

Related professor : Professor Kazuo Taki, Kobe Univ. (President-Director)

[2] Synthesis Corporation (http://www.synthesis.co.jp/)

Related professor : Professor Emeritus Isao Shirakawa, Osaka Univ. (Director)

Description of business : (1) Hardware/software co-design
(2) System LSI design, design services
(3) Development and sales of IPs
(4) Development of EDA tools

[3] Nanodesign Corporation (http://www.nanodesign.co.jp/)

Related professor : Professor Kazuyuki Nakamura, Kyushu Institute of Technology. (Representative Director)

[4] A-R-Tec Corp. (http://www.a-r-tec.jp/)

Related professor : Professor Emeritus Atsushi Iwata, Hiroshima Univ. (Representative Director)

Description of business : (1) Measurement and analysis of LSI substrate noise
(2) Design of analog-RF mixed signal LSIs
(3) Training of analog design on the JOB method

[5] Ishijima Electronics (http://ishi.main.jp/)

Description of business : (1) Electronic circuit development
(2) Software development
(3) Consulting

1.8 "Nanotechnology Platform": Ultra Small Lithography and Nanometric Observation Site

VDEC is operating an open-use nanotechnology platform "Ultra Small Lithography and Nanometric Observation Site" together with the Institute of Engineering Innovation of Graduate School of Engineering. The site is supported by Japanese Ministry of Education (MEXT)'s Nanotechnology Platform grant. Any researchers in Japanese Universities, Laboratories, and Companies can take full advantage of The University of Tokyo's cutting-edge nanotechnology apparatuses and know-hows. The accessible technology includes Lithography and Etching environment, Ultra High-Voltage Acceleration (1MV) transmission electron microscope (TEM) that is capable of visualizing upto light materials such as Nitrogen. VDEC takes part in the lithography at Takeda Sentanchi Super Cleanroom. Through VDEC's key apparatus F5112+VD01 donated from Advantest Corporation as well as F7000S-VD02 purchased by national budget, VDEC is supporting post-VLSI activities such as MEMS. The machine is capable of rapidly writing patterns on arbitrary-shaped targets sizing from 1cm-sqare chip to 8-inch round wafers. The performance is measured by the number of research reports and machine use. The University of Tokyo site has received 162 research reports, composed of 26 from big companies, 4 from Small and Medium-size Enterprises (SMEs), 28 from other universities, 91 from UTokyo researchers (including external collaboration but excluding VDEC), and 11 from public research institutes. The exposure count was 2359 for 12 months (196.5 / month), which is the record since beginning of existing statistics (total 460 for FY 2000). As shown in the Fig. 1, usage is monotonously increasing. "Open ratio", which is the number of days in which users outside the University of Tokyo came, divided by machine open days, was 99%. Due to the strong support of nanotech. Platform, even a novice user can obtain fine lithography result by using the apparatuses with the Platform engineering staffs of VDEC.

URL: http://nanotechnet.t.u-tokyo.ac.jp/

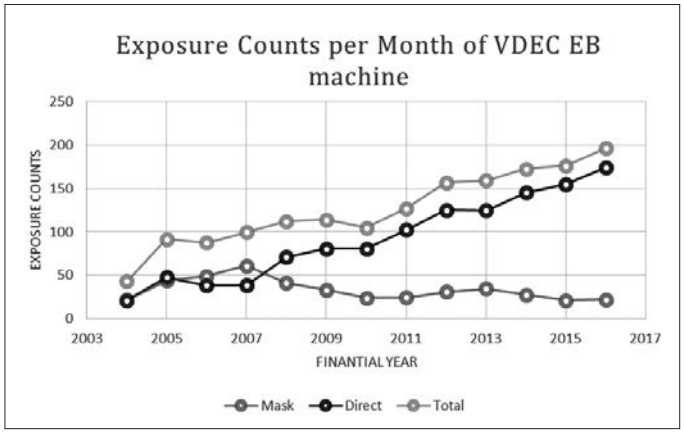


Fig. 1 Monthly Average Exposure Count of EB Machine (s).

Chapter 2 Activity Report of "ADVANTEST D2T Research Division"

2. 1 Introduction of "ADVANTEST D2T Research Division"

2. 1. 1 Aim of the establishment of "ADVANTEST D2T Research Division"

ADVANTEST D2T research division was established in VDEC in October 2007. As the name of the research division indicates, it is financially supported by ADVANTEST Corporation.

The aim of establishment of ADVANTEST D2T research division is to promote the research and education environment of VLSI testing in all universities and colleges in Japan." D2T" means that we consider not only design but also test. As the results of our activities, we hope to provide the experts of design and test for industry. In addition, we are exchanging researchers with other universities or research institute in both Japan and overseas. Moreover, D2T research division is in a good environment to make collaboration with industry because testing of VLSI is one of the most practical research topics in industry. Based on those activities, our final goal is to become a center of excellence of VLSI Testing in Japan.

D2T research division has spent 9 years in total with the 1st (Oct. 2007–Sep. 2010), 2nd (Oct. 2010–Sep. 2013), and 3rd (Oct. 2013–Sep. 2016) project phases already, and in October 2016, we lunched the 4th phase of D2T project through the courtesy of ADVANTEST Corporation.

In 2016, we invited Professor Stewart Smith from the University of Edinburgh (2016/5–2016/9), and Professor Krishnendu Chakrabarty from Duke University (2016/9–2016/12) for research and educational collaborations with VDEC.

Details of our group's activities are presented in the following sections.

2. 1. 2 Members of "ADVANTEST D2T Research Division"

Project Professor	Krishnendu Chakrabarty (Sep. 2016–Dec. 2016)
Project Associate Professor	Stewart Smith (May 2016–Sep. 2016)
Project Lecturer	Rimon Ikeno
Assistant Professor	Nguyen Ngoc Mai-Khanh
Researcher	Takahiro Yamaguchi (ADVANTEST Laboratories Ltd.)
Researcher	Masahiro Ishida (ADVANTEST Corporation)
Assistant Clerk	Makiko Okazaki

2. 2. Report of “11th D2T Symposium”

“The 11th D2T Symposium” was held on September 21st, 2016 at Takeda Hall.

Under its main theme:” Design, fabrication, and test of heterogeneous systems”, the symposium had valuable lecturers by distinguished researchers invited from both overseas and domestic institutes, latest achievement reports by VDEC researchers, and a panel discussion by the lecturers and guest panelists.

The invited lecturers were Professor Anthony Walton (The University of Edinburgh) and Professor Kwang-Ting Cheng (Hong Kong University of Science and Technology). Two visiting professors (Professor Krishnendu Chakrabarty and Professor Stewart Smith) also gave lectures on their recent research activities. At the panel discussion, Professor Hiroyuki Fujita (Institute for Industrial Science, The University of Tokyo) kindly served as the moderator to conduct the active discussions with the theme of “Breakthrough technology and application of heterogeneous micro/nano systems for industrial/economic success.”

We sincerely appreciate every participant for their contribution at the symposium. We look forward to seeing many participants at the next symposium again.

11th D2T Symposium program

10:00	**Opening Remarks** Kunihiro Asada (Director, VLSI VDEC, The University of Tokyo) Takashi Sekino (Vice President, Nanotechnology Business, ADVANTEST Corporation)
10:15	**Session 1** (Chairman: Yoshio Mita, The University of Tokyo) *"Design and Test of Micro-Electrode-Dot-Array (MEDA) Digital Microfluidic Biochips"* Krishnendu Chakrabarty (Duke University, VDEC, The University of Tokyo) *"IMPACT - Implantable Microsystems for Personalised Anti Cancer Therapy"* Stewart Smith (The University of Edinburgh, VDEC, The University of Tokyo)
11:45	**Lunch**
13:15	**Session 2** (Chairman: Tetsuya Iizuka, The University of Tokyo) *"Experimental Demonstration of Cancelling Systematic Variation for free-Calibration Stochastic ADC"* Nguyen Ngoc Mai Khanh (VDEC, The University of Tokyo) *"A new method for measuring alias-free aperture jitter in an ADC output"* Takahiro J. Yamaguchi (ADVANTEST Laboratories, VDEC, The University of Tokyo) *"Power Supply Impedance Emulation Technique for ATE Device Power Supply"* Masahiro Ishida (ADVANTEST Corporation, VDEC, The University of Tokyo.) *"High-throughput and high-accuracy electron-beam direct writing"* Rimon Ikeno (VDEC, The University of Tokyo)
14:45	**Coffee Break**
15:15	**Session 3** (Chairman: Toru Nakura, The University of Tokyo) *"Options for the integration of technologies with CMOS Integrated Circuits"* Anthony J. Walton (The University of Edinburgh) *"3D Integrated CMOS-Memristor Hybrid Circuits: Devices, Integration, Architecture, and Applications"* Kwang-Ting (Tim) Cheng (Hong Kong University of Science and Technology)
16:35	**Break**
16:45	**Panel Discussion** Theme: *"Breakthrough technology and application of heterogeneous micro/nano systems for industrial/economic success"* Moderator: Hiroyuki Fujita (Institute of Industrial Science, The University of Tokyo) Panelists: Anthony Walton (Edinburgh University) Kwang-Ting Cheng (Hong Kong University of Science and Technology) Krishnendu Chakrabarty (Duke University, The University of Tokyo) Stewart Smith (Edinburgh University, The University of Tokyo)
18:00	**Closing**
	Reception

2.3 Research Activity Reports of "ADVANTEST D2T Research Division"

Fine Resolution Analog-to-Digital converter based on Stochastic Comparators

Nguyen Ngoc Mai-Khanh, Rimon Ikeno, Takahiro J. Yamaguchi, Tetsuya Iizuka, Kunihiro Asada

This research is to implement a fine-resolution sub-ranging analog to digital converter (ADC) circuit based on stochastic comparators.

Process variations together with many factors such as variations on voltage or temperature lead to mismatched design parameters that produce input-referred offsets and hence cause non-linearity and missing output codes of an ADC. Instead of making an effort to suppress such process variations as conventional ADC, the stochastic ADC approach exploits process variations based on the Gaussian distribution assumption of comparator voltage offset.

A layout strategy is proposed to reduce systematic variation and achieve Gaussian offset distribution with a reasonable number of comparators. A measurement setup for differential signals and low noise is performed. In addition, several types of modified differential comparators are invested and measured. Several measured results demonstrated the relationship of number of comparators and the effective resolution LSB of stochastic ADC. These results are helpful for a design-guide of the tradeoff between the numbers of comparator elements, the required LSB resolution, die area, and power consumption for the fine-resolution stochastic ADC approach.

Power Integrity Evaluation Method

Masahiro Ishida, Naoki Terao, Akira Matsukawa, Rimon Ikeno, Toru Nakura, Tetsuya Iizuka, Kunihiro Asada

While a required power supply voltage has become lower due to the advanced miniaturization of the semiconductor process, the power supply current consumed by a semiconductor device has increased because of the huge number of transistors integrated on a single chip. It may increase the power supply noise, and power integrity issues of the device under test in both an ATE and a practical operating environments. The purposes of this research project are to develop a power delivery network modeling method for evaluating power integrity at on-chip power supply nodes in semiconductor devices and a new power integrity control method which is based on the feedback operation.

This year, for the power delivery network modeling, we have investigated an algorithm for calculating an impedance model of the on-chip power delivery network based on the measurements of voltages and currents at the power supply pins of the device while loading a current at the on-chip power supply node, and evaluated its feasibility by using computer simulations. For the power integrity control method, we have developed extended methods of the previously proposed feedback-based power supply characteristic emulation to 1) a multiple power supply pin control, 2) a correction of the compensation current source characteristic, and emulation of serially connected impedance models, and demonstrated the concept and feasibility of the extended methods by computer simulations and experiments with an actual hardware including an FPGA.

High-throughput and high-accuracy electron-beam direct writing (EBDW) strategy for wide range of EBDW applications

Rimon Ikeno, Yoshio Mita, Kunihiro Asada

Maskless lithography by Electron-Beam Direct Writing (EBDW) lithography is expected as a low-cost and short turn-around time (TAT) lithography technology, but it also has some drawbacks like low process throughput and low accuracy against the intended layout shapes. We are pursuing high-speed and high-accuracy EBDW strategy utilizing Character Projection (CP) method to overcome these concerns and to boost EBDW use in arbitrary fields like MEMS, photonics, and so on.

In this year, we applied our high-throughput and high-accuracy EB exposure strategy by combination of CP and Variable-Shaped Beam (VSB) methods to practical device structures like optical wave guides, and investigated the shot-count reduction capability and resultant line-edge roughness (LER) utilizing Atomic Force Microscopy (AFM) for precise resist shape

observation and analysis. We also conducted numerical analysis of chip temperature during EB exposure process to optimize conditions of resist baking, resist development, and exposure processes.

2.4 Publications

Journal papers

[1] Masahiro Ishida, Toru Nakura, Takashi Kusaka, Satoshi Komatsu, and Kunihiro Asada, "Dynamic Power Integrity Control of ATE for Eliminating Overkills and Underkills in Device Testing," Journal of Electronic Testing: Theory and Applications, vol. 32(3), pp. 257-271, 2016.

[2] Rimon Ikeno, Satoshi Maruyama, Yoshio Mita, Makoto Ikeda, and Kunihiro Asada, "Electron beam lithography with character projection technique for high-throughput exposure with line-edge quality control," Journal of Micro/Nanolithography, MEMS, and MOEMS, 15(3), 31606, 2016.

[3] Masahiro Ishida, Toru Nakura, Takashi Kusaka, Satoshi Komatsu, and Kunihiro Asada, "Power Supply Voltage Control for Eliminating Overkills and Underkills in Delay Fault Testing," IEICE Transactions on Electronics, vol. E99-C, no. 10, pp. 1219-1225, October 2016.

International Conferences, Symposiums, Workshops

[1] James S. Tandon, Satoshi Komatsu, Takahiro J. Yamaguchi, and Kunihiro Asada, "A comparative study of body biased time-to-digital converters based-on stochastic arbiters and stochastic comparators," IEEE 2016 14th IEEE International New Circuits and Systems Conference (NEWCAS 2016), June 2016.

[2] Takahiro J. Yamaguchi, Katsuhiko Degawa, Tetsuya Iizuka, and Kunihiro Asada, "Common pitfalls in application of a threshold detection comparator to a continuous-time level crossing quantization," 21st International Mixed-Signal Testing Workshop (IMSTW 2016), July 2016.

[3] Toru Nakura, Naoki Terao, Masahiro Ishida, Rimon Ikeno, Takashi Kusaka, Tetsuya Iizuka, and Kunihiro Asada, "Power Supply Impedance Emulation to Eliminate Overkills and Underkills due to the Impedance Difference between ATE and Customer Board," International Test Conference 2016, November 2016.

[4] Nguyen Ngoc Mai-Khanh, Rimon Ikeno, Takahiro J. Yamaguchi, Tetsuya Iizuka, and Kunihiro Asada, "Experimental Demonstration of Stochastic Comparators for Fine Resolution ADC Without Calibration," 2016 IEEE International Conference on Electronics, Circuits, & Systems (ICECS), December 2016.

[5] Rimon Ikeno, Yoshio Mita, and Kunihiro Asada, "Line-edge quality optimization of electron-beam resist for high-throughput character projection exposure utilizing atomic force microscope analysis," SPIE Advanced Lithography 2017, 10148-33, March 2017.

[6] Stewart Smith, Yudai Takeshiro, Yuji Okamoto, Jonathan G. Terry, Anthony J. Walton, Rimon Ikeno, Kunihiro Asada, and Yoshio Mita, "Test Structures for Nano-Gap Fabrication Process Development for Nano-Electromechanical Systems," 30th International Conference on Microelectronics Test Structures (ICMTS 2017), 9.4, March 2017.

[7] Naoki Terao, Toru Nakura, Masahiro Ishida, Rimon Ikeno, Takashi Kusaka, Tetsuya Iizuka, and Kunihiro Asada, "Extension of Power Supply Impedance Emulation Method on ATE for Multiple Power Domain," to be presented at 22nd IEEE European Test Symposium, May 2017.

Domestic Conferences, Workshops, etc.

[1] Rimon Ikeno, "Analysis of IR-drop influence on at-speed test quality," 75th FTC Workshop, July 16th, 2016.

[2] Naoki Terao, Toru Nakura, Masahiro Ishida, Rimon Ikeno, Takashi Kusaka, Tetsuya Iizuka, and Kunihiro Asada, "Emulation of Power Supply Impedance for LSI Testing," 2017 IEICE General Conference, A-1-3, March 23rd, 2017.

Chapter 3 Research in VDEC

Asada, Nakura and Iizuka Laboratory

(http://www.mos.t.u-tokyo.ac.jp)

Supply Fluctuation Monitoring, Analysis and Reduction Method

Kunihiro Asada, Toru Nakura, Tetsuya Iizuka, Masahiro Kano

As miniaturization of semiconductor process increases, a resonant power supply noise due to parasitic impedance on power supply lines and parasitic capacitance of a core circuit has become a serious problem in designing mixed signal SoCs.

Passive decap is one of the most popular method used for resonant power supply noise suppression, however, this requires large silicon area for large capacitance. Then, we focused on the active charge injection method in order to realize both noise reduction and silicon area reduction. For the active charge injection, there are 2 approaches. One is capacitor-based approach charging and discharging the capacitors with a higher supply voltage, and the other is resistor-based approach directly extracting the charge from a higher supply voltage through the pass transistors. We analyzed both approaches under certain assumptions and designed the circuits (voltage drop detector, injection controller circuit and canceling capacitor/resistor circuit) to realize the analyzed charge injection. From the measurement results of the real silicon chips, we realized 14% and 24% noise reduction by using capacitor-based and resistor-based approach, respectively. Also, the proposed circuit using resistor-based approach consumes only 10% silicon area compared with MOS capacitors for the same amount of noise reduction.

However, more accurate model and the feedback control realizing it are required for more robust system.

LSI Test and Improved Reliability in Ultra-Fine Process Technologies

Kunihiro Asada, Toru Nakura, Tetsuya Iizuka, Akira Matsukawa, Toshiyuki Kikkawa, Takashi Toi, and Meikan Chin.

As miniaturization of semiconductor process increases, power supply voltage fluctuation due to its parasitic impedance has become serious concern. LSIs are tested after manufacturing process to see if it will work properly under customer's environment. Power supply impedance mismatch between testing environment and customer's environment, however, can potentially degrade reliability of the test.

We proposed power supply module for ATE which has an ability to change its parasitic inductance and capacitance using compensation current injection, so that it can emulate customer's environment, by which we can expect significant improvement of testing reliability. Experimental measurement results by prototype system showed that the voltage fluctuation waveform of the ATE was adjusted to that of the customer board, meaning that the impedance on the customer board was successfully emulated by the ATE.

As an expansion of this method, we proposed an application to the devices with multiple power supply pins using matrix operation. Also, we proposed the way to emulate not only the parameters of inductor or capacitor, but also arbitrary power supply network using nested-feedback digital filter and confirmed the concept by simulation.

PLL circuit with Time-Domain control

Kunihiro Asada, Toru Nakura, Tetsuya Iizuka, Keigo Tu, Tsukasa Kagaya

In this research, we have applied time-domain control methods to PLL circuit. A Pulse-Width Controlled PLL (PWPLL) is a new type of PLL whose oscillator is controlled by a pulse width.

In intermittent systems such as a variety of IoT devices, fast-locking PLL can reduce energy consumption as well as the latency time for system start-up. Therefore, the fast-locking method for PWPLL is proposed in the system where PWPLL refers and outputs the same fre-

quency.

For fast-locking, we adopt storing and reproducing measures for the phase and frequency-control code in the locked feedback system of PWPLL.

In order to realize this scheme, we add Time to Digital Converter (TDC), Digital to Time Converter (DTC), and other memory circuits to conventional PWPLL for storing phase and frequency-control code. When PWPLL gets started again after this series of the storing procedures, the stored values of phase and frequency-control code is set as initial values and as a result fast-locking is realized.The lock time of this fast-locking PWPLL has been proved to be 20~150 ns by simulations and 70 ns by measurements.

In order to make the PLL design simpler and take less time, we proposed an automatic design flow. Actually not all the PLLs could be designed automatically, this design flow is suitable for a ADPLL which is built by standard cells.

Nowadays, we have realized the design flow to synthesize parts of this ADPLL. In this design flow Both Verilog netlist and Spice netlist are automatically generated by script. Based on the netlist the layout and simulation are also engendered in this design flow. However, this flow only can design the DCO by set some parameters manually. In order to improve the automatic design more conveniently, we are working on generating all parameters from performance specificationautomatically.

Time Domain CDR and TDC Designs

Kunihiro Asada, Toru Nakura, Tetsuya Iizuka,
Meikan Chin, Ryuichi Enomoto

While digital circuits directly benefit from advanced process technologies, analog circuits suffer from negative effects such as small voltage headroom. Time-domain circuits, where analog signals are represented by digital signal edge transitions, could be a solution to the problem of analog circuits in a nanometer process.

Time-to-Digital Converter (TDC) is a representative example of time-domain circuits. The TDC converts a time interval between two rising edges into a digital code by using delay elements. In this research, we focus on pulse-shrinking TDC. In general, TDC has a trade-off between the time resolution and dynamic range, and the trade-off is particularly remarkable in the pulse-shrinking TDC. We proposed and designed a new TDC that improves the dynamic range while keeping the high resolution by using a hierarchical approach.

TDC can be applied for various applications and Clock and Data Recovery (CDR) based on Cycle Lock Gated Oscillator (CLGO) is one example. Since this CDR targets at serial communication systems which operate only intermittently, it is important that not only increasing power consumption rate in the operational state but also minimizing power consumption of stand-by state and maximizing the period of stand-by state by launching quickly. In this research, we proposed CDR based on CLGO using Delay Tunable Buffer and Vernier TDC which has same resolution, for increasing the data rate and decreasing the power consumption while keeping its quick start-up attribute.

Radiation Detector Utilizing Semiconductor Photodiode

Kunihiro Asada, Toru Nakura, Tetsuya Iizuka,
Yang Xiao, Kai Xu

Scintillation detectors and semiconductor detectors have received wide spread attention since they can specify the nuclide of radiation and estimate the arrival angle. Former research proposed a detector using the cube scintillator, SPAD (Single Photon Avalanche Diode) array image sensors, multi-coated materials, and pinholes and verified the method to detect the position of point light source inside the scintillator. We proposed a new method which calculated the track of photons to precisely estimate the position of light source. This method can cost less time to detect the light source position compared to the former research. The result of the simulation verified that by using this method the position of the light source inside the 1mm-size scintillator could be detected with a spatial resolution of 10 um-20 um in less than 0.3s. About the structures of SPADs we have tested, the p-well/deep-n-well with poly gate SPAD shows the lowest DCR. A 31x31 SPAD sensor featuring breakdown pixels extraction architecture for efficient data readout has been fabricated, and it's ability of capturing a short laser pulse has been proved by measurements.

Crosstalk Reduction on High Speed Communication Line

Kunihiro Asada, Toru Nakura, Tetsuya Iizuka,
Tokuhiko Nakasato

With the improvement of the circuit performance due to the miniaturization of the semiconductor process, the speed of transmission has been improving. The data rate necessary for applications also has been improving because UHD TVs and automobiles with a lot of electrical equipment was developed.

It is necessary to speed up transmission from both aspects of technology and demand, crosstalk is one of the factors hindering this. As measures for crosstalk, a circuit for reducing crosstalk at the receiving end was proposed in the previous research. In this research, we proposed a circuit with PD control circuit and time delay element based on the circuit in the previous research. Using simulation, we showed that the circuit can reduce crosstalk more effectively.

Surface magnetic field modeling for LSI security

Kunihiro Asada, Toru Nakura, Tetsuya Iizuka,
Nguyen Ngoc Mai Khanh, Yuki Oda

The modern VLSI systems that demand high reliability require carefully-designed power/ground network to provide stable power supply. Though the power supply connection is verified before tapeout, it is quite difficult to evaluate its actual quality and reliability after fabrication.

Using the measurement results of magnetic field emission from LSI, the proposed method estimates the actual current flow from the magnetic field measurement results, and enables us to find defects or design faults such as VIA/wire disconnections and/or current concentration with low cost.

Experimental result using an electromagnetic field simulator demonstrate that the proposed method precisely estimates the current flow in the supply network and clearly indicates the VIA fault location.

To verify the feasibility of the proposed method with actual measurement results, the test structure is designed and fabricated in 0.18 um 1P5M CMOS process. Current flow of power network in the chip was successfully estimated by actual measurement data.

UWB-IR Pulse Generators for Low Power Application

Kunihiro Asada, Toru Nakura, Tetsuya Iizuka,
Nguyen Ngoc Mai-Khanh, Parit Kanjanavirojkul,
Yudai Suzuki

Wideband pulse generation methods are studied, aiming at ultra-wideband impulse radio sensing applications in high frequency bands. In contrast to conventional feedback based switched-oscillator pulse generation, this work focused on excitation based pulse generation, in which the center oscillation frequency is not limited by CMOS's Fmax. Moreover, it feature quick-starting time and zero stand-by power. Two pulse generation techniques utilizing voltage-mode excitation and current mode excitation are proposed. The transmission line resonator is used in place of the lump LC resonator, such that the Q factor is highly increased and the modeling at high frequency is simpler. As a result the energy conversion efficiency of 3.13% is achieved at 12.5 GHz oscillation frequency in measurement. This is improved from conventional excitation type pulse generators, which have efficiency less than 1%. The prototypes are realized by CMOS chip flipped on the transmission line resonator on quartz substrate.

High-performance A-D Converters

Kunihiro Asada, Toru Nakura, Tetsuya Iizuka,
Takaaki Ito, Taiki Sugiyama

Analog-to-Digital Converters (ADC) are widely used as circuits which convert analog signal to digital signal. The purpose of this study is designing high-resolution ADCs which are used in circuits imitating neuron. These ADC need not execute high-speed conversion. However, each circuit component has thermal noise and non-linear distortion which should be eliminated for enhance ADC's resolution. Recently, we designed a SAR (successive approximation register) ADC with redundant bits for high resolution and low-power switching method.

Also, LSI process is getting smaller and design of analog circuits is becoming more difficult. Offset cancelling techniques and bigger circuits are used for ADC design to eliminate process variation and noise.

Another design approach is stochastic approach in which many comparators are driven in parallel. This emerging approach can be applied to level-crossing ADC and it is called level-crossing stochastic ADC.

We analyze input slope dependency of level-crossing stochastic ADC by circuit simulations. And we will measure the input slope dependency using the chip we designed manually.

Fujita Laboratory

(http://www.cad.t.u-tokyo.ac.jp/)

A New Approach for Debugging Logic Circuits

Masahiro FUJITA, Amir Masoud GHAREHBAGHI

Debugging logic circuits usually requires determining the new function for some internal nodes such that the circuit behavior becomes the same as the given specification. In this paper, we present a new approach for specifying the new function that focuses on finding the inputs to the new function instead of the function itself. First, we try to find the dependency of the new function to the primary inputs, if they are not known. Then, the internal nodes that are candidate of the inputs to the new function are selected. Finally, the inputs to the new function are determined. Both the primary input, and the internal nodes that are inputs to the new function are selected based on an iterative SAT solving procedure that guarantees the correctness of the solution. Our experimental results on ITC'99 benchmarks shows that our method can find the new function after debug in tens of SAT solver iterations even when the number of candidates are more than 1000.

Efficient Topological Matching Among Multiple Circuits

Masahiro FUJITA, Amir Masoud GHAREHBAGHI

Recognizing similarities and differences among multiple circuits is very useful for managing and maintaining IP libraries as well as merging circuits, fraud detection, reverse engineering, and redundancy checking. We address the problem of finding the maximum common subcircuit among two or more logic circuits. Given the gate-level netlists of the circuits, first we represent the circuits as graphs. Then, we try to find the largest common subgraph with a new approach based on signature generation and matching. In this work, we have introduced a new hash function for the signatures along with its efficient implementation that resulted in almost an order of magnitude faster matching compared to our previous work, for the large circuits. For example, Our experiments on IWLS2005 benchmark suite show that our method is able to find the perfect matching between two 160,000-gate IP in less than 30 seconds.

High-level description generation method for ECO and its application

Masahiro FUJITA, Amir Masoud GHAREHBAGHI, Qinhao WANG, Yusuke KIMURA,

In VLSI design, ECO (Engineering Change order) may happen after optimizing a gate-level circuit. In this case, designers may modify the gate-level circuit directly in order to preserve the optimization effort spent so far. In this research, we presented a method to generate a corresponding high-level description utilizing the modified gate-level circuit. Moreover, we presented a new equivalence checking method between a gate-level circuit and a high-level description.

Efficient Methods for Automatic Test Pattern Generation (ATPG) for Multiple Faults

Masahiro FUJITA, Amir Masoud GHAREHBAGHI, Conrad J. MOORE

Due to the continuous shrinking of semiconductor technology, there are more and more subtle errors or faults widely distributed in manufactured chips, and traditional "single" stuck-at fault model may become inappropriate. It is definitely better if all combinations of multiple faults can be completely tested. Although there are exponentially more multiple faults than single faults in any given circuit design, our previous works have shown that given an initial set of test patterns for single faults, relatively few additional tests are required in order to cover all multiple faults. In this work, the exact situations in which test patterns generated by ATPG for single stuck-at (SSA) faults do not detect multiple stuck-at (MSA) faults are examined. This will be done by presenting proofs which show the conditions that need to be met such that ATPG for single faults can cover all multiple faults. An analysis is then performed to determine the exact conditions that, when removed from the circuit, violate the assumption that ATPG for single faults will detect all multiple faults. Finally, we have proposed ATPG algorithm which detects up to double stuck-at (DSA) faults. Our experiments show that with the proposed methods, only a

small number of double faults have to be considered explicitly for test generation, as all the remaining ones are already covered by the test patterns for single fault.

Communication Aware Compiler for Reconfigurable Processors

Masahiro FUJITA, Amir Masoud GHAREHBAGHI, Qinhao WANG, Lu YI, Tomohiro MARUOKA

Program optimization on highly parallel systems is considered a hard work almost with experts doing much of performance tuning by hand. In addition, with the transistor size development, in deep submicron technology, the interconnection latency of inter-core data transfer now become

dominating the system latency. These problems cause many-core system performance still underutilized in many scenarios. In this work, we propose an integer linear programming(ILP) based method to analysis and optimize program data flow graph on a mesh-structured processors array. The proposed model includes interconnect-aware function unit binding and mapping. as well as data transformation routing. With this formal and flexible ILP based formulation, we got the optimized binding, mapping and routing result for specific program on target architecture. This ILP based formulation can be used for high level ECO while do high level synthesis, as well as estimate the FU binding on software defined system.

Partial C Program Synthesis

Masahiro FUJITA, Yusuke KIMURA

This research targets the method to synthesize a C program using so-called a "template" which is a C program including vacant places, and some use-cases. CEGIS (Counter Example Guided Inductive Synthesis) is utilized and our experimental results show that small number of use-cases are enough to synthesize the C program.

Narrowing Down Candidates of Electrical Bugs Using Trace Buffers

Masahiro FUJITA, Amir Masoud GHAREHBAGHI, Kentarou IWATA

As VLSI becomes denser, placing and routing become more difficult. In these circumstances, there is the case that the function is correctly designed, however, outputs are wrong in a real chip. This is caused mainly by electrical bugs, which are caused by electrical factors. It is difficult to reproduce them because their occurrence depends on operating history and conditions. Thus, debugging them is very time-consuming. To address such problems, trace buffers which are on-chip memories are used to record values of some flip-flops. Some untraced flip-flop values are restored from them. Using recorded and restored values, we try to narrow down candidates of electrical bugs by checking exhaustively whether there is possibility that electrical bugs can be occurred at each flip-flop and at each cycle.

Acceleration of Neural Network with FPGA

Masahiro FUJITA, Amir Masoud GHAREHBAGHI, Tomohiro OKAMOTO, Masato NEISHI

Dedicated hardware is generally faster and more energy-efficient than a general hardware. A circuit optimized for specific calculation can be obtained without chip fabrication using a Field Programmable Gate Array (FPGA), which is a programmable circuit. In this work, we have considered acceleration of simulation of neural networks with multiple FPGA chips. Neural network is a mathematical model of the mechanism of a brain. We implemented a highly pipelined circuit on a FPGA to simulate the network composed of 768 spiking neurons and we could achieve 93x faster operation than real-time brain on single FPGA. Furthermore, we have proposed partitioning of neurons among multiple FPGA chips that are connected through a ring network. Our proposed method is able to distribute the operations of 7,400 (= 768 * \sqrt{93}) neurons among 93 FPGA chips connected through a ring network such that the operation of the neural network is performed at the speed of a human brain.

Mapping and routing method for the FPGA which has wires between only neighbor blocks

Masahiro FUJITA, Tomohiro MARUOKA

As the integration degree of FPGA increases, FPGA becomes faster and its cost becomes lower, but the timing closure problem has become a major problem. Therefore, to prevent the problem, we consider the FPGA model which has wires between only neighbor blocks. In this research, we propose the method of mapping and routing on the FPGA model by formu-

lating constraints on mapping and routing as Integer Linear Programming (ILP) program. Since we could not get a solution in a short time only by the ILP method, we tried to divide a circuit and apply the ILP method to get an acceptable solution in a short time. We simulated mapping and routing for some benchmark circuits on the FPGA model, and it became possible to implement it with a practical number of cycles in small circuits.

Takamiya Laboratory

(http://icdesign.iis.u-tokyo.ac.jp/)

Energy Efficient Design for IoT Devices

Makoto Takamiya and Takayasu Sakurai

Requirements for IoT sensor nodes, wearable healthcare devices, and implanted medical devices are the wearing-unconsciousness and the maintenance-free operation. To enable the wearing-unconsciousness, mechanically flexible or small-size devices with the wireless connection are required. To enable the maintenance-free operation, energy autonomous devices are required. The energy autonomy is achieved by both the energy efficient operation and the energy harvesting.

Large Area and Flexible Electronics with Organic Transistors

Makoto Takamiya, Takao Someya, and Takayasu Sakurai

Large area electronics is a new frontier in electronics where intelligent electronic devices are distributed on a flexible surface, 10 cm to 10 m on a side, for the human interface and the comfortable daily life. Flexible and low-cost organic FETs (OFETs) are suitable for large-area electronics and have great potential as a supplement of solid and expensive silicon MOSFETs for VLSI's. We have proposed and demonstrated several large area and flexible applications including a surface electromyogram measurement sheet for prosthetic hand control, a flexible wet sensor sheet for biomedical applications, and a fever alarm armband.

Ikeda Laboratory

(http://www.mos.t.u-tokyo.ac.jp)

Current Research Projects

High-performance Cryptographic Engine Design

M. Ikeda, H. Awano, T.Ikeda, T. Ichihashi, R. Saito, K. Koga, and F. Arakawa

We have designed scalable multi-operation general purpose cryptographic processors, whose circuit area and operation times are tunable over a wide range of values using implementation parameters. One of the configurations, synthesized using 65 nm SOTB CMOS library, with a circuit area of 638k gates, can execute an elliptic curve scalar multiplication operation in just 0.16 ms. We have also studied area efficient implementation of Elliptic Curve Digital Signature Algorithm (ECDSA) signature generation / verification. Based on synthesis over 65 nm SOTB CMOS, we have established the relationship between area and processing time for various sets of coordinate systems, algorithms, and radices, which acts as a quantitative guideline for selection of methods towards area-efficient implementation. We have also studied cryptographic processing engine for high-speed extension field calculation.

Self-Synchronous System based on Dynamic Circuits

M. Ikeda, and Y. Kim

In this research, we investigated the low voltage operating characteristics of Differential Cascode Voltage Switch Logic (DCVSL), a dynamic circuit used in construction of completely asynchronous circuits, parameterized by the number of inputs. We evaluated by performing measurements on a SOTB 65 nm CMOS chip, with 2 to 6 input transistors optimized for low voltage operation, with operating voltage limit, power consumption, delay and power delay product as performance indices. This research aims at aiding a more efficient realization of low power operation dynamic circuits.

3D-range finding and Secure Sensing by Smart Image Sensors

M. Ikeda, T. Kikkawa, E. Kume, U. Kim, V.G. Vishwa, N. Toyoshima, and M. Tanibuchi

We are trying to propose new methods for 3-D mea-

surement, with advanced functionality, and secure sensing.

In 3-D measurement, we have proposed a new method with the capability of selective light detection and background suppression, and studied a new circuit with in-pixel polarized information acquisition.

In secure sensing, we are studying strong and light weight sensor data security scheme involving novel architecture at circuit level. We have proposed an interference attack method against phase shift method and also proposed a method of protection against the attack. We have also studied pixel parallel analog front-end architecture for THz imaging.

Mita Laboratory

(http://www.if.t.u-tokyo.ac.jp)

Programmable Matter - Study on LSI-MEMS energy-autonomous distributed microsystems for realization of deformable matter

Y. Mita, N.Usami, J.Bourgeois,
B.Piranda (FEMTO-ST, France),
S. Delalande (PSA-Peugeot)

As one example of integrated MEMS that is expected to open new research and industrial application fields, the authors are trying to show a top-down application of energy-autonomous distributed microrobots. A number of identical tiny robots, sized below 1 cm, will be released in an environment. Individual robot can communicate with their neighbor, can stick each other, can share energy, to realize cooperative function. The PI has received a French National Research Center (ANR) grant on behalf of host professor of CNRS laboratory in the Institute of Industrial Science (LIMMS, CNRS-IIS, UMI 2820), together with FEMTO-ST Laboratory and PSA-Peugeot Laboratory for such "micro robots that can realize deformable substance by cooperative action, named Programmable Matter". Target is set in understanding on physics and devices working in aqueous environment.

Top-down fabrication of small-gap electrode devices by Fine E-Beam writing and MEMS process

Y. Mita, Y.Takeshiro, N.Washizu, A.Takada,
M. Fujiwara, T.Sawamura, R.Ikeno, and K. Asada

Towards the goal of production of brand-new sensor devices with higher sensitivity and functionality, the team is working on small-gap electrode fabrication process. The team takes full advantage of newly-acquired (in 2013) rapid electron beam writer F7000S-VD02. The capability of high electron dose and sharp edge due to cell (character) projection machine configuration is used for fabrication process. The target of first year is reliable sub 100 nm gap electrode fabrication, as well as microactuator-integrated nanogap system.

University-Industry collaborative research on highly-functional system by MEMS post-process of CMOS-VLSI

Y. Mita, K.Tohyama, Y.Nakayama (Konica Minolta),
M.Takiguchi (Sony), Y.Sato (Nanox Japan)

The research targets are new sensor devices, made by post-process at clearnrooms such as VDEC Takeda Supercleanroom and others, of VLSI wafer made through VDEC. The important finding has been that VLSI wafer acquired just after transistor fabrication could sustain processes even with heat treatment, such as deposition, ion implantation, and drive-in. In 2016, a VLSI device made on Silicon-on-Insulator (SOI) wafer was successfully Deep-RIE processed. The industrial interest is its versatility–many different types of application devices, which differ one from another according to request of market, can be fabricated by using the same technology. More and more companies are interested in the scheme and are working on the technology on the collaborative research projects.

LSI hot-spots active cooling system

Y. Mita, Y. Okamoto, K. Fujimoto (Titech),
H.Ryoson (Titech), and T. Oba (Titech)

A hotspot, which is referred to a high-temperature area due to the overheating of a circuit block that excess passive cooling capability, is becoming a key limiting factor of LSI performance. An active cooling system that tries to actively remove such local heating by circulating liquid coolant is our research target. In FY2016, an out-of-plane cooling scheme was confirmed to be efficient for heat removal, by test structure experiments, modeling with equations, and finite element method simulations.

Assessment of through-the-chip backside Focused Ion Beam (FIB) process to transistor characteristics

Y. Mita, N.Usami, J.Kinoshita (Toyotsu Electronics Van Partners), R. Ikeno, Y. Okamoto, and K. Asada

VDEC acquired a new Focused Ion Beam machine FEI V400ACE in FY 2013, due to supplemental national budget decided in 2012. The machine can make through-the-chip etching of VLSI, with capability of dual-side alignment of infrared (IR) camera and CAD data. The research aimed at assessing an impact of such through-the-chip FIB process on transistor characteristics. The result revealed a necessity of composing both high-speed (but less precise) and low-speed (but more precise) etching recipes to minimize transistor characteristics change.

An LSI probing system with CMOS-MEMS

Y. Mita, R.Setoguchi and Y. Okamoto

The team is developing a "MEMS" probe card for electron device testing such as VLSI. The originality is to integrate CMOS circuit to provide high functionality. In the year 2014, a piezo-resistive stress measurement circuit was developed to quantify real stress put on the probe. A company-made polysilicon resistor, made by post-processing commercial CMOS 0.6 μm 1P2M circuit, was integrated into cantilever and responded to the stress with good gauge factor (around 20). The technology has been standardized and could be applied to other groups'research work. Also, to have reliable microprocess, a test structure to visualize end-point of Deep-RIE process is developed.

Right-brain-computing integrated circuits: associative processing systems

N.Yamashita, Y.Mita

Digital computers are dedicated machines for vary fast execution of numerical calculations. However, their performance is extremely poor in such tasks like seeing, recognizing, and taking immediate actions, which are effortless tasks in our daily life. This research aims at building intelligent VLSI systems based on the psychological model of a brain. In our system past experience is stored as template vectors in non-volatile vast memories and the maximum-likelihood event to the current event is recalled in real time by a fully parallel processing. The key ingredient of the system is a new functional device called "Neuron MOS Transistor" (neuMOS or ν MOS) which mimics the action of a nerve cell neuron at a single transistor level. Based on such architecture that "association" is the very computing primitive, we are pursuing human-like intelligence system implementation directly in silicon integrated circuits. Currently research is in progress for robust image recognition and classification processing including robust feature extraction. The sate-of-the-art silicon technology has been utilized to implement such associative processors in both analog and digital CMOS VLSI chips, and was published.

"Zeolite-Electronics-Nanostructure (ZEN)" integrated chemical sensor

Y.Mita, K. Yamada, Y.Okamoto, M.Denoual (ENSI de Caen, France), Tixier Mita Agnès, Eric Lebrasseur, Hussein Awala (ENSI de Caen, France), Julien Grand (ENSI de Caen, France), Sveltana Mintova (ENSI de Caen, France)

One of the most important application field of MEMS is sensors that can detect physical and chemical amount that cannot be sensed by human beings. Following a long history of the group's research, the team was appointed in 2015 as a JSPS-CNRS bilateral cooperative research project grant. The goal of the research is to develop a chemical sensor by integrating Zeolite material that is new to VLSI, and applying post-process on it. Within one year, the team have successfully demonstrated two types of devices: a zeolite chemical sensor by resonant frequency shift detection, and by thermal capacity change detection according chemical concentration. A reliable embedding method of zeolite into 3D silicon MEMS trenches have been developed as well.

Development of shock resonant spectrum (SRS) sensor for cyber physical system

Y. Mita, R Ranga Reddy, N. Usami

VDEC is awarded a Japanese JST–Indian DST joint grant (SICORP) for cyber physical systems research, in cooperation with IIT Bombay campus. The team is participating the project through a Shock Resonant Spectrum (SRS) sensor, which has been a research theme of 2012-2014. A new Ph.D student from India is assigned and fabrication process was recovered.

Development of LSI post-processing for hybrid integration

Y. Mita, D. Lämmerer, A. Mizushima, E. Ohta,
N. Kondo, T. Momose (Material Eng.)

To provide new capability to Nanotechnology Platform Users, a couple of process technologies for LSI hybrid integration is under development. In FY2016, a stable gold electroplating system was purchased and a bump plating for LSI flip-chip bonding was developed. In parallel, a supercritical fluid deposition (SCFD) machine was restored to investigate trench embedding deposition with metal.

Takagi-Takenaka Laboratory

(http://www.mosfet.k.u-tokyo.ac.jp/)

III-V/Ge Metal-Oxide-Semiconductor (MOS) FETs

S. Takagi, M. Takenaka, Cai Weili, Yu Xiao,
WuKang Kim, Chang Chih-Yu, Ke Mengan,
Liao Chenyu, Aya Shimada

We have conducted the research on high-peformance III-V/Ge MOSFETs.

We have investigated InGaAs gate stack technologies by using La_2O_3/InGaAs MOS interfaces. We have shown that La_2O_3 deposted by ALD enable superior MOS interfaces for InGaAs. We have also fabricated extremeley-thin body Ge-on-Insulator MOSFETs by using wafer-bonded GeOI wafers. We have revealed the physical mechanism which degrades hole mobility in the ultra-thin Ge channel.

Tunnel FET

S. Takagi, M. Takenaka, Min-Soo Kim, Takahiro Gotow,
Daehwan An, Takumi Kato, Yoon Sanghee

We have investigated tunnel FETs (TFETs) which can exhibit steep subthreshold slope for low-power operation. Lateral InGaAs TFETs and GaAsSb/InGaAs hetro-junction TFETs have been explored. By growing GaAsSb/InGaAs hetrostructure by MBE, we have demonstrated vertical GaAsSb/InGaAs TFETs. We have also investigated Ge/s-Si TFET for high Ion operation.

Si CMOS photonics

M. Takenaka, S. Takagi, Y. Kim, J. Han, J. Kang,
K. Takeuchi

We have proposed Ge CMOS photonics platform by using wafer-bonded GeOI wafers on which Ge CMOS and Ge photonic-wire devices are monolithically integrated. We have successfully demonstrated Ge photonic-wire waveguide operated at mid-infrared wavelengths on the GeOI wafer. Optical modulation by carrier injection into the Ge waveguide was also demonstrated for the first time. For strained SiGe optical modulators, we have proposed MOS-based optical modulators fabricated by wafer bonding. We have established the void-less wafer bonding technology by using Al_2O_3/HfO_2 interfacial layer for wafer bonding.

III-V CMOS photonics

S. Takagi, M. Takenaka, Y. Chen, J. Park, S. Takashima,
N. Sekine

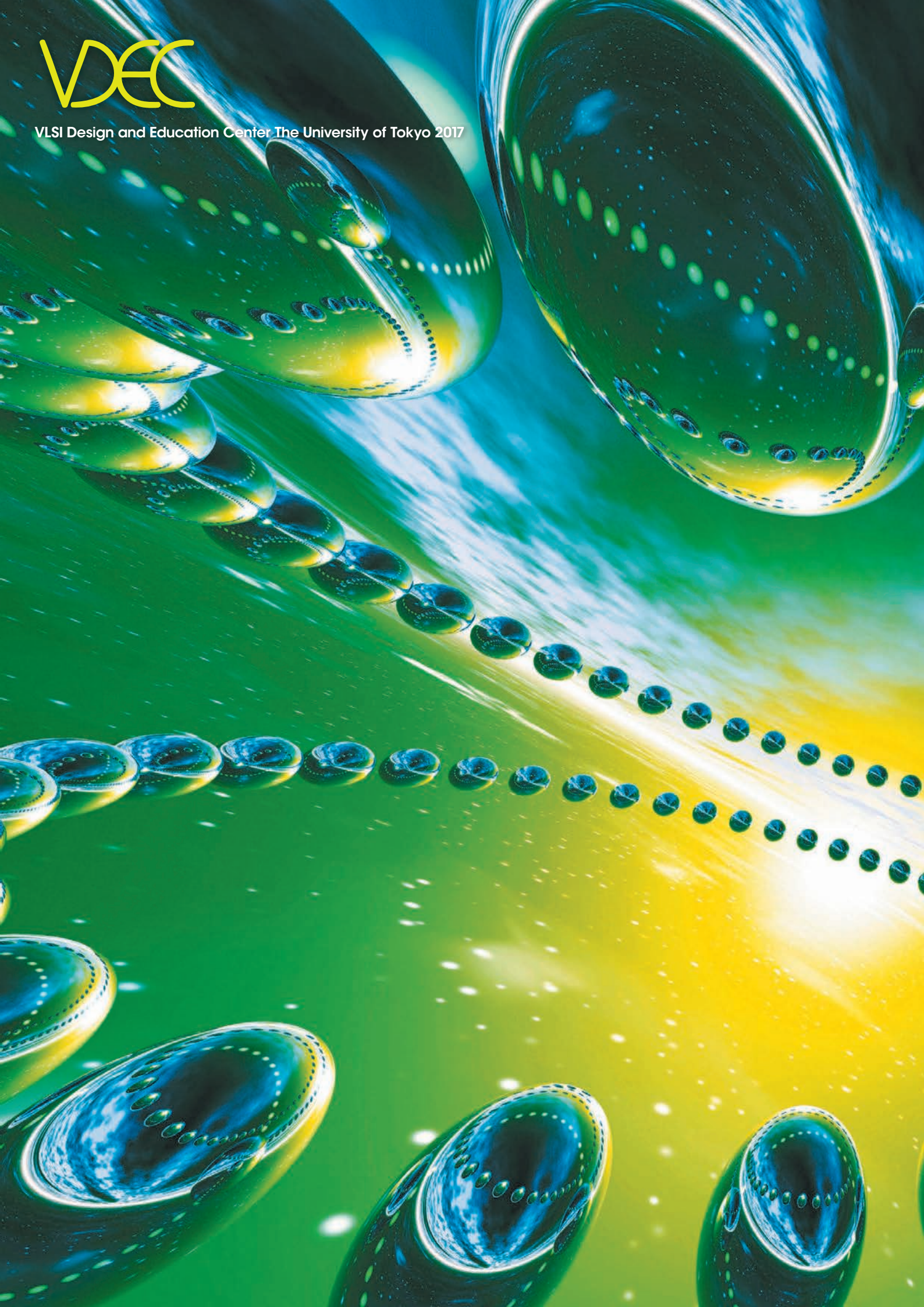
We have investigated the III-V CMOS photonics platform by using III-V on insulator wafer. On the III-V-OI wafer, III-V MOSFETs and III-V photonics can be monolithically integrated. We have successfully integrated an InP grating coupler with waveguide InGaAs photodetector (PD) on the III-V CMOS photonics platform. We have also revealed that a depletion-based InGaAsP optical modulator exhibits 4 times higher modulation efficiency than Si. We have also clarified the mechanism of quantum well intermixing on the III-V-OI wafer. In addition, the bandgap wavelength shift of more than 100 nm has been demonstrated, enabling active-passive integration on the III-V CMOS photonics platform.

VLSI Design and Education Center, The University of Tokyo
Annual Report

October, 2017

Published by
VLSI Design and Education Center, The University of Tokyo
Director Kunihiro Asada
Address: Yayoi 2-11-16, Bunkyo-ku, Tokyo, 113-8656, Japan

Printed in
Sanbi Printing Co., Ltd.
Address: Nishinippori 5-9-8, Arakawa-ku, Tokyo, 116-0013, Japan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VLSI Design and Education Center The University of Tokyo 2017