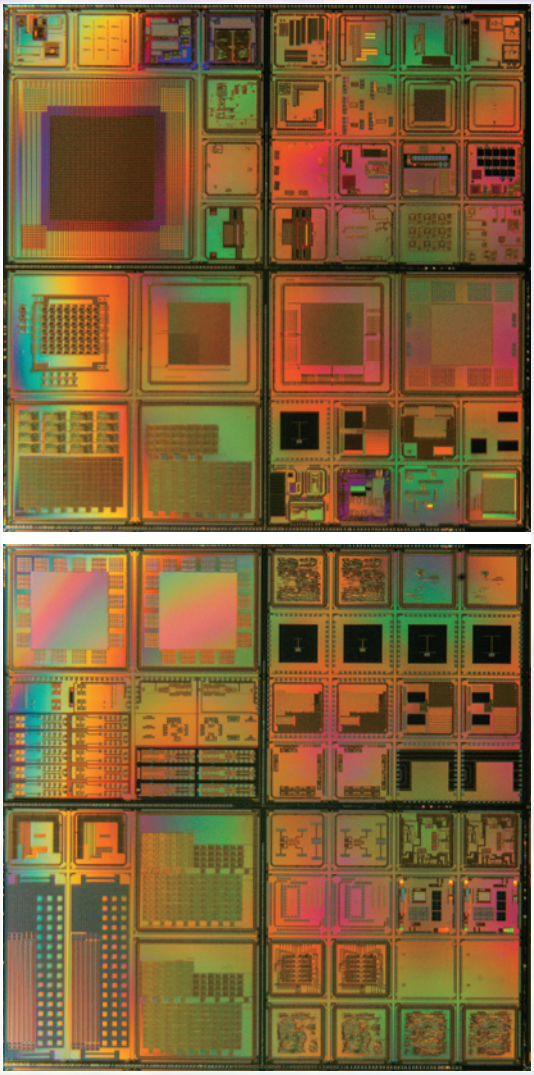
VDEC

平成30年度

東京大学
大規模集積システム設計教育研究センター
年報

2018
VLSI Design and Education Center, The University of Tokyo Annual Report



VLSI Design and Education Center
The University of Tokyo

I was appointed as director of VLSI Design and Education Center (VDEC) on April 1 following the director, Prof. Asada. VDEC was established in May 1996, and has been operating for 22 years. The first director, Prof. Hoh and the previous director, Prof. Asada have made VDEC as one of the most important and widely used organizations in Japanese academia for VLSI chip design and development. Annually around 300 research groups in academia use the design tools provided through VDEC, and nearly 200 research groups use various facilities including clean rooms and measurement tools for chip development.

Semiconductor industry has been continuously growing since the last century and is expected to continue to grow with the increasing need from IoT and related technology. It is extremely important to support academia as it is the basis of semiconductor industry. There are several organizations in the world, specifically in US, Canada, Europe, South Korea, and Taiwan, and others, whose goals are basically the same as VDEC. There have been efforts in the collaboration among these organizations. Every year, multiple meetings to discuss collaborative ways to supply various services for world-wide VLSI chip design and development are set up, and more intensive joint activities are expected to come.

D2T (Design to Test) which is an industry donated division in VDEC has been working for ten years and has received a number of world top-level visiting professors. D2T has already stimulated educational and research activities of VLSI testing in broad sense and has generated several results which have actually influenced the VLSI testing area world-wide. It is expected to continue to generate more influential results in VLSI design and testing.

VDEC is an essential organization for academic VLSI design and development. Now it is planned to expand to include not only just chip development, but also ICT system developments through tighter collaboration with various resources in information technology. With that goal in mind, VDEC continues to work for more efficient ways of chip and system developments, EDA tools which can be used commercial chips, and integration of VLSI chip and device developments. VDEC including myself appreciates your continuous support.

VLSI Design and Education Center, University of Tokyo
Director Masahiro Fujita
藤田昌宏

VLSI Design and Education Center, The University of Tokyo
Annual Report 2018

CONTENTS

Chapter 1 Activity Report of VDEC

1.1 Introduction of VDEC activities and activity report of FY2017

VLSI Design and Education Center(VDEC), University of Tokyo was established in May 1996. VDEC has been operating for the following 3 major roles: "spreading the latest information on VLSI design and education," "providing licenses of CAD tools," and "supporting on VLSI chip fabrications for academic use." The VDEC activity report of FY 2017 is described hereafter according to Fig. 1.1.

The missions of VDEC are for advancement of researches and education on LSI design in public and private universities and colleges in Japan and send many distinguished VLSI designers into industry. After 22 years of VDEC establishment, educations on CAD software, LSI design and design flow in universities have been well established. On the other hand, advancement on nano-meter CMOS technologies forces design flow and CAD software complicated. We have been continuing CAD tool seminar by the lecturers from EDA vendors for twice a year. We hold the seminar in VDEC and provide distance learning through video streaming. We expect spread of the up-to-date LSI design methodology by using CAD tools.

We assume our LSI design flow seminars as educations on basic LSI design concepts and practical experience of LSI design with CAD tool chain. VDEC holds "LSI design education seminar", a.k.a. VDEC Refresh Seminar, once a year. This year we hold 3 courses, "Analog design course" and "RF design course", and initiated "MEMS design course" in July-September time frame. We invite experienced professors among universities as lecturers for the courses to conduct LSI design education courses with practical experience. We also hold "Transistor level design flow in VDEC" and "Digital design flow in VDEC EDA environment" for designers in universities. We started to charge these two LSI design education courses, as well as VDEC Refresh Seminars.

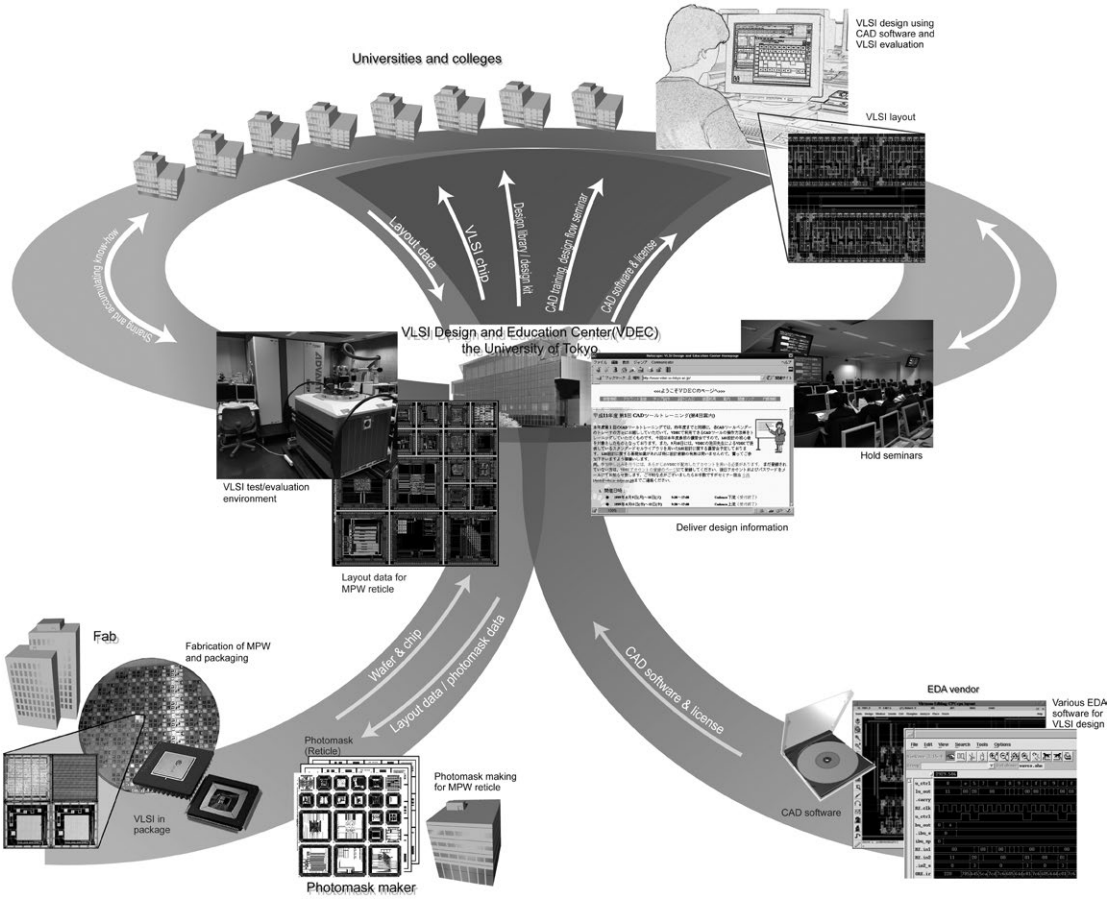


Fig. 1.1 VDEC activities

In addition to the above seminars, we hold "VDEC Designer'Forum" among young professors and students annually. This is a workshop that the participants exchange their design examples with not only success stories but also their failure stories, in addition to invited talks. We expect students and professors who will start designs to learn kinds of know-hows. We have initiated "IEEE SSCS Japan Chapter VDEC Design Award" this year, and final examination and awarding have carried out during the "VDEC Designer' Forum". Mr. H. Asano (Kobe Univ.) is awarded as "IEEE SSCS Japan Chapter VDEC Design Award" winner, and Mr. H. Asano (Kobe Univ.), Mr. K. Fujimoto (Nara Institute of Science and Technology), Mr. Y. Matsushita (Keio Univ.)) are awarded as "the best VDEC Design Award", and Mr. T. Yamaguchi (Nara Institute of Science and Technology), Mr. H. Hayami (Nara Institute of Science and Technology), Mr. H. Sun (Waseda Univ.) are awarded as the "VDEC Design Award." Also Mr. D. Terutsuki (Univ. of Tokyo) are awarded as the "VDEC Design Award."

LSI designers come up against various difficulties during actual LSI design scene, even after the basic educations through various seminars and the forum. One of the biggest problems for beginners is the setup of CAD softwares. Many of them also get confused by "Esoteric messages" come out from CAD softwares, even after they successfully setup CAD tools. In such situations, VDEC mailing-lists make significant contributions. VDEC users can register to VDEC mailing-lists on CAD tools, and process dependent groups through VDEC web pages, and can ask questions and helps on their facing issues. It is not a responsibility for the registrant of such mailing-lists to give answers to questions, however, in most cases, replies are given by the experienced users of CAD tools and experienced designers within a couple of hours to a couple of days. Moreover, emails are accumulated and are open to the VDEC users, as shown in Fig. 1.2, who have registered VDEC accounts, as the important educational assets. We expect all the VDEC users to make the full use of this mechanism to help solve problems.

We continue chip fabrication services on FDSOI CMOS 28 nm by ST Microelectronics, 0.18 mm CMOS by Rohm and 0.8 μm CMOS by On-semi Sanyo Semiconductor. And started chip fabrication services on SOTB CMOS 65 nm by Renesas Electronics.

Our donated division "Design To Test (D2T)", which was founded by donation from Advantest in Oct. 2008, focuses on enrichment of education on LSI testing and bridging between design and testing.

Fig. 1.3 shows trends of number of papers through VDEC activities. Number of papers is increasing, which means researches in the field of VLSI design have been encouraged after VDEC establishment.

Fig. 1.4 shows number of papers related to CAD usage, chip fabrications and VDEC facility usages. CAD tools are widely used to write papers. CAD tools are used not only chip designs themselves but also used for preparation of chip fabrication and they contribute to verify fundamental ideas of researches. Advanced CMOS processes are preferred for publications, and not only papers with 65 nm/40 nm CMOS chips, but also with 32 nm CMOS, 22 nm CMOS and 14 nm CMOS are emerging in the world. We would like to prepare chip fabrication services for the advanced CMOS processes. In addition, we would

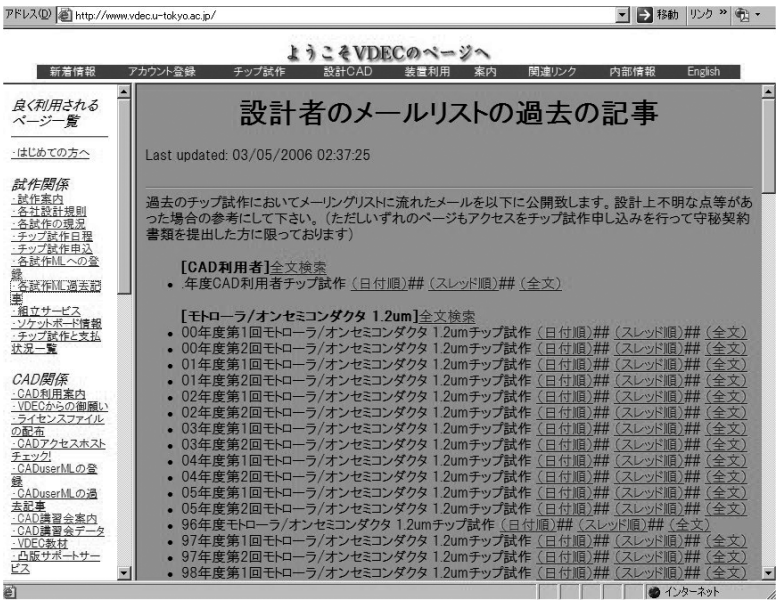


Fig. 1.2 Archives of emails of VDEC mailing-list.

like to setup chip fabrication services related to CMOS/MEMS to fulfill the researches for “More than Moore”. We also encourage researchers to fully use of VDEC facilities such like LSI testers, FIB systems and EB writer for the wide spread of research purposes.

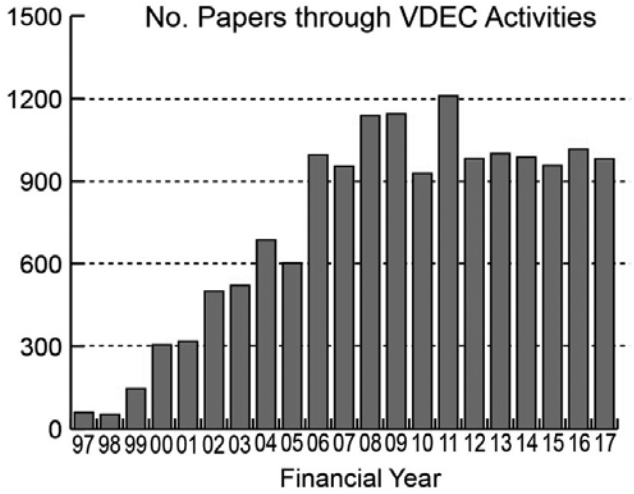


Fig. 1.3 Trends of number of papers through VDEC activities.

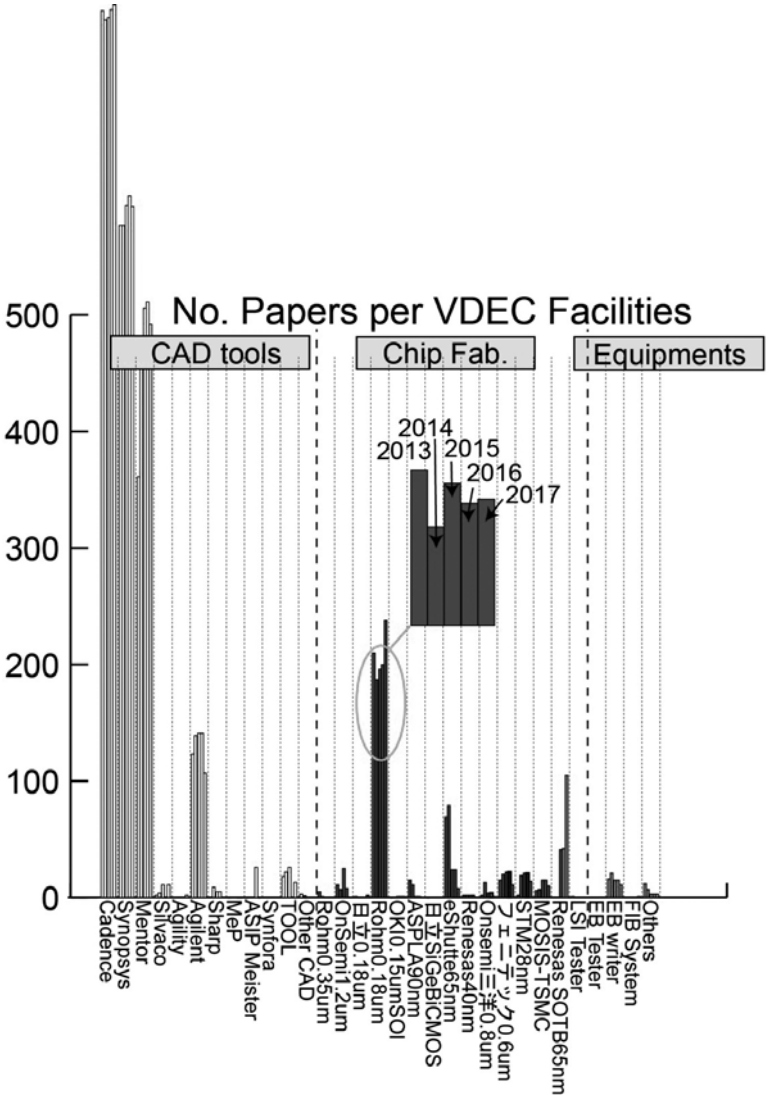


Fig. 1.4 Number of papers related to VDEC facilities.

1.2 VDEC CAD Tools

Since 1996, VDEC has provided CAD software licenses to the registered researchers in universities and colleges in Japan. The CAD tools we provided in 2018 are shown in Table.1.2.1. The researchers can use those CAD tools when their local machines, whose IP addresses are registered in advance, are authorized by one of VDEC license server located in the ten VDEC subcenters shown in Fig. re 1.2.1. For each CAD tool, VDEC provides 10-100 floating licenses. Those CAD tools can be utilized only for research and education activities in national universities, other public universities, private universities, and colleges.

When one is going to use VDEC CAD tools and chip fabrication service (the details are described in Section 1-3), some faculty member of his/her research group in a university or a collage needs to do user registration. Fig. re 1.2.2 shows (a) the number of registrants, (b) the number of distinguished universities/colleges of the registrants, and (c) the number of registrants who applied VDEC CAD tools, (d) the number of applied licenses of all CAD tools.

Table 1.2.1 VDEC CAD tools

Name	Function	Vendor
Cadence tool set	Verilog-HDL/VHDL entry, Simlation, Logic synthesis, Test pattern generation, Cell-based (including macros) place, route, and back-annotation, Interactive schematic and layout editor, Analog circuit simulation, Logic verification, Circuit extraction	Cadence Design Systems, Inc.
Synopsys tool set	Verilog-HDL/VHDK simulation, Logic synthesis, Test pattern generation, Cell-based (including macros) place, route, and back-annotation, Circuit simulation, Device simulation	Synopsys, Inc.
Mentor tool set	Layout verification, Design rule check	Mentor Graphics Co. Ltd.
Silvaco tool set	Fast circuit simulation	Silvaco
ADS/Golden Gate	Design and verification of high-frequency circuits	Keysight Technologies
Bach system	BachC-based design, synthesis, and verification	Sharp
LAVIS	Layout visualization platform	TOOL

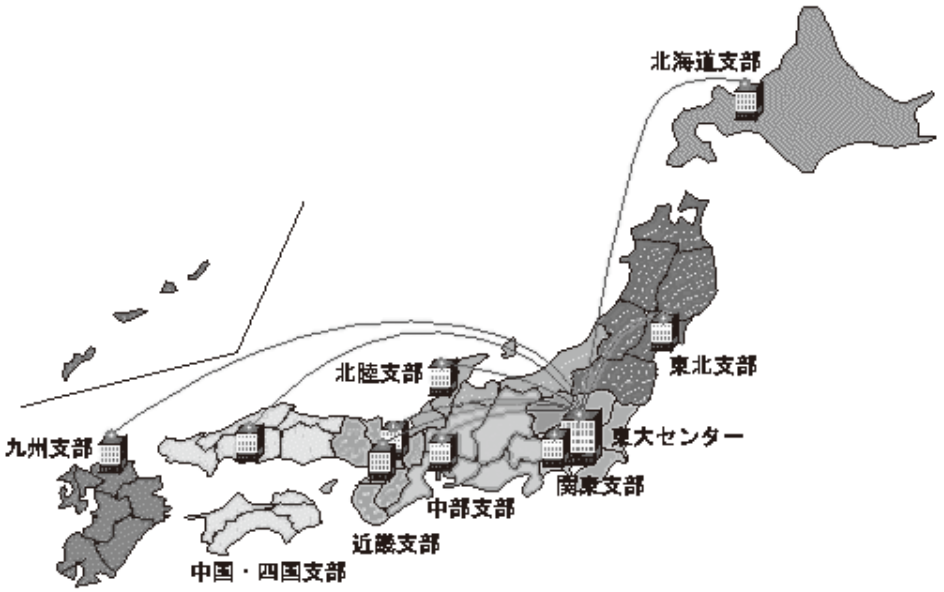
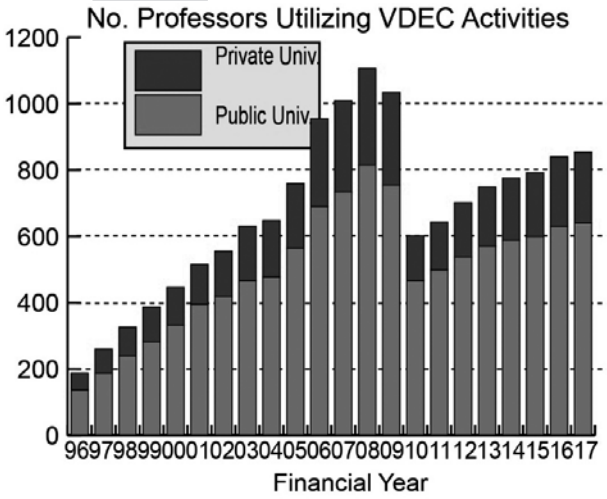
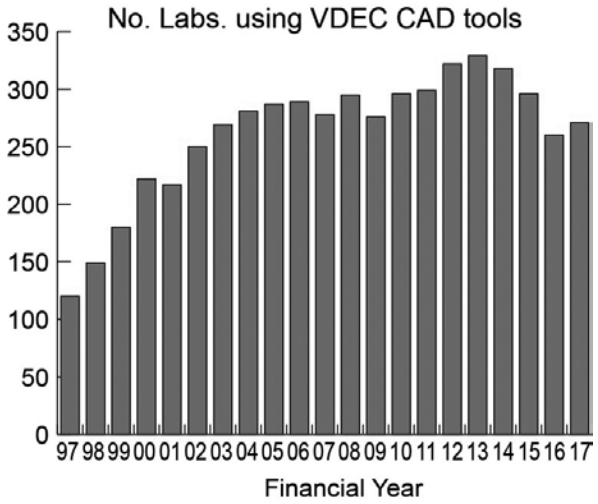


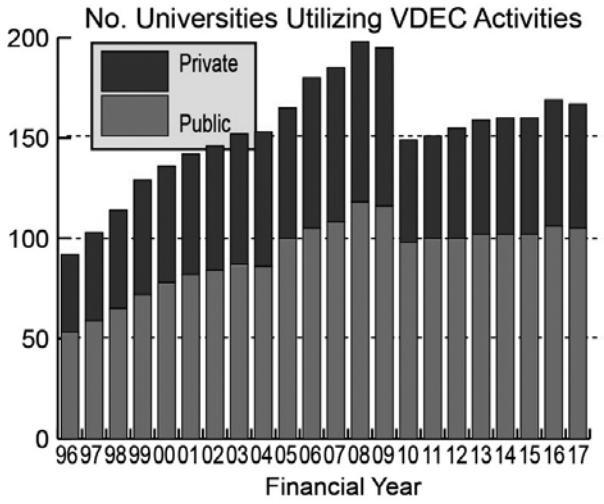
Fig. 1.2.1 VDEC Subcenters



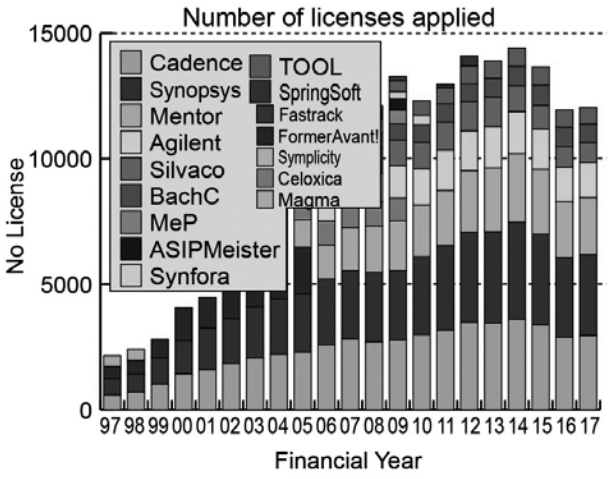
(a) The number of registrants



(c) The number of research group applied CAD tools



(b) The number of universities colleges of the registrants



(d) The number of applied licenses of all CAD tools

Fig. 1.2.2 The numbers of VDEC CAD Applications

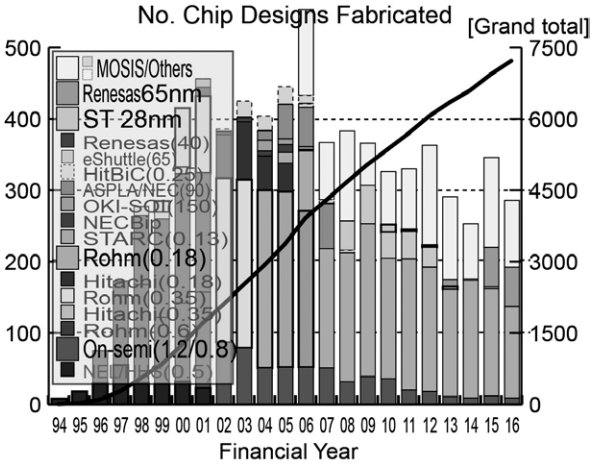
1.3 VLSI Chip Fabrication

1.3.1 Trends of VLSI Chip Fabrication Services

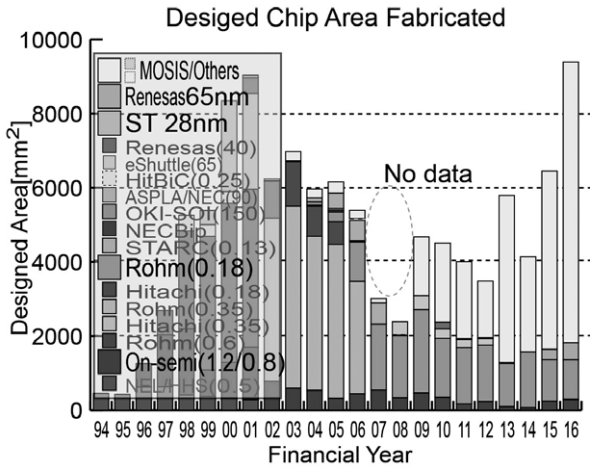
Fig. 1.3.1 shows a trend of number of designed chips for VDEC chip fabrication services, including pilot project prior to VDEC establishment.

VLSI chip fabrication is limited to 0.5 mm CMOS provided by NTT Electronics during the pilot project in 1994 and 1995. VDEC chip fabrication had started in 1996 with 1.2 mm CMOS provided by Motorola Japan, which is now On-Semiconductor as well as the 0.5 mm CMOS. In 1997, VDEC received cooperation from Rohm and has started 0.6 mm CMOS process. In 1998, VDEC started chip fabrication services of 0.35 mm CMOS by Hitachi, and in 1999, VDEC started 0.35 mm CMOS by Rohm. We had a test chip fabrication of 0.13 mm CMOS by STARC through "IP development project" in 2001. We added 0.18 mm CMOS by Hitachi into our chip fabrication menu in 2001. From 2002, we started VDEC-MOSIS chip fabrication program initiated by Prof. Iwata of Hiroshima University. Under this program, VDEC member can access to TSMC and IBM processes with lower price. We also started Bipolar chip fabrication by NEC Compound Semiconductor Devices. In 2004, we started 0.15 mm SOI-CMOS chip fabrication by Oki Electric as test chip fabrications. In the same year we started 90 nm CMOS chip fabrication by ASPLA/STARC. In 2006, we started 0.18 mm CMOS by Rohm and 0.25 mm SiGeBiCMOS by Hitachi. In 2008, we started 65 nm CMOS process by eShuttle, after closure of 90 nm CMOS chip fabrication in 2007. In 2010, we started 40 nm CMOS process by Renesas Electronics through "Next Generation Semiconductor Circuits & Architecture" project between METI and STAR. On the other hand, 1.2 mm CMOS chip fabrication program came to end by the September 2011. 40 nm CMOS by Renesas Electronics and 65 nm by eShuttle also come to end by Oct. 2012 and Aug. 2013, respectively. We started CMOS 0.8 μm in Oct. 2012 by On-semiconductor-Sanyo as a test chip fabrication and opened it as the regular chip fabrication menu in 2012. We started FD-SOI 28 nm CMOS by ST-Microelectronics through CMP, France, as the advanced CMOS process in 2013. We started SOTB 65 nm CMOS by Renesas Electronics in 2015. We initiated two more chip fabrication trials in 2017, on CMOS 0.6 um HV from Ricoh, and CMOS 40 nm from Mie Fujitsu.

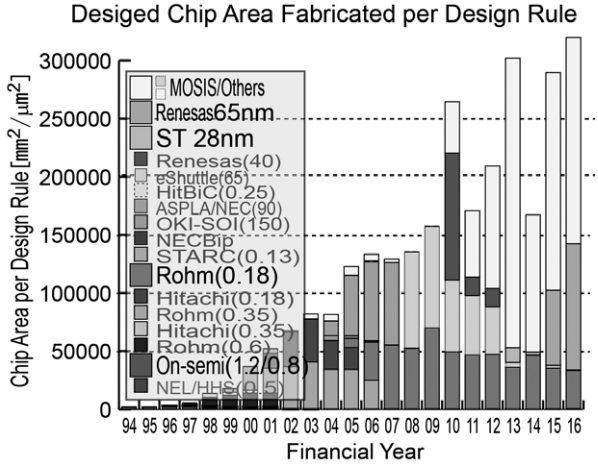
Fig. 1.3.1(a) shows trends of number of chip designed for VDEC chip fabrication. For the first 6 years until 2001, the number of designed chips shows steady increase, which means drastic improve of the effectiveness



(a) Trend of number of designs fabricated.



(b) Trend of designed area.



(c) Trend of designed area normalized by design rule.

Fig. 1.3.1 Trend of number of designs and designed chip area.

researches and education of LSI design, and we assume drastic increase of number of students related to LSI chip design and education. During few years of stable number around 400 chip designs per year, we can see transition of designs toward finer process. In 2007, we saw a large drop, which was caused by sudden process transition from 0.35 mm CMOS to 0.18 mm CMOS, and in 2008, we also saw another drop by process transition from 90 nm CMOS to 65 nm CMOS.

Fig. 1.3.1(b) shows trends of designed chip area, which shows much clear trends of drop by process migration. On the other hand, Fig. 1.3.1(c) shows trends of designed chip area normalized by design rule, which assume to be strong relation with design efforts. Coming from the fact that the normalized chip area is still growing, we assume the major reason for decrease of number of chips and designed area is increase of design effort per chip and per unit area due to process scaling.

Fig. 1.3.2 shows trends number of professors and universities fabricated chip. Number of professors who have contracted NDA for process technologies to access design rules and design libraries are, 83, 283, and 45, respectively, for 65 nm CMOS, 0.18 mm CMOS, and 0.8 um CMOS.

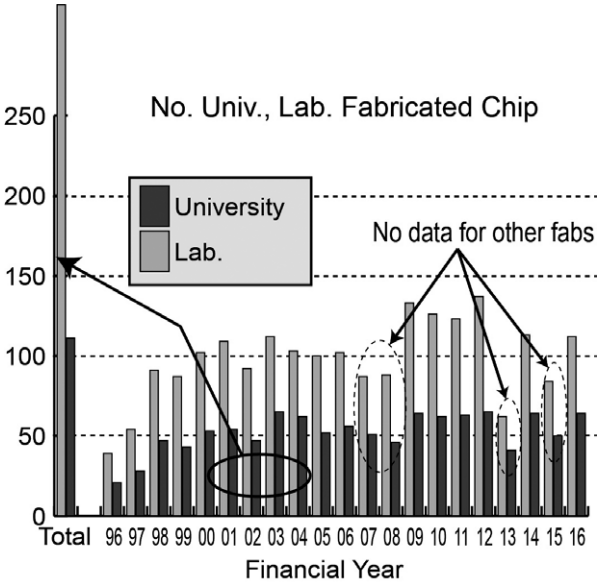


Fig. 1.3.2 Trend of number of processors and universities fabricated chip.

1.3.2 Overview of chip fabrication in 2017

Table 1.3.1 lists chip fabrication schedule in 2017. Please refer to list in Chapter 2 for details of designers and contents of chip designed.

Table 1.3.1 Chip fabrication schedule in 2017

○ 0.8 mm CMOS (On-Semiconductor - Sanyo)

	Chip application deadline	Design deadline	Chip delivery
2017 #1	2017/ 7/10	2017/10/ 2	2018/ 1/ 4
2017 #2	2018/ 1/15	2018/ 3/26	2018/ 6/25

○ 0.18 mm CMOS (Rohm)

	Chip application deadline	Design deadline	Chip delivery
2017 #1	2017/ 5/21	2017/ 6/26	2017/ 9/21
2017 #4	2017/ 9/ 7	2017/ 9/19	2017/12/19
2017 #2	2017/ 8/ 7	2017/10/30	2018/ 1/31
2017 #3	2017/11/27	2018/ 2/19	2018/ 5/28

○ SOTB 65 nm CMOS

	Chip application deadline	Design deadline	Chip delivery
2017 #1	2017/ 6/19	2017/ 7/18	2017/12/14
2017 #2	2017/12/18	2018/ 2/23	2017/ 8M

1.3.3 Libraries and design flows

VDEC have been working to prepare design libraries and design flows for digital design and PDKs for analog design. Table 1.3.2 lists libraries available now.

Table 1.3.2 Libraries available for VDEC chip fabrication

Technology	Name	Author	Contents
0.18 mm CMOS (Rohm)	Rohm library	Rohm Library Std. Cells, IO cells, RAM (Distributed with CDROM)	Synthesis(Synopsys)
			Simulation(VerilogXL)
			P&R(LEF/DEF)
	Kyodai Library	Onodera Lab., Kyoto University	Synthesis(Synopsys)
			Simulation(VerilogXL)
			P&R(Astro)
	Todai Library	VDEC Design flow based on library prepared by Onodera Lab., Kyoto University	Synthesis(RTL Compiler)
			Simulation(VerilogXL)
			P&R(Encounter)
	PDK	VDEC	PDK(IC6.1)

1.4 Seminar

Seminar is indispensable for the improvement of LSI design technology. Some seminar and forums, such as technical seminar for CAD use, refreshing seminar for working people, designer's forums for young professors and students were held in 2016.

【Technological seminar for CAD use】

In a technological seminar for CAD use, VDEC invites lecturer from each tool vender, such as Cadence, Synopsys and Agilent, to hold the CAD operation course. Moreover, the course concerning the design flow in the VDEC environment was held by the VDEC staff. A technological seminar for CAD use for the beginner was held in The University of Tokyo VDEC in August and September at the year 2017. This seminar took 5 days for 2 kinds of Cadence tools, 3 days for 2 kinds of Synopsys tools, 1 days for 1 kind of Keysight tool. In addition, VDEC teachers gave lecturers on transistor level circuit design course, and digital circuit design course under the VDEC EDA environment. Teachers and students up to 40 people attended a lecture in each course, and master the use of each tool for VLSI design flow that uses the VDEC library. Moreover, another technical seminar for CAD use for matured teachers and students was held in March by Cadence 2 kind and 4 days, Synopsys 2 kinds and 2 days (Table 1.4.1). The demand for these CAD technological seminars is very large, and VDEC has maintained the mechanism of a large-scale CAD technological seminar holding corresponding to this situation. So far, the seminar was held at the University of Tokyo OR other VDEC branch, however, we started to distribute the lecture using Web streaming, so that students around VDEC branch can take the seminar at the branch school.

Table 1.4.1 CAD technological seminar in summer of the year 2016

2017/08/17-18	Synopsys DesignCompiler+PowerCompiler Seminar	Univ. of Tokyo	13
2017/08/17-18	Synopsys DesignCompiler+PowerCompiler Seminar	Kyoto Univ.	1
2017/08/17-18	Synopsys DesignCompiler+PowerCompiler Seminar	Osaka Univ.	6
2017/08/17-18	Synopsys DesignCompiler+PowerCompiler Seminar	Hiroshima Univ.	2
2017/08/22-23	Cadence Virtuoso ADE Seminar	Univ. of Tokyo	11
2017/08/22-23	Cadence Virtuoso ADE Seminar	Tohoku Univ.	3
2017/08/22-23	Cadence Virtuoso ADE Seminar	Kyoto Univ.	1
2017/08/22-23	Cadence Virtuoso ADE Seminar	Hiroshima Univ.	1
2017/08/22-23	Cadence Virtuoso ADE Seminar	Akita Pref. Univ.	2
2017/09/6-8	Cadencee Virtuoso Layout Seminar	Univ. of Tokyo	15
2017/09/6-8	Cadencee Virtuoso Layout Seminar	Kyoto Univ.	2
2017/09/6-8	Cadencee Virtuoso Layout Seminar	Osaka Univ.	5
2017/09/6-8	Cadencee Virtuoso Layout Seminar	Hiroshima Univ.	1
2017/09/6-8	Cadencee Virtuoso Layout Seminar	Akita Pref. Univ.	5
2017/09/13	Synopsys HSPICE Seminar	Univ. of Tokyo	8
2017/09/13	Synopsys HSPICE Seminar	Tohoku Univ.	2
2017/09/13	Synopsys HSPICE Seminar	Osaka Univ.	4
2017/09/13	Synopsys HSPICE Seminar	Hiroshima Univ.	1
2017/09/13	Synopsys HSPICE Seminar	Akita Pref. Univ.	5
2017/09/13	Synopsys HSPICE Seminar	Ariake Tech. Col.	9
2017/09/14	Keysight Golden Gate Seminar	Univ. of Tokyo	9

2017/09/14	Keysight Golden Gate Seminar	Osaka Univ.	1
2017/09/14	Keysight Golden Gate Seminar	Hiroshima Univ.	1
2017/09/14	Keysight Golden Gate Seminar	Akita Pref. Univ.	5

2018/03/08-09	Cadence Innovus Seminar	Univ. of Tokyo	16
2018/03/08-09	Cadence Innovus Seminar	Osaka Univ.	3
2018/03/08-09	Cadence Innovus Seminar	Hiroshima Univ.	3
2017/03/13	Synopsys XA-VCS CoSim Seminar	Univ. of Tokyo	13
2017/03/13	Synopsys XA-VCS CoSim Seminar	Hiroshima Univ.	2
2017/03/13	Synopsys XA-VCS CoSim Seminar	Miyazaki Univ.	1
2017/03/14	Synopsys IC Symplify Seminar	Univ. of Tokyo	19
2017/03/14	Synopsys IC Symplify Seminar	Hiroshima Univ.	2
2017/03/19-20	Cadence Allegro PCB + Sigrity Seminar	Univ. of Tokyo	13
2017/03/19-20	Cadence Allegro PCB + Sigrity Seminar	Hokkaido Univ.	2
2017/03/19-20	Cadence Allegro PCB + Sigrity Seminar	Hiroshima Univ.	2

【Refresh Seminar for Working People】

Teachers of universities and designers in the first line of the enterprise were invited to the lecturer at "VLSI design refresh seminar" was held aiming at the latest, advanced knowledge and technical learning concerning VLSI design as a refreshing education for working people involved in the integrated circuit industry (Table 1.4.2). Though this seminar started chiefly in year 1998 under the support of Ministry of Education Technical Education Division to give practicing education of the latest VLSI design technology, it continues under many supports from many societies.

Course A: analog integrated circuit design (7/10 -12), Course M1: MEMS design (6/12-13), Course M2:MEMS fabrication (7/18-20), and Course R: RF circuit design (7/13-14). Teachers from industry and universities involved in the integrated circuit research and the education were invited as the lecturer, and they introduced a state-of-the-art VLSI design technology including the practice using a lecture concerning VLSI design and the latest CAD tool. The participants for the course A, M1, M2, R were 19, 14, 12, 3, respectively.

Fig. 1.4.2 Refresh Seminar at VDEC seminar room at the University of Tokyo, VDEC.

Table 1.4.2 Refresh Seminar

Course A: Analog Circuit Design (3 days)
Analog Circuit Design and simulation Integrated Circuits Verification (LVS, DRC)
Masahiro Sugimoto (Chuo Univ.), Hidetoshi Onodera (Kyoto Univ.), Koji Kotani (Tohoku Univ.)

Course M1: MEMS Design (2 days)
MEMS Basic 1: Fabrication Process MEMS Basic 2: Operation Principle Structual Design Layout Design
Yoshio Mita (Univ. of Tokyo)

Course M2: MEMS Fabrication (3 days)
CAD Design and Analysis Lithography, Etching, Release Vibration measurement and analysis
Yoshio Mita (Univ. of Tokyo)

Course R: CMOS-RF Circuit Design (3days)
Modulation/Demodulation, Cascaded connection Basic Performace, Tranceiver Architecture Circuit Element, Design Flow
Hiroyuki Ito (Tokyo Institute of Technology)

【Designer's forum for young teachers and students】

VDEC LSI designer forum intended for students and young teachers has been held. The VDEC LSI designer forum has aimed to sharing information that cannot be obtained at a society and an academic society, for example, the failure case and the solution in which LSI designer has a hard time, the inside story of CAD industry, the construction method in the design milieu in the laboratory, and so on. This year, we had the meeting in Futsukaichi Hot Spring, in September. No less than 35 participants were flourishing at the gathering.

Table 1.4.3 Program of Designers Forum in 2017

9/4 (Mon)

Time	
12:00-12:30	Reception
12:40-14:20	VDEC Design Award Presentation I
14:30-16:10	VDEC Design Award Presentation II
16:20-17:40	VDEC Design Award Presentation III
19:00-	VDEC Design Award Ceremony

9/5 (Tue)

Time	
9:00-10:00	Idea Contest Presentaion
10:00-12:00	Ph.D Session
12:00-13:00	Plenary Talk
13:00-13:10	Closing

1.5 Facilities

The VDEC has provided the big facilities for universities in Japan from its establishment (1996). Big facilities refer to those which are impossible to acquire and or maintain by an individual research unit. Table 1.5.1 shows the available facilities of VLSI testers and some process machines, which are placed at the tester room and the super clean room of the Takeda building. In 2004, the VLSI tester (T2000) and the EB lithography machine (F5112+VD01) were donated to the VDEC by the ADVANTEST. In the year 2012, VDEC joined MEXT (Ministry of Education)'s Nanotechnology platform to enforce its multi-use capability. (For Nanotechnology Platform refer section 1.8).

In 2017, VDEC has launched a cooperative project with LPKF Laser & Electronics Corporation Japan. LPKF's UV laser printed circuit machine (ProtoLaser U3) is installed in Takeda Building room 204 (called as VDEC backend room). The machine is capable of engraving up to 35 μm-thick copper wirings and othermaterials.

The facilities can be used by user himself, after a couple of times'training by attendance of licensed users; also, by presence of licensed persons, a new user can readily use the machine.

Table1.5.1 Available facility list

Facility	Equipment name	Description	Status	Contact
Logic LSI test System	EB tester: IDS10000	The chip surface voltage during operation can be measured with the LST tester. The digital circuit with 384 pins, 1 GHz can be tested.	Available	nanotech@sogo.t.u-tokyo.ac.jp
	LSI tester: ADVANTEST T2000	The digital circuit with 256 pins, 512 MHz can be tested. Analog test is optional.	Available	nanotech@sogo.t.u-tokyo.ac.jp
	Auto prober: PM-90-A	Automated prober for testing LSI wafers, which can be used with the LSI testers. The probe card for LSIs with the VDEC standard pin connections is available.	Available	nanotech@sogo.t.u-tokyo.ac.jp
Analog/RF measurement system	Analog/RF measurement system: B1500A, 4156B, HP4284, etc	DC parameter measurement, Capacitance measurement, Network analyzer, Spectrum analyzer, etc.	Available	nanotech@sogo.t.u-tokyo.ac.jp
	Low-noize manual prober: Cascade Microtec	6 inch wafer can be measured with six DC probles and two RF probes upto 50 GHz.		
	Low-noize, temperature controlled semi-auto prober: Süss Microtec	8inch wafer can be measured. The chip temperature range is -50 to 200°C.		
Nanotechnology Platform Apparatuses	Mask lithography, Direct lithography: F5112+VD01	Minimum linewidth: 50 nm. Lithography for 5 inch photomask (thickness: 2.3 mm), 2-8 inch wafers, and chips is possible.	Available	nanotech@sogo.t.u-tokyo.ac.jp
	Rapid Mask and Direct lithography: F7000S-VD02	Minimum linewidth: 1xnm. Lithography for 5 inch photomask (thickness: 2.3 mm), 2-8 inch wafers, and chips is possible. Stencil character projection of non-square shapes such as circle, triangle is possible.	Available	
	Chlorine ICP plasma etcher CE-S	High density plasma etching with Cl_2 and BCl_3 is possible.	Available	
	Silicon DRIE MUC-21 ASE-Pegasus	High speed, high aspect ratio etching of silicon is possible	Available	

	UV Laser Printed Circuit Board Engraver LPKF ProtoLaser U3	Using UV laser, copper material up to 35μm and other materials such as flexible material can be engraved.	Available at VDEC 204
FIB system	FIB: SII XVision200TB	Repair of photomask, sample etching, etc. (Through Nanotech. Platform and LCNet)	Available
LSI FIB system	FIB: FEI V400ACE	Repair of VLSI from both frontside and backside, with CAD navigation and / or IR camera is possible. W/SiO_2 deposition is possible.	Available
Chip Bonding System	Wedge Bonder: Westbond 7476D	25 μm ϕ Al or Au wire wedge bonding machine.	Available
	Epoxy Die Bonder Westbond7200C	Precision Manupilator system. Epoxy and or Ag paste chip bonding and or glued wiring.	
	Semi-Auto Bonder Westbond4700E	18 ～ 25 μm ϕ Au Ball bonding or bump creation.	
	Precision Manual Flip-Chip Bonder Finetech Fineplacer Lambda	Face-to-face bonding up to 15 mm square chips. Alignment is through video camera. Bonding is by heating chips with TV camera. (Ultrasonic Unit can additionally be purchased.) XY ± 0.5 μm, and θ =1mrad precision.	

1.6 Activity plan for 2018

VDEC will continue activities on chip fabrication services, CAD tool support, dispatching design related information and donated division "D2T", as has been previous years.

【Design related information dispatching/Seminar】

We will continue holding the following seminars: (1) CAD tools seminars which have been continued since 1997, (2) "Refresh seminar" since 1998, (3) "Designer'Forum" since 1997. We will also continue seminars for LSI tester usage at VDEC and sub-centers, workshops on LSI testing technologies initiated by D2T.

【CAD tool support】

We will continue Cadence tools, Synopsys tools and Mentor tools as the main stream design tools. We will continue analog RF design environment, GoldenGate and ADS by Agilent, C-based design environment, BachC by Sharp. In addition, we continue trial of several CAD tools, such as layout platform, Lavis by TOOL. Design debugging platform from SpringSoft has merged into Cadence tools and will be continued. SmartSpice by Silvaco, will be also continued.

【Chip fabrication services】

We will continue chip fabrication services for SOTB 65 nm CMOS by Renesas Electronics, 0.18 mm CMOS by Rohm, FD-SOI 28 nm CMOS by ST Microelectronics through CMP and 0.8 mm CMOS by On-semiconductor-Sanyo as the regular services.

Table 1.7.1 Chip fabrication schedule

【CMOS 1.2μm2P2M】 On-Semiconductor(Former Motorola Japan)

	Chip application deadline	Design deadline	Chip delivery
2018 #1	2017/ 7/10	2017/10/ 2	2017/12/25
2018 #2	2018/ 1/15	2018/ 3/26	2018/ 6/25

【CMOS 0.18μm1P5M(+MiM)】 Rohm

	Chip application deadline	Design deadline	Chip delivery
2018 #1	2018/ 4/ 2	2018/ 6/25	2018/10/12
2018 #2	2018/ 6/18	2018/ 9/10	2018/12/28
2018 #3	2018/ 8/13	2018/11/ 5	2019/ 2/22
2018 #4	2018/12/ 3	2019/ 2/25	2019/ 6/14

【FD-SOI CMOS 28 nm1P10M】 ST Microelectronics

Based on the chip fabrication schedule through CMP.

【SOTB CMOS 65 nm】 Renesas Electronics

	Chip application deadline	Design deadline	Chip delivery
2018 #1	2018/ 6/18	2018/ 7/30	2019/ 2/ 2
2018 #2	2018/12/17	2019/ 1/28	2019/ 7/27

1.7 Venture companies related to VDEC

Some professors related to VDEC started venture companies. The following is a list of the venture companies related to VDEC.

[1] AIL Co., Ltd. (http://www.ailabo.co.jp/)

Related professor : Professor Kazuo Taki, Kobe Univ. (President-Director)

[2] Synthesis Corporation (http://www.synthesis.co.jp/)

Related professor : Professor Emeritus Isao Shirakawa, Osaka Univ. (Director)

Description of business : (1) Hardware/software co-design
(2) System LSI design, design services
(3) Development and sales of IPs
(4) Development of EDA tools

[3] Nanodesign Corporation (http://www.nanodesign.co.jp/)

Related professor : Professor Kazuyuki Nakamura, Kyushu Institute of Technology. (Representative Director)

[4] A-R-Tec Corp. (http://www.a-r-tec.jp/)

Related professor : Professor Emeritus Atsushi Iwata, Hiroshima Univ. (Representative Director)

Description of business : (1) Measurement and analysis of LSI substrate noise
(2) Design of analog-RF mixed signal LSIs
(3) Training of analog design on the JOB method

[5] Ishijima Electronics (http://ishi.main.jp/)

Description of business : (1) Electronic circuit development
(2) Software development
(3) Consulting

1.8 “Nanotechnology Platform”: Ultra Small Lithography and Nanometric Observation Site

VDEC is operating an open-use nanotechnology platform “Ultra Small Lithography and Nanometric Observation Site” together with the Institute of Engineering Innovation of Graduate School of Engineering. The site is supported by Japanese Ministry of Education (MEXT)’s Nanotechnology Platform grant. Any researchers in Japanese Universities, Laboratories, and Companies can take full advantage of The University of Tokyo’s cutting-edge nanotechnology apparatuses and know-hows. The accessible technology includes Lithography and Etching environment, Ultra High-Voltage Acceleration (1MV) transmission electron microscope (TEM) that is capable of visualizing upto light materials such as Nitrogen. VDEC takes part in the lithography at Takeda Sentanchi Super Cleanroom. Through VDEC’s key apparatus F5112+VD01 donated from Advantest Corporation as well as F7000S-VD02 purchased by national budget, VDEC is supporting post-VLSI activities such as MEMS. The machine is capable of rapidly writing patterns on arbitrary-shaped targets sizing from 1cm-sqare chip to 8-inch round wafers. The performance is measured by the number of research reports and machine use. The University of Tokyo site has received 168 research reports, composed of 29 from big companies, 4 from Small and Medium-size Enterprises (SMEs), 35 from other universities, 91 from UTokyo researchers (including external collaboration but excluding VDEC), and 10 from public research institutes. The exposure count was 2434 for 12 months (202.8 / month), which is the first time that use per month exceeded 200. As shown in the Fig. 1, usage is monotonously increasing. “Open ratio”, which is the number of days in which users outside the University of Tokyo came, divided by machine open days, was 99%. Due to the strong support of nanotech. Platform, even a novice user can obtain fine lithography result by using the apparatuses with the Platform engineering staffs of VDEC. Consequently, free machine time is decreasing so the team is trying to acquire financial support to increase the number of machines. Also in FY2017, the French Nanotechnology Network project CNRS-RENATECH asked to the UTokyo VDEC to launch an engineer-class international exchange program. The program is financially fully supported by VDEC’s project and one Ph.D-holding research engineer from France (FEMTO-ST, Besançon) is with VDEC Mita Lab for one year.

URL:http://nanotechnet.t.u-tokyo.ac.jp/

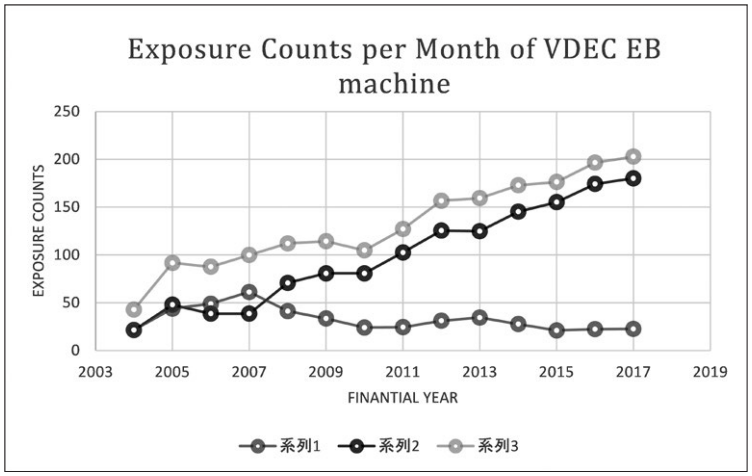


Fig. 1 Monthly Average Exposure Count of EB Machine (s).

2. Activity Report of ADVANTEST D2T Research Division

2.1 Introduction of ADVANTEST D2T Research Division

2.1.1 Aim of the establishment of ADVANTEST D2T Research Division

The ADVANTEST D2T research division was established in VDEC in October 2007. As the name suggests, it is financially supported by ADVANTEST Corporation.

The aim of establishment of the ADVANTEST D2T research division is to promote the research and education environment of VLSI testing in all universities and colleges in Japan. "D2T" means that we consider not only design but also testing. Through our activities, we hope to provide expertise in design and testing for the industry. In addition, we are exchanging researchers with other universities and research institutes in both Japan and overseas. Moreover, the D2T research division is suitable for collaborations with the industry because the testing of VLSI is one of the most practical research topics in the industry. Based on these activities, our final goal is to become a center of excellence of VLSI testing in Japan.

The D2T research division has spent 10 years in total for the 1st (Oct. 2007–Sep. 2010), 2nd (Oct. 2010–Sep. 2013), and 3rd (Oct. 2013–Sep. 2016) project phases, and now we are in the 4th phase of the D2T project courtesy of ADVANTEST Corporation.

In this financial year, we invited Professor Adit Singh from Auburn University (2018/1–) for research and educational collaboration with VDEC.

The details of our group's activities are presented in the following sections.

2.1.2 Members of ADVANTEST D2T Research Division

Project Professor	Masahiro Fujita
Project Professor	Adit Singh (2018/1～)
Project Lecturer	Akio Higo (2017/10～)
Project Lecturer	Rimon Ikeno (～2017/9)
Project Researcher	Parit Kanjanavirojkul (2017/4～2018/3)
Researcher	Takahiro Yamaguchi (ADVANTEST Laboratories Ltd.) (～2017/12)
Researcher	Masahiro Ishida (ADVANTEST Corporation) (～2017/9)
Researcher	Koji Asami (ADVANTEST Corporation) (2017/10～)
Assistant Clerk	Makiko Okazaki

2.2 Report of 12th D2T Symposium

The 12th D2T Symposium was held on September 28th, 2017 at Takeda Hall.

This year, we invited four lecturers from overseas for their work on research topics related to IoT and data analytics: Prof. Kwang-Ting (Tim) Cheng from Hong Kong University of Science and Technology, Prof. Shawn Blanton from Carnegie Mellon University, and Prof. Wolfgang Kunz and Prof. Dominik Stoffel from Technische Universität Kaiserslautern. The symposium also featured special lectures by Prof. Shinichi Takagi and Prof. Hiroyuki Morikawa from the University of Tokyo.

We sincerely appreciate every participant for their contribution at the symposium. We look forward to seeing many participants again at the next symposium.

12th D2T Symposium program

10:00	**Opening Remarks** Kunihiro Asada (Director, VDEC, The University of Tokyo) Koichi Tsukui (Managing Executive Officer Executive Vice President, Corporate Relations Group, ADVANTEST Corporation)
10:30	**Session 1** (Chairman: Makoto Ikeda, The University of Tokyo) *"Advanced MOS device technology for ultra-low-power IoT applications"* Shinichi Takagi (The University of Tokyo) *"Going Digital: Transformation of Society, Industry, and Life"* Hiroyuki Morikawa (The University of Tokyo)
12:00	**Lunch**
13:15	**Session 2** (Chairman: Tetsuya Iizuka, The University of Tokyo) *"Power Supply Impedance Emulation to Eliminate Overkills and Underkills due to the Impedance Difference between ATE and Customer Board"* Toru Nakura (The University of Tokyo) *"Common Pitfalls in Application of a Threshold Detection Comparator to a Continuous-Time Level-Crossing Quantization"* Takahiro J. Yamaguchi (Advantest Laboratories Ltd., The University of Tokyo)
14:05	**Break**
14:15	**Session 3** (Chairman: Yoshio Mita, The University of Tokyo) *"Variation and Failure Characterization Through Test Data Analytics"* Kwang Ting Cheng (Hong Kong University of Science and Technology) *"Test-Chip Design for Yield Learning at the 7-nm Technology Node"* Shawn Blanton (Carnegie Mellon University)
15:45	**Coffee Break**
16:15	**Session 4** (Chairman: Masahiro Fujita, The University of Tokyo) *Rethinking Design in the IoT Era - How Formal Methods Help to Meet the Challenges"* Wolfgang Kunz (Technische Universität Kaiserslautern) *"Software in a Hardware View: New Models for Firmware Development and Safety Analysis in IoT Systems"* Dominik Stoffel (Technische Universität Kaiserslautern)
17:45	**Closing**
18:00	**Reception**

2.3 Research Activity Reports of ADVANTEST D2T Research Division

High-Resolution Analog-to-Digital Converter Based on Stochastic Comparators

Takahiro J. Yamaguchi, Parit Kanjanavirojkul,
Nguyen Ngoc Mai-Khanh, Rimon Ikeno,
Tetsuya Iizuka, Kunihiro Asada

This project aimed to implement a high-resolution sub-ranging analog-to-digital converter (ADC) circuit based on stochastic comparators.

Process variations, together with many factors such as variations in voltage or temperature, lead to mismatched design parameters that produce input-referred offsets and hence cause non-linearity and missing output codes in an ADC. Instead of attempting to suppress such process variations as in conventional ADC, the stochastic ADC approach exploits process variations based on the assumption of a Gaussian distribution of comparator offset voltage. We identified the root cause of a voltage bounce of the source nodes of the comparator input PMOSFETs, which introduces a conversion error of the flash ADC circuit at the first stage in our sub-ranging ADC system, as quick signal transition. We improved the performance of the ADC by refining operational conditions, such as input signal frequency, slope, and voltage range, as well as by adding a delay in starting the differential current integration so as to discard the unstable current during the bouncing period.

Power Integrity Evaluation Method

Masahiro Ishida, Naoki Terao, Rimon Ikeno,
Toru Nakura, Tetsuya Iizuka, Kunihiro Asada

While the required power-supply voltage has decreased owing to the advanced miniaturization of the semiconductor process, the power-supply current consumed by a semiconductor device has increased because of the huge number of transistors integrated on a single chip. This may increase the power-supply noise and cause power integrity issues of the device under test in both an ATE and practical operating environments. The purposes of this research project are to develop a power delivery network modeling method for evaluating power integrity at on-chip power-supply nodes in semiconductor devices and a new power integrity control method based on the feedback operation.

We proposed a new modeling method of series impedance connection using the nested-feedback configuration in the digital filter composition for the previously proposed feedback-based power supply impedance emulation, and we demonstrated its feasibility through computer simulation and experiments. We also extended the impedance modeling method to cases with multiple power-supply pins and carried out simulation-based studies to verify the assumed modeling methods. Furthermore, we demonstrated that the proposed method can eliminate the discrepancy of test results between two power-supply environments through an experiment with FPGA devices.

High-Performance Analog-to-Digital Conversion Using the Wideband Spread Spectrum and Its Application

Koji Asami, Byambadorj Zolboo, Akio Higo,
Tetsuya Iizuka, Kunihiro Asada,

To measure low-cost RF devices for IoT and other applications, analog-to-digital conversion techniques with a low cost and high efficiency are required. To acquire narrow-band modulation signals scattered in a wide frequency range, a compression sampling method is studied.

In this financial year, a modulated wideband converter was investigated as a compression sampling method. After a recovery error using an arbitrary waveform was estimated, we determined that the recovery of a side lobe, as well as the main lobe, is required in a modulated waveform. Therefore, the relationship among recovery error, ADC performance (resolution and sampling rate), and the number of channels is needed to establish the cost of ADC. We study the cost of ADC, spread code, recovery algorithm, and mismatch correction between analog-to-digital channels.

High-Throughput and High-Accuracy Electron-Beam Direct Writing (EBDW) Strategy for Wide Range of EBDW Applications

Rimon Ikeno, Akio Higo, Yoshio Mita, Kunihiro Asada

Maskless lithography by electron-beam direct writing (EBDW) is expected to be a low-cost lithography technology with a short turn-around time (TAT), but it has some drawbacks such as a low process throughput and low accuracy against the intended layout shapes. We are pursuing a high-speed and high-accuracy EBDW strategy utilizing the character projection (CP) method to overcome these concerns and to boost EBDW use in fields such as MEMS and photonics.

We investigated the resist and development process conditions for the high-resolution observation of lithographic results by our high-throughput and high-accuracy EB exposure strategy that combines the CP and variable-shaped beam (VSB) methods. A new CP mask for the F7000S EB writing system in the VDEC Takeda Clean Room was designed for further performance improvement. We also conducted a numerical analysis of chip temperature during the EB exposure process as well as the propagation loss of light waveguides dependent on the line-edge (wall) condition.

2.4 Publications

International Conferences, Symposiums, Workshops

[1] Naoki Terao, Toru Nakura, Masahiro Ishida, Rimon Ikeno, Takashi Kusaka, Tetsuya Iizuka, and Kunihiro Asada, "Extension of Power Supply Impedance Emulation Method on ATE for Multiple Power Domain," 22nd IEEE European Test Symposium (ETS 2017), May 2017.

Domestic Conferences, Workshops, etc.

T. Sugiyama, T. Iizuka, T. Yamaguchi, T. Nakura, K. Asada "Performance Analysis of Level-Cross Detection Method Based on Stochastic Comparator," IEICE-CAS2017-66, IEICE-ICD2017-54, IEICE-CPSY2017-63, 12/14/2017.

Chapter 3 Research in VDEC

Asada, Nakura and Iizuka Laboratory

(http://www.mos.t.u-tokyo.ac.jp)

LSI Test and Improved Reliability in Ultra-Fine Process Technologies

Kunihiro Asada, Toru Nakura, Tetsuya Iizuka, Naoki Terao

In LSI test, mismatch of power supply impedance between an automatic test equipment (ATE) and a customer board can cause overkills and underkills. We propose power supply impedance control method on the ATE for emulating arbitrary power supply impedance using compensation current injection. Experimental measurement results by a prototype system shows that the voltage fluctuation waveform of the ATE is adjusted to that of the customer board, meaning that the impedance on the customer board is successfully emulated by the ATE.

Our digital filter implementation method using feedback can be applied to arbitrary impedance network, not only for the power supply with single supply pin but also for the power supply with multiple power domains.

To confirm the effect of the proposed method on real LSI test, we developed a virtual ATE for demonstration. Test result of 50 real devices shows significant reduction of overkills and underkills under the power supply condition with impedance emulation.

PLL and LDO circuits with Time-Domain control

Kunihiro Asada, Toru Nakura, Tetsuya Iizuka, Keigo Tu, Jing Wang, Naoki Ojima, Hidemasa Yoshimura

In this research, we have applied time-domain control methods to PLL circuit and its measurement. A Pulse-Width Controlled PLL (PWPLL) is a new type of PLL whose oscillator is controlled by a pulse width. The PWPLL is implementable in a very small area, on the one hand, its operating conditions are sensitive to the several variations. For example, a lock range of the PWPLL tends to be narrower than that of other PLLs.

We demonstrated a PWPLL compiler which generates GDS data and summarizes synthesized and simulation results of area, power and jitter of PWPLL with different gate length cells and choose an appropriate PWPLL design from performance specification. The inputs of the compiler are standard cell libraries, several manual cells, SPICE parameters and the target specification input-output frequency, the division ratio and the Process, Voltage, and Temperature (PVT) corner conditions. The PLL compiler calculates rough values of the design parameters, runs SPICE simulations, analyze the waveform files to adjust the design parameters, considering the variation of the PLL characteristics with the given PVT variation. When the waveform satisfies the specification, the compiler generates a verilog netlist and a GDS is designed from the netlist.

Besides, since skilled circuit designers need to spend a lot of time to make PLL(Phase Locked Loop) circuits, so a method by which everyone can create a PLL circuits in a short time is required. In this research, automatic design was made possible by creating a DCO (Digital Controlled Oscillator) in the digital PLL circuit using an inverter, NAND gate and 4-input multiplexer. We automatically simulated the DCO performance by SPICE, automatically found the appropriate parameters of the DCO circuit from the input performance of DCO and automatically created the layout of DCO using a C program.

We also do a research on LDO. Designing LDO regulators nowadays almost largely demands analog circuit design flows. Because Analog flows take time and effort, they become a bottleneck in designing LDOs. In this research, to remove the loads of analog flows, we applied a method of making LDOs with a P&R tool which is usually used in digital circuit design flows. In conventional LDOs, the parts which makes comparison between the reference and the output, such as error amplifiers or comparators, often require analog flows. The proposed circuit in the research contains two inverter chains and a phase detector. The phase detector recognizes the voltage difference between reference and output as the delay difference between two inverter chains. This comparison part is all synthesizable from standard cells, so all the circuit can be made by a P&R tool. We designed and made the proposed circuit, and confirmed trackability when the reference or the load current are changed.

Time Domain CDR and TDC Designs

Kunihiro Asada, Toru Nakura, Tetsuya Iizuka,
Meikan Chin, Ryuichi Enomoto

While digital circuits directly benefit from advanced process technologies, analog circuits suffer from negative effects such as small voltage headroom. Time-domain circuits, where analog signals are represented by digital signal edge transitions, could be a solution to the problem of analog circuits in a nanometer process.

Time-to-Digital Converter (TDC) is a representative example of time-domain circuits. TDC basically converts a time interval between two rising edges into a digital code by using delay elements. In our research, we focus on a pulse-shrinking TDC, which is one kind of the sub-gate-delay resolution TDCs. In general, TDC has a trade-off between the time resolution and dynamic range, and the trade-off is particularly remarkable in the pulse-shrinking TDC. Last year we designed and measured a TDC that improves the dynamic range while keeping the high resolution by using a hierarchical approach. We found that the TDC has a serious nonlinearity caused by process variation. So, we analyzed the impact of it by Monte Carlo simulation and designed a new TDC resistant to process variation.

TDC can be applied for various applications and Clock and Data Recovery (CDR) based on Cycle Lock Gated Oscillator (CLGO) is one example. Since the CDR consumes no dynamic power in its standby state and resumes from the standby state just after a 4-bit preamble, it can improve the total power efficiency of serial communication systems that work intermittently such as mobile and IoT sensor node applications which require not only low power consumption in operation but also in standby state and quick startup form the standby state. We proposed CDR using Delay Tunable Buffer (DTB) and Vernier TDC for tracking frequency range extension and low power consumption, designed and measured. While DTB and digital control work as designed, we found the deviation of timing in Vernier TDC. So we proposed new Vernier TDC whose reference level is tunable.

Radiation Detector Utilizing Semiconductor Photodiode

Kunihiro Asada, Toru Nakura, Tetsuya Iizuka,
Yang Xiao

Scintillation detectors and semiconductor detectors have received wide spread attention since they can specify the nuclide of radiation and estimate the arrival angle. Former research proposed a detector using the cube scintillator, SPAD (Single Photon Avalanche Diode) array image sensors, multi-coated materials, and pinholes and verified the method to detect the position of point light source inside the scintillator. We proposed a new method which calculated the track of photons to precisely estimate the position of light source. This method can cost less time to detect the light source position compared to the former research. The result of the simulation verified that by using this method the position of the light source inside the 1 mm-size scintillator could be detected with a spatial resolution of 10 um-20 um in less than 0.3s.

About the SPAD imager, we have designed several SPADs with different structures in standard CMOS process, and found a suitable structure. Then, a 31 x 31 SPAD imager with event discriminator based on the proposed breakdown pixel extraction architecture has been fabricated, and its functionality of short weak light detection has been demonstrated.

High-Frequency Circuit Design for Communication through Dielectric Waveguide

Kunihiro Asada, Toru Nakura, Tetsuya Iizuka, Nguyen Ngoc Mai-Khanh, Yoshitaka Otsuki, Daisuke Yamazaki

High-speed communication with the millimeter-wave band has been actively researched. Wireline communication with a dielectric waveguide such as polymer has been proposed and expanded research. Because it is possible to increase the communication distance at low cost while maintaining the communication speed.

The signal leaks to the outside at the bent portion of the waveguide when the frequency is low in the dielectric waveguide communication. Therefore, a high-frequency oscillator is required. In this research, we studied oscillators that oscillate at 140 GHz and have low phase noise, and also designed transmission lines and pads for measurement.

The dielectric waveguide is superior to the metal waveguide in terms of weight and price, the loss is large, so that a low loss on-chip coupler is required.

In this research, we designed a low loss on-chip coupler for use in dielectric waveguides.

One of the main causes of the electric-electromagnetic wave conversion loss in the on-chip coupler is that part of the electric power is converted into heat due to

the eddy current generated in the substrate. For this reason, we propose a method to suppress the eddy current by removing the Si substrate of the chip and reduce the loss during conversion. We verified this low loss implementation method and designed a chip for verification.

Design and Analysis Method for High-Reliability LSIs

Kunihiro Asada, Toru Nakura, Tetsuya Iizuka, Nguyen Ngoc Mai-Khanh, Norihiko Nakasato, Daigo Takahashi, Tamaki Fukudome

The modern VLSI systems that demand high reliability require carefully-designed power/ground network to provide stable power supply. Using the measurement results of magnetic field emission from LSI, the proposed method estimates the actual current flow from the magnetic field measurement results and enables us to find defects or design faults such as VIA/wire disconnections and/or current concentration with low cost. To verify the feasibility of the proposed method with actual measurement results, the test structure is designed and fabricated in 0.18 um 1P5M CMOS process. Current flow of power network in the chip was successfully estimated by actual measurement data.

Information security is very important in the modern society in which the Internet has penetrated. In this research, we propose a method to enhance the reliability of PUF (Physical Unclonable Function) and TRNG (True Random Number Generator) by employing aging phenomenon of scaled MOSFET to control the threshold voltage. Reliability enhancement of both circuits will lead to miniaturization and low-power consumption of security hardware. Currently, we confirmed by measurement that it is possible to improve the reliability of both circuits by inducing proper degradation in the SRAM.

With the improvement of the circuit performance due to the miniaturization of the semiconductor process, the speed of transmission has been improving. The data rate necessary for applications also has been improving because UHD TVs and automobiles with a lot of electrical equipment was developed. It is necessary to speed up transmission from both aspects of technology and demand, crosstalk is one of the factors hindering this. As measures for crosstalk, a circuit for reducing crosstalk at the receiving end was proposed in the previous research. In this research, we proposed a circuit with PD control circuit and time delay element based on the circuit in the previous research. Using simulation, we showed that the circuit can reduce crosstalk more effectively.

High-Precision A-D Converters

Kunihiro Asada, Toru Nakura, Tetsuya Iizuka, Takaaki Ito, Taiki Sugiyama

Analog-to-Digital Converters (ADC) are widely used as circuits which convert analog signal to digital signal. Low-power and high-precision ADCs are needed for applications such as biomedical sensing and wireless sensor network. In this study, successive approximation register (SAR) ADC which have several advantages for better power efficiency is designed in order to achieve high-precision and low-power ADCs. Though there is a tradeoff between conversion accuracy and power consumption, we optimized power consumption by combining noise tunability implemented to comparator and redundant bit technique. Recently, we designed prototype ADC and evaluated its performance.

ADC based on level-cross detection quantizes time rather than voltage. When the clock frequency is doubled, SNR of ADC improves 3 dB whereas that of level-crossing ADC improves 6 dB. Therefore, level-crossing ADC benefits more from fine time resolution in scaled technologies. A stochastic comparator that drives multiple comparators in parallel is proposed to improve both voltage and time resolutions by utilizing stochastic nature of offset and noise whose impact is increasing through process miniaturization. A stochastic comparator is familiar with the digital design because of the concept based on process variation and it will improve the performance by process miniaturization. We analyze the precision of level-cross-timing estimation method based on a stochastic comparator. We show that the level-cross-timing estimation method exhibits finer resolution compared to that uses the single comparator with the same total area of comparators. We also verify the theory by measurement. Another design approach is stochastic approach in which many comparators are driven in parallel. This emerging approach can be applied to level-crossing ADC and it is called level-crossing stochastic ADC. We analyze input slope dependency of level-crossing stochastic ADC by circuit simulations. And we will measure the input slope dependency using the chip we designed manually.

Fujita Laboratory

(http://www.cad.t.u-tokyo.ac.jp/)

Automatic Correction of Logic Bugs after ECO

Masahiro FUJITA, Amir Masoud GHAREHBAGHI, Yusuke KIMURA, Peikun WANG, Yukio MIYASAKA, Kentaro IWATA, Xingming LE, Xiaoran HAN

Correction of logic bugs after ECO usually requires changing the functionality of some logic gates as well as changing the topology or connections among the gates. In this work, we have introduced techniques to efficiently accommodate even hard ECO cases, such as changing the functionality for a few minterms of the whole circuit. Our experiments on ITC'99 benchmarks show that we can find the function after ECO after tens of iterations of solving SAT problems even in the case of hard ECO problems. In addition, we have shown the potential application of the method for approximate logic synthesis. Moreover, we have extended our previous method to deal with multiple buggy locations in addition to its efficient implementation. Our program for "Resource-aware Patch Generation", named DEPAG, has won the 3rd prize in the 2017 CAD contest at ICCAD conference (among 38 participated teams in the same track).

Efficient Test Pattern Generation for Different Fault Models

Masahiro FUJITA, Amir Masoud GHAREHBAGHI, Peikun WANG

Traditional test pattern generation (ATPG) methods are not sufficient for the modern LSI chips, as the simple model of single stuck-at fault cannot cover many kinds of defects. Therefore, it is necessary to have efficient ATPG methods for other fault models such as multiple stuck-at fault and bridging fault. In this work, we have introduced efficient methods for test pattern generation for double stuck-at fault model. Moreover, we have introduced a new approach for diagnosing bridging faults. Our experiments on ISCAS benchmarks shows that even in large benchmarks, with a couple of SAT solving, on average, a fault can be diagnosed.

Post-Silicon Debugging of Electrical Bugs

Masahiro FUJITA, Amir Masoud GHAREHBAGHI, Kentaro IWATA

Electrical bugs are an important category of post-silicon bugs that are typically hard to debug due to complex interdependence of layout and netlist as well as their dependency to the running workload and environment. In this work, we tackle the problem of debugging electrical bugs using trace buffers. Given erroneous values captured in the trace buffer due to occurrence of an electrical bug, we try to identify the spatial and temporal location of the error. We have formulated the problem of debugging electrical bugs as a SAT problem and proposed a debugging method based on that. Moreover, we have shown that the existing signal selection methods for logical bugs that are typically trying to maximize signal restoration ratio (SRR) metric, do not perform better than random selection when debugging electrical bugs. On the other hands, utilizing a more sophisticated signal selection that is considering propagation of bit-flips due to electrical bugs is more effective.

Template-Based High-Level Partial Synthesis

Masahiro FUJITA, Amir Masoud GHAREHBAGHI, Yusuke KIMURA, Qinhao WANG

In this work, we have introduced method for C language description generation method based on templates. We have used the method to reconstruct the corresponding C description after ECO in register transfer level (RTL). Starting from the original C description before ECO, which is not equivalent to the design after ECO, we iteratively try to change the portions of the C description until the solution is found, and the new C description becomes equivalent to the design after ECO. Moreover, we have shown application of the method in high-performance computing. In this method, starting from an original description that is not suitable for hardware implementation or acceleration, the design is refined iteratively by using the templates until it becomes ready for hardware implementation/acceleration.

Acceleration of Neural Network with FPGA

Masahiro FUJITA, Amir Masoud GHAREHBAGHI, Tomohiro OKAMOTO

Acceleration of large neural networks is usually not possible by a single FPGA chip. Therefore, we need to utilize multiple connected chips to be able to accelerate large neural networks. In this work, we have introduced methods to efficiently partition computations of a spiking neural network on several FPGA chips connected together in a ring topology. We have shown that with 8 FPGA chips, 6144 (8*768) neurons can be simulated.

Design Automation for FPGAs with Neighboring Communication

Masahiro FUJITA, Amir Masoud GHAREHBAGHI, Tomohiro MARUOKA

In this work, we have presented design automation techniques for special kind of programmable devices (FPGAs) that their internal logic blocks only have communication with neighboring blocks. We have formulated the problem of mapping and routing as integer linear programming (ILP), and introduced heuristics to accelerate solving the problem. We have shown that for medium size ISCAS circuits, efficient mapping and routing is feasible within practical time.

Takamiya Laboratory

(http://icdesign.iis.u-tokyo.ac.jp/)

Energy Harvesting, Wireless Powering, and DC-DC Converters for IoT Nodes.

Makoto Takamiya and Takayasu Sakurai

We present an approach to realize the levitation of a small object with an embedded electronic circuit. Luciola is a light-emitting particle with a diameter of 3.5 mm and a weight of 16.2 mg moving in mid-air in a 10.4 cm x 10.4 cm x 5.4 cm space through acoustic levitation using two 40-kHz 17 x 17 ultrasonic transducer arrays placed face-to-face at a distance of 20 cm and wirelessly powered by 12.3-MHz resonant inductive coupling. The novelty is the acoustically levitated electronic object by the combined application of ultrasonic levitation and wireless powering to the levitated electronic object. To enable the levitation of a particle, a custom IC chip is essential in reducing the size and weight of the particle. In the design of the custom IC chip, a new voltage detector circuit enabling an accurate voltage detection and a correct output during the start-up is proposed to achieve an intermittent lighting of the LED to increase the maximum distance between the transmitter and the receiver coil. Luciola is applied to a self-luminous pixel in a mid-air display and drawings of characters in mid-air are demonstrated.

Programmable Gate Driver IC for IGBT

Makoto Takamiya and Takayasu Sakurai

A programmable gate driver IC for IGBT to dynamically change the gate driving current during the switching of IGBT is developed. In the proposed gate driver, the 6-bit gate control signals with four 160-ns time steps are globally optimized using a simulated annealing algorithm, reducing the collector current overshoot by 37% and the switching loss by 47% at the double pulse test of 300 V, 50 A IGBT.

Integrated Voltage Regulators for Energy Efficient Microprocessors

Makoto Takamiya and Takayasu Sakurai

A 2/3 and 1/2 reconfigurable switched capacitor (SC) DC-DC converter is developed for a per-core dynamic voltage scaling of many-core microprocessors. The power conversion efficiency and the output power density of the SC DC-DC converter in 2/3 mode is degraded, because full-swing and half-swing drivers for power transistors are mixed and the resistive loss of the power MOSFETs with the half-swing drivers is large. To solve the problem, a fully-integrated driver amplitude doubler (DAD) is proposed. In DAD, the gate amplitude of the power MOSFETs is increased from half-swing to full-swing by generating a 1/3 input voltage sampled from a flying capacitor. In the fabricated 2.7-V input SC DC-DC converter mounting four 100-nF 0402 (0.4 mm x 0.2 mm x 0.2 mm) multilayer ceramic chip capacitors (MLCCs) on 180-nm CMOS die achieves the highest efficiency of 92.9% at the output power density of 62 mW/mm2 in the published step-down SC DC-DC converters.

Ikeda Laboratory

(http://www.mos.t.u-tokyo.ac.jp)

Design of High Performance Cryptographic Processor

M. Ikeda, H. Awano, S. Sugiyama, R. Saito, and F. Arakawa

Public key cryptography based on elliptic curve cryptography is widely employed from automobiles to terminal sensor nodes, and performance requirement for cryptographic engines is also diversified. For example, in vehicle-to-vehicle communication, signature generation and signature authentication with extremely low latency and high throughput are required for autonomous driving, so speeding up by hardware implementation of elliptic curve cryptography is becoming important. We have designed and fabricated crypto-processors capable of scalar multiplication which the core operation for elliptic curve cryptography. We optimized the scheduling of pipeline Montgomery multipliers, results in throughput per area by 1.6 times compared with the conventional state-of-the art. Measurement results demonstrates signature generation time of 31.3us, which fulfills requirements of V2V communication. Meanwhile, it is essential to realize small foot-print public key based crypto-engine for sensor nodes. We have optimized radix of multipliers, and minimized temporary variables to realize lowest foot-print crypto-engine.

Design of Functional Cryptographic Processor

M. Ikeda, H. Awano, T. Ichihashi, K. Koga, and C. Cai

We study hardware implementation of functional cryptography, which is capable of, for example, searching among encrypted data or statistical processing without decryption along with secure communication, and lattice-based cryptography, which has gained increasing attention as quantum computers are emerging. One of the most important primitives for functional cryptography is a computation called pairing, whose computational complexity prevents many schemes to be feasible, 210us for each pairing even with state-of-the-art CPUs. We studied a wide range of sub-algorithm and architectural possibilities and showed that with dedicated hardware a pairing can be computed under 40us. On the other hand, we are also investigating efficient hardware implementation of Paillier encryption, which is a additive homomorphic cryptosystem widely used in the field of biometric authentication, and high-speed implementation of lattice-based encryption for the post-quantum era. Examining the degree of paralellism and area cost for the number theoretic transform (NTT), which is the core algorithm for lattice-based cryptography, we implemented an evaluation chip.

Evaluation of attack resistance of PUF Using Deep Learning

M. Ikeda, H. Awano, and T. Iizuka

Recently PUF (Physically Unclonable Function) has attracted a lot of attention as a method that is low cost and secure device authentication. Among PUFs, Double-Arbiter PUF (DAPUF) is known to be highly resistant to modeling attacks. We proposed a deep neural network-based modeling attack for DAPUF and evaluated the resistance of that. Our model successfully predicted responses to unseen challenges with probability of 88.4%, which is 21.1% higher than the conventional method. Those results highlight an important fact that PUF-based authentication schemes should be carefully designed considering the rapid evolving machine learning technology.

A Weak-Signal-Readout Integrated Circuit for Terahertz-Video-Imaging

M. Ikeda, H. Awano, T. Kikkawa, and E. Kume

For Terahertz-Video-Imaging, we designed a readout integrated circuit (ROIC) which converts a weak signal detected by InAs MOS-HEMT to digital signal. The ROICs which contain low noise amplifier, lock-in amplifier and $\Delta\Sigma$ analog-to-digital converter are integrated as 8x7 array on 180 nm CMOS and utilized with the detectors stacked on them. On the chip, digital-to-analog converters are also implemented adjacent to the ROICs to calibrate the detectors. In our work, several control parameters and digitized signals are serially communicated by serial peripheral interface. As a future work, we will demonstrate the ROIC with stacked detectors for the imaging.

Advanced 3-D Measurement System by Smart Image Sensors and Secure Sensing

M. Ikeda, H. Awano, U. Kim, V.G. Vishwa, and N. Takeda

We are trying to propose new methods for 3-D measurement, with advanced functionality, and secure sensing. In 3-D measurement, we have proposed a new method and a image sensor with the capability of selective light detection and background suppression, and are fabricating and measuring a CMOS image sensor in which polarizers are discretely arranged in specific pixels to obtain polarization information necessary for detection of specular reflection. Towards secure sensing, we are trying a unified architecture, merging the functions of A/D conversion and data encryption and authentication.

Mita Laboratory

(http://www.if.t.u-tokyo.ac.jp)

Programmable Matter - Study on LSI-MEMS energy-autonomous distributed microsystems for realization of deformable matter

Y. Mita, N. Usami, G. Ulliac,
E. Lebrasseur (LIMMS, CNRS-UTokyo IIS),
J. Bourgeois, B. Piranda (FEMTO-ST, France),
S. Delalande (PSA-Peugeot)

As one example of integrated MEMS that is expected to open new research and industrial application fields, the authors are trying to show a top-down application of energy-autonomous distributed microrobots. A number of identical tiny robots, sized below 1 cm, will be released in an environment. Individual robot can communicate with their neighbor, can stick each other, can share energy, to realize cooperative function. The PI has received a French National Research Center (ANR) grant on behalf of host professor of CNRS laboratory in the Institute of Industrial Science (LIMMS, CNRS-IIS, UMI 2820), together with FEMTO-ST Laboratory and PSA-Peugeot Laboratory for such "micro robots that can realize deformable substance by cooperative action, named Programmable Matter". Target is set in understanding on physics and devices working in aqueous environment.

Top-down fabrication of small-gap electrode devices by Fine E-Beam writing and MEMS process

Y. Mita, Y. Takeshiro, N. Washizu, A. Takada,
M. Fujiwara, T. Sawamura, R. Ikeno, and K. Asada

Towards the goal of production of brand-new sensor devices with higher sensitivity and functionality, the team is working on small-gap electrode fabrication process. The team takes full advantage of newly-acquired (in 2013) rapid electron beam writer F7000S-VD02. The capability of high electron dose and sharp edge due to cell (character) projection machine configuration is used for fabrication process. The target of first year is reliable sub 100 nm gap electrode fabrication, as well as microactuator-integrated nanogap system.

University-Industry collaborative research on highly-functional system by MEMS post-process of CMOS-VLSI

Y. Mita, S. Inagaki, T. Kuriyama,
Y. Nakayama (Konica Minolta), Y. Sato (Nanox Japan)

The research targets are new sensor devices, made by post-process at clearnrooms such as VDEC Takeda Supercleanroom and others, of VLSI wafer made through VDEC. The important finding has been that VLSI wafer acquired just after transistor fabrication could sustain processes even with heat treatment, such as deposition, ion implantation, and drive-in. In 2016, a VLSI device made on Silicon-on-Insulator (SOI) wafer was successfully Deep-RIE processed. The industrial interest is its versatility–many different types of application devices, which differ one from another according to request of market, can be fabricated by using the same technology. More and more companies are interested in the scheme and are working on the technology on the collaborative research projects.

LSI hot-spots active cooling system

Y. Mita, Y. Okamoto, K. Fujimoto (Titech),
H. Ryoson (Titech), and T. Oba (Titech)

A hotspot, which is referred to a high-temperature area due to the overheating of a circuit block that excess passive cooling capability, is becoming a key limiting factor of LSI performance. An active cooling system that tries to actively remove such local heating by circulating liquid coolant is our research target. In FY2016, an out-of-plane cooling scheme was confirmed

to be efficient for heat removal, by test structure experiments, modeling with equations, and finite element method simulations.

Assessment of Critical Dimension by direct Laser patterning

Y. Mita, N. Usami, A. Higo, Y. Okamoto

Direct patterning using UV Lasers has potential to become an ultimate short Turn Around Time (TAT) fabrication method with because it can suppress lithography step. To further extend its resolution down to beyond 10 μm, assessment of systematic and random size variability is mandatory. We have therefore developed a test structure design to electrically measure and extract discrepancy between designed and realized dimensions. Precision that can go down to 1 μm has been obtained.

"Zeolite-Electronics-Nanostructure (ZEN)" integrated chemical sensor

Y. Mita, K. Yamada, Y. Okamoto,
M. Denoual (ENSI de Caen, France),
Tixier Mita Agnès, Eric Lebrasseur,
Hussein Awala (ENSI de Caen, France),
Julien Grand (ENSI de Caen, France),
Sveltana Mintova (ENSI de Caen, France)

One of the most important application field of MEMS is sensors that can detect physical and chemical amount that cannot be sensed by human beings. Following a long history of the group's research, the team was appointed in 2015 as a JSPS-CNRS bilateral cooperative research project grant. The goal of the research is to develop a chemical sensor by integrating Zeolite material that is new to VLSI, and applying post-process on it. Within one year, the team have successfully demonstrated two types of devices: a zeolite chemical sensor by resonant frequency shift detection, and by thermal capacity change detection according chemical concentration. A reliable embedding method of zeolite into 3D silicon MEMS trenches have been developed as well.

"Zeolite-Electronics-Nanostructure (ZEN)" integrated chemical sensor

A. Higo, N. Usami, Y. Okamoto,
K. Yamada, (LIMMS, Mita Laboratory)
W. Haibin, N. Kubo, K. Segawa,
M. Sugiyama, (Next PV, CNRS-UTokyo RCAST)
Y. Mita

Electron devices using colloidal quantum dots are believed to open new application fields such as light emitting devices and or photovoltaics. Up to date, very few research activities have been done in sensors applications; if we can realize integrated photodiodes that have extended sensitive wavelength as long as 1. 35 μm-1.4 μm wavelength, such devices can be used by many new applications such as security cameras and / or Laser Radar (Lidar) under sunlight. The aim of this research is to find an integration method for beyond Si-LSI device. We try to integrate colloidal quantum dots of which absorption spectra can be designed through molecular design. By integration, Silicon device will be able not only to capture infrared wavelength lights, which is impossible by its original characteristics, but also my include information reading and computation circuits. For the first year's exploratory study, partly financed by the LIMMS internal project grant, spin coating integration method has been investigated. The enhancement of absorbance spectra at such wavelength has been experimentally confirmed.

Development of shock resonant spectrum (SRS) sensor for cyber physical system

Y. Mita, R Ranga Reddy, N. Usami

VDEC is awarded a Japanese JST–Indian DST joint grant (SICORP) for cyber physical systems research, in cooperation with IIT Bombay campus. The team is participating the project through a Shock Resonant Spectrum (SRS) sensor, which has been a research theme of 2012-2014. A new Ph. D student from India is assigned and fabrication process was recovered. This year we have developed microactuators included test structure to extract static and dynamic friction coefficient of DRIE walls.

Development of LSI post-processing for hybrid integration

Y. Mita, X. Hurtaud E. Ohta, T. Momose (Material Eng.)

To provide new capability to Nanotechnology Platform Users, a couple of process technologies for LSI hybrid integration is under development. In FY2016, a stable gold electroplating system was purchased and a bump plating for LSI flip-chip bonding was developed. In parallel, a supercritical fluid deposition (SCFD) machine was restored to investigate trench embedding deposition with metal. This year, we have found a condition of SCFD over trenches covered with silicon dioxide.

Takagi-Takenaka Laboratory

(http://www.mosfet.k.u-tokyo.ac.jp/)

III-V/Ge Metal-Oxide-Semiconductor (MOS) FETs and the 3 dimensional integration

S. Takagi, M. Takenaka, WuKang Kim, Ke Mengan, Kwangwon Jo, Cheol-Min Lim, Tsung-En Lee, Sanghee Yoon, Chiaki Yokoyama, Zilong Wang, Kei Sumita

We have conducted the research on high-performance III-V/Ge MOSFETs and the 3 dimensional stacked CMOS structures by using these high mobility MOSFETs. For reliability of InGaAs MOS interfaces, we have found that amounts of interface states at InGaAs MOS interfaces generated by electrical stress have correlation with substrate hole currents of InGaAs n-MOSFETs, suggesting a hole-triggered mechanism of interface states. For Ge MOSFETs, we have found that thinning SiGe layers in SiGe/SOI substrates used for Ge condensation significantly increases compressive strain in Ge-on-Insulator structures, leading to the realization of SiGe-OI pMOSFETs with high hole mobility.

Tunnel FET

S. Takagi, M. Takenaka, Huang Po-Chin, Kimihiko Kato, Takahiro Gotow, Taeeon Bae, Daehwan Ahn, Ryotaro Takaguchi

We have investigated tunnel FETs (TFETs) which can exhibit steep subthreshold slope for low-power operation. Lateral InGaAs TFETs, Ge TFET, GaAsSb/InGaAs hetero-junction, Ge/strained Si hetero-junction and ZnO/(Si, Ge) TFETs have been explored. It was found that abrupt np junctions in Ge can be formed by P diffusion and the Ge p-channel TFETs using these source junctions operates. Also, we have proposed novel oxide semiconductor/column-VI semiconductor hetero-structure TFETs utilizing vertical tunneling. We have fabricated these ZnO/Si and ZnO/Ge n-channel TFETs and demonstrated the operation.

Ferroelectric gate insulator MOSFETs

S. Takagi, M. Takenaka, Kimihiko Kato, Kiyoshi Endo, Ichitaro Fukui, Masashi Yamaguchi

We have conducted the research for MOSFETs using ferroelectric gate insulators. We have confirmed ferroelectricity of ALD $HfZrO_2$ films on Si and the operation of MOSFETs with these gate insulators. On the other hand, the physical origin of the ferroelectric hysteresis and reduction in S factors of MOSFETs with ALD La_2O_3 is found to be attributed mainly to drift of any ions in the La_2O_3 gate insulators.

Si CMOS photonics

M. Takenaka, S. Takagi, Frederic Boeuf, Qiang Li, Ziqiang Zhao, Takumi Fujigaki, Dongheng Lyu, Yoshitaka Taguchi

We have conducted the research for MOS-based Si optical modulators. We have successfully demonstrated that the III-V/Si hybrid MOS optical modulator exhibits 10 times smaller modulation loss than Si MOS modulator. As a result, we have revealed that the III-V/Si hybrid MOS optical modulator is suitable for high-speed optical interconnect beyond 50 Gbps. Moreover, we have demonstrated an optical switch based on the III-V/Si hybrid MOS optical phase shifter, suitable for optical deep learning using an universal photonic integrated circuit. We have also conducted the research of the mid-infrared photonic integrated circuits based on Ge-on-Insulator (GeOI) wafer fabricated by wafer bonding. We have successfully demonstrated a suspended Ge waveguide for the first time by removing a SiO_2 buried oxide underneath the Ge waveguide.

III-V CMOS photonics

M. Takenaka, S. Takagi, Naoki, Sekine,
Pengyuan Cheng, Takaaki Sanjoh

We have investigated the III-V CMOS photonics platform by using III-V on insulator wafer. On the III-V-OI wafer, III-V MOSFETs and III-V photonics can be monolithically integrated. We have numerically analyzed the InGaAsP depletion optical modulator which exhibits superior modulation characteristics to Si optical modulator. To improve the heat dissipation of III-V-OI platform, we have proposed the III-V on SiC platform. By making III-V on SiC wafer by wafer bonding, the heat dissipation was significantly improved.

2D material devices

M. Takenaka, S. Takagi, Yuki Yamaguchi,
Masashi Yamashita, Hanzhi Tang

We have investigated 2D materials such as graphene and MoS_2 for semiconductor devices. We have numerically analyzed graphene optical phase modulator. It was found that pure optical phase modulation can be obtained by suing mid-infrared wavelength.

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