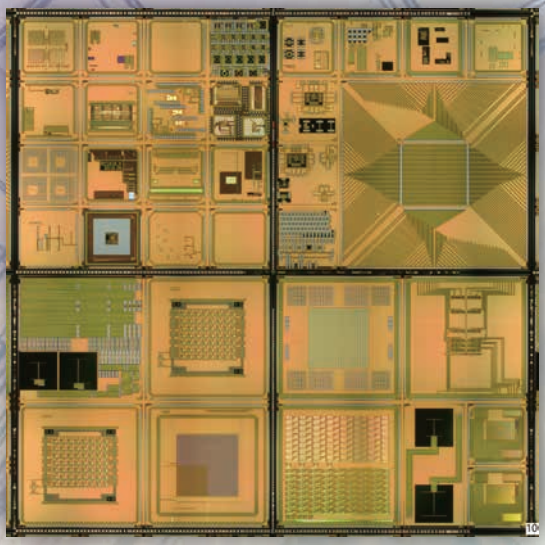
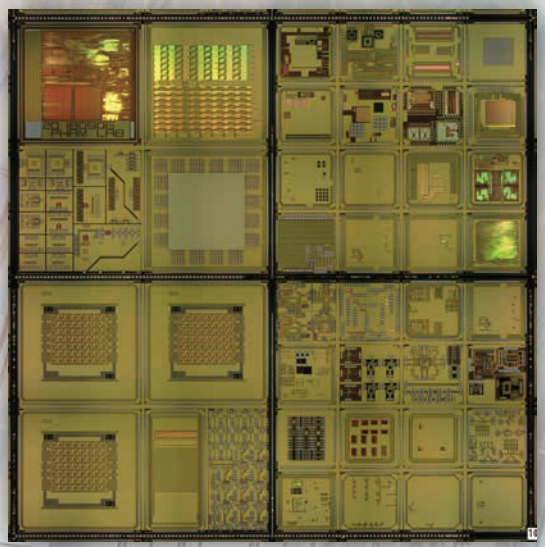
平成31年度

東京大学
大規模集積システム設計教育研究センター
年　報

2019
VLSI Design and Education Center, The University of Tokyo Annual Report





2019
VLSI Design and Education Center,
The University of Tokyo

The first director, Prof. Hoh and the previous director, Prof. Asada have made VDEC as one of the most important and widely used organizations in Japanese academia for VLSI chip/device design and development. Annually more than 300 research groups in academia use the design tools provided through VDEC, and more than 200 research groups use various facilities including clean rooms and measurement tools for chip development.

Semiconductor industry has been continuously growing since the last century and is expected to continue to grow with the increasing need from IoT, AI chip, and related technology. It is extremely important to support academia as it is the base of semiconductor industry. There are several organizations in the world, specifically in US, Canada, Europe, South Korea, and Taiwan, and others, whose goals are essentially the same as VDEC. Some of them has increases its size significantly in recent years. There have been international efforts in the collaboration among these organizations. Every year, multiple meetings to discuss collaborative ways to supply various services for world-wide VLSI chip design and development are set up, and more intensive joint activities are expected to come.

D2T (Design to Test) which is an industry donated division in VDEC has been working for nearly twelve years and has received a number of world top-level visiting professors. D2T has already stimulated educational and research activities of VLSI testing in broad sense and has generated several results which have actually influenced the VLSI testing area world-wide. It is expected to continue to generate more influential results in VLSI design and testing.

VDEC has become an essential organization for academic VLSI chip/device design and development. It is now highly expected that VDEC gives essential contributions on the university as well as the industry through a well-thought expansion that keeps the efficiency and flexibility of VDEC. For that achievement, VDEC including myself appreciates your continuous support.

VLSI Design and Education Center, University of Tokyo

Director **Masahiro Fujita**

藤田昌宏

2019
VLSI Design and Education Center,
The University of Tokyo
Annual Report

C O N T E N T S

Chapter1 Activity Report of VDEC

1.1 Introduction of VDEC activities and activity report of FY2018

VLSI Design and Education Center(VDEC), University of Tokyo was established in May 1996. VDEC has been operating for the following 3 major roles: "spreading the latest information on VLSI design and education," "providing licenses of CAD tools," and "supporting on VLSI chip fabrications for academic use." The VDEC activity report of FY 2017 is described hereafter according to Fig. 1.1.

The missions of VDEC are for advancement of researches and education on LSI design in public and private universities and colleges in Japan and send many distinguished VLSI designers into industry. After 23 years of VDEC establishment, educations on CAD software, LSI design and design flow in universities have been well established. On the other hand, advancement on nano-meter CMOS technologies forces design flow and CAD software complicated. We have been continuing CAD tool seminar by the lecturers from EDA vendors for twice a year. We hold the seminar in VDEC and provide distance learning through video streaming. We expect spread of the up-to-date LSI design methodology by using CAD tools.

We assume our LSI design flow seminars as educations on basic LSI design concepts and practical experience of LSI design with CAD tool chain. VDEC holds "LSI design education seminar", a.k.a. VDEC Refresh Seminar, once a year. This year we hold 3 courses, "Analog design course" and "RF design course", and initiated "MEMS design course" in July-September time frame. We invite experienced professors among universities as lecturers for the courses to conduct LSI design education courses with practical experience. We also hold "Transistor level design flow in VDEC" and "Digital design flow in VDEC EDA environment" for designers in universities. We started to charge these two LSI design education courses, as well as VDEC Refresh Seminars.

In addition to the above seminars, we hold "VDEC De-

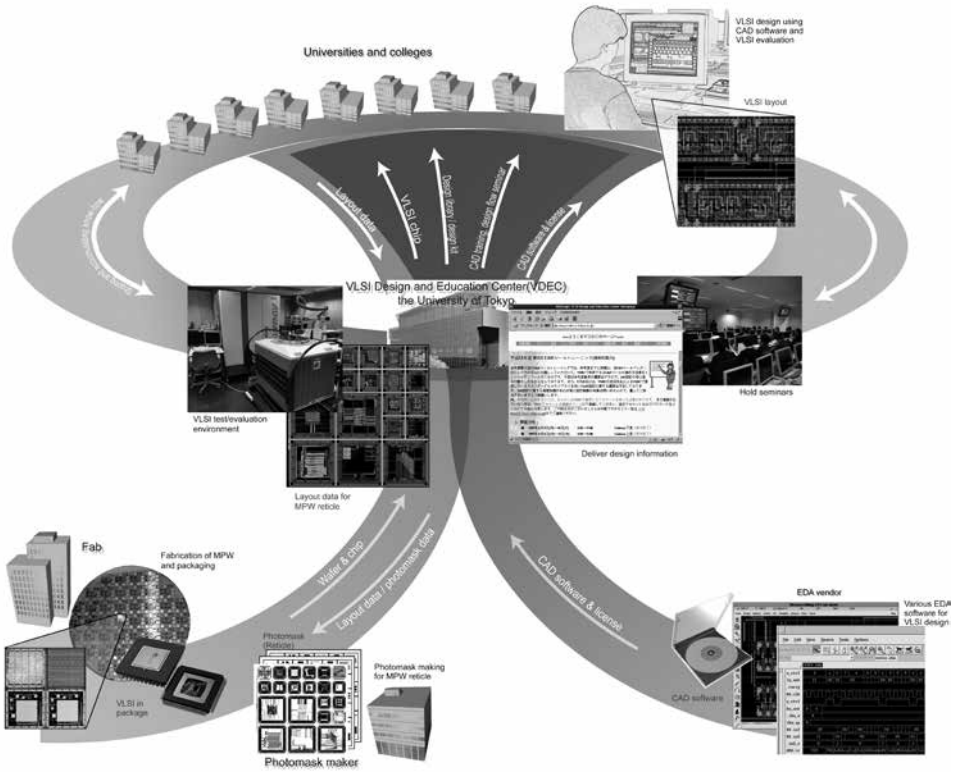


Fig. 1.1 VDEC activities

signer' Forum" among young professors and students annually. This is a workshop that the participants exchange their design examples with not only success stories but also their failure stories, in addition to invited talks. We expect students and professors who will start designs to learn kinds of know-hows. We have initiated "IEEE SSCS Japan Chapter VDEC Design Award" this year, and final examination and awarding have carried out during the "VDEC Designer' Forum". Ms. Y. Kanazawa(Hokkaido Univ.) is awarded as "IEEE SSCS Japan Chapter VDEC Design Award" winner, and Ms. S. Yokoyama(Hokkaido Univ.), Mr. A. Kameyama(Nara Institute of Science and Technology), and H. Liu(Tokyo Institute of Technology) are awarded as "the best VDEC Design Award", and Ms. S. Tajima(Waseda Univ.), H. Kawauchi(Shizuoka Univ.), and T. Ikegami(Hokkaido Univ.) are awarded as the "VDEC Design Award."

LSI designers come up against various difficulties during actual LSI design scene, even after the basic educations through various seminars and the forum. One of the biggest problems for beginners is the setup of CAD softwares. Many of them also get confused by "Esoteric messages" come out from CAD softwares, even after they successfully setup CAD tools. In such situations, VDEC mailing-lists make significant contributions. VDEC users can register to VDEC mailing-lists on CAD tools, and process dependent groups through VDEC web pages, and can ask questions and helps on their facing issues. It is not a responsibility for the registrant of such mailing-lists to give answers to questions, however, in most cases, replies are given by the experienced users of CAD tools and experienced designers within a couple of hours to a couple of days. Moreover, emails are accumulated and are open to the VDEC users, as shown in Fig. 1.2, who have registered VDEC accounts, as the important educational assets. We expect all the VDEC users to make the full use of this mechanism to help solve problems.

We continue chip fabrication services on FDSOI CMOS 28nm by ST Microelectronics, 0.18mm CMOS by Rohm and 0.8μm CMOS by On-semi Sanyo Semiconductor. And started chip fabrication services on SOTB CMOS 65nm by Renesas Electronics.

Our donated division "Design To Test(D2T)", which was founded by donation from Advantest in Oct. 2008, focuses on enrichment of education on LSI testing and bridging between design and testing.

Fig. 1.3 shows trends of number of papers through VDEC activities. Number of papers is increasing, which means researches in the field of VLSI design have been encouraged after VDEC establishment.

Fig. 1.4 shows number of papers related to CAD usage, chip fabrications and VDEC facility usages. CAD tools are widely used to write papers. CAD tools are used not only chip designs themselves but also used for preparation of chip fabrication and they contribute to verify fundamental ideas of researches. Advanced CMOS processes are preferred for publications, and not only papers with 65nm/40nm CMOS chips, but also with 32nmCMOS,

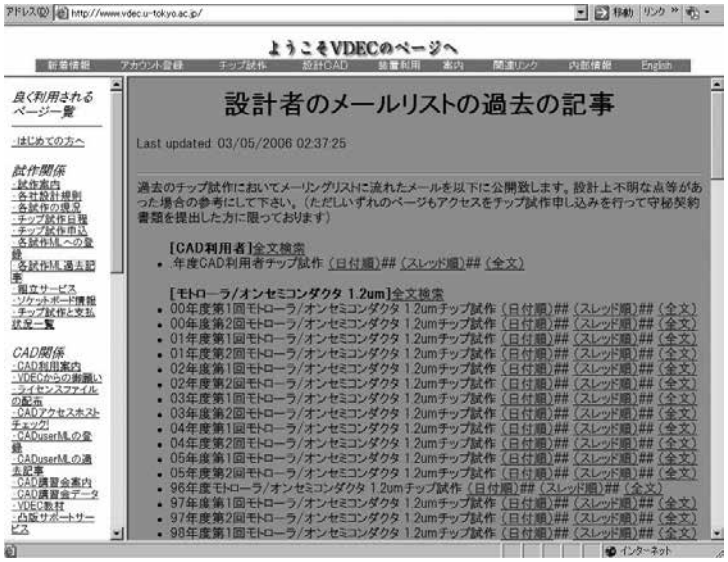


Fig. 1.2 Archives of emails of VDEC mailing-list.

22nmCMOS and 14nmCMOS are emerging in the world. We would like to prepare chip fabrication services for the advanced CMOS processes. In addition, we would like to setup chip fabrication services related to CMOS/MEMS to fulfill the researches for "More than Moore". We also encourage researchers to fully use of VDEC facilities such like LSI testers, FIB systems and EB writr for the wide spread of research purposes.

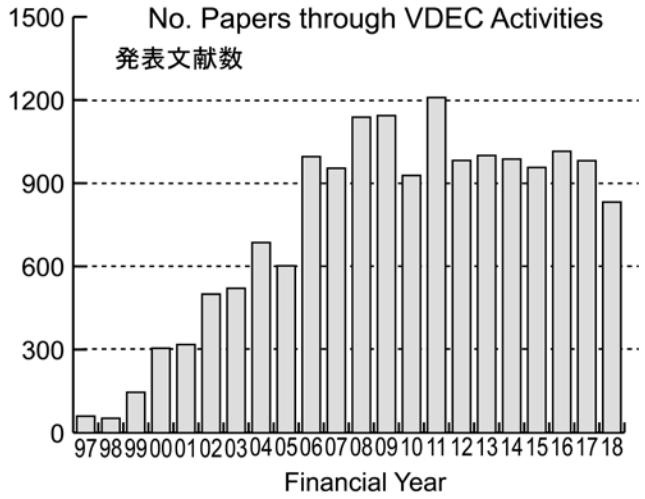


Fig. 1.3 Trends of number of papers through VDEC activities.

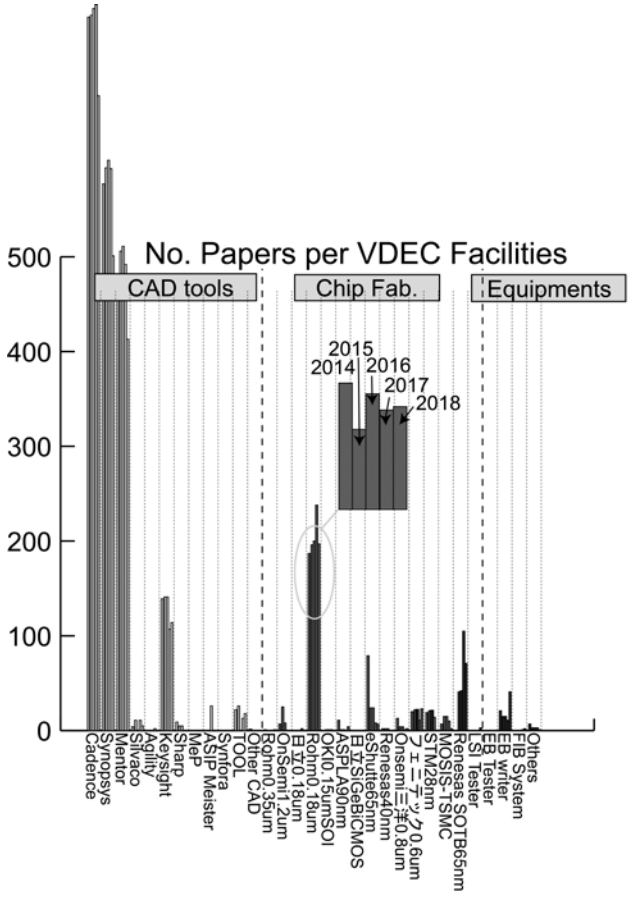


Fig. 1.4 Number of papers related to VDEC facilities.

1.2 VDEC CAD Tools

Since 1996, VDEC has provided CAD software licenses to the registered researchers in universities and colleges in Japan. The CAD tools we provided in 2019 are shown in Table 1.2.1. The researchers can use those CAD tools when their local machines, whose IP addresses are registered in advance, are authorized by one of VDEC license server located in the ten VDEC subcenters shown in Figure 1.2.1. For each CAD tool, VDEC provides 10-100 floating licenses. Those CAD tools can be utilized only for research and education activities in national universities, other public universities, private universities, and colleges.

When one is going to use VDEC CAD tools and chip fabrication service (the details are described in Section 1-3), some faculty member of his/her research group in a university or a collage needs to do user registration. Figure 1.2.2 shows (a) the number of registrants, (b) the number of distinguished universities/colleges of the registrants, and (c) the number of registrants who applied VDEC CAD tools, (d) the number of applied licenses of all CAD tools.

Table 1.2.1 VDEC CAD tools

Name	Function	Vendor
Cadence tool set	Verilog-HDL/VHDL entry, Simlation, Logic synthesis, Test pattern generation, Cell-based (including macros) place, route, and back-annotation, Interactive schematic and layout editor, Analog circuit simulation, Logic verification, Circuit extraction	Cadence Design Systems, Inc.
Synopsys tool set	Verilog-HDL/VHDK simulation, Logic synthesis, Test pattern generation, Cell-based (including macros) place, route, and back-annotation, Circuit simulation, Device simulation	Synopsys, Inc.
Mentor tool set	Layout verification, Design rule check	Mentor Graphics Co. Ltd.
Silvaco tool set	Fast circuit simulation	Silvaco
ADS/Golden Gate	Design and verification of high-frequency circuits	Keysight Technologies
Bach system	BachC-based design, synthesis, and verification	Sharp
LAVIS	Layout visualization platform	TOOL

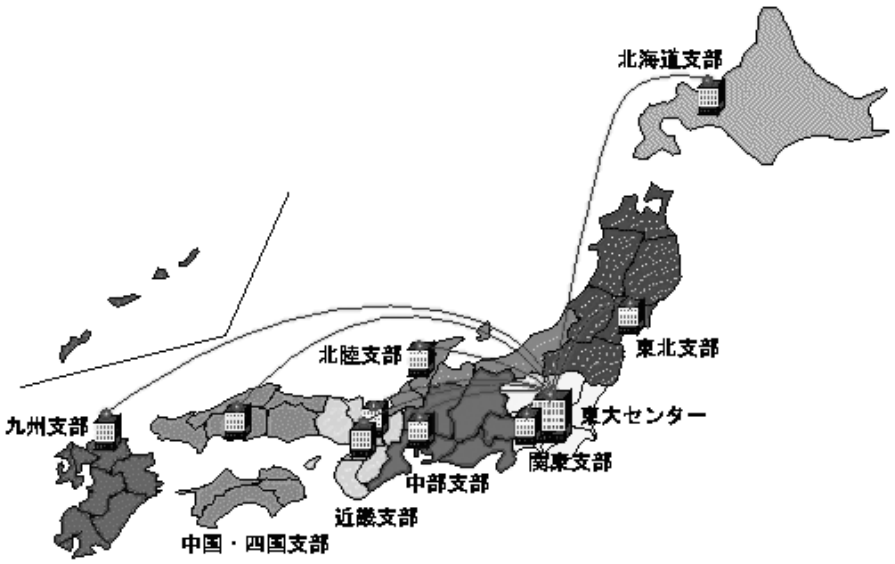


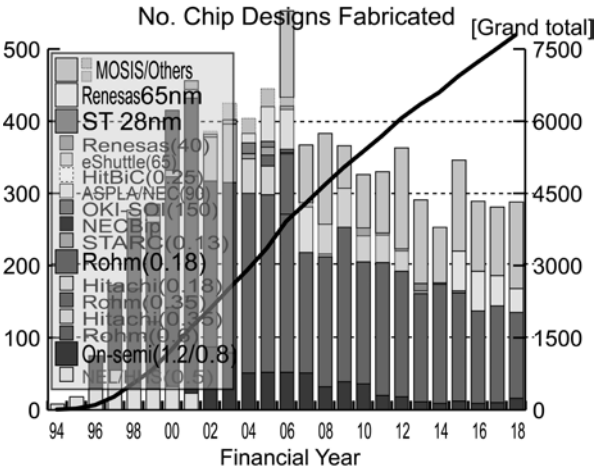
Fig. 1.2.1 VDEC Subcenters

1.3 VLSI Chip Fabrication

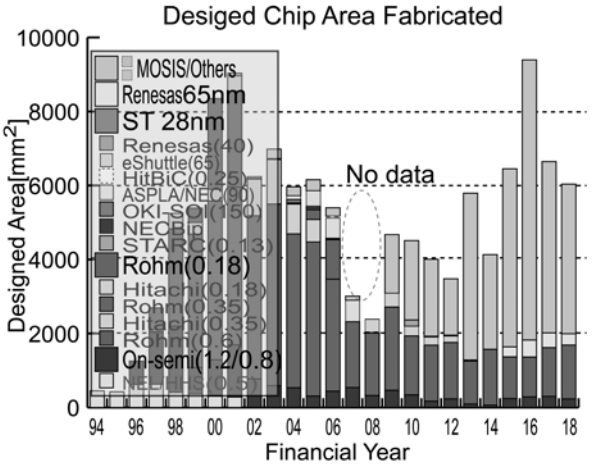
1.3.1 Trends of VLSI Chip Fabrication Services

Fig. 1.3.1 shows a trend of number of designed chips for VDEC chip fabrication services, including pilot project prior to VDEC establishment.

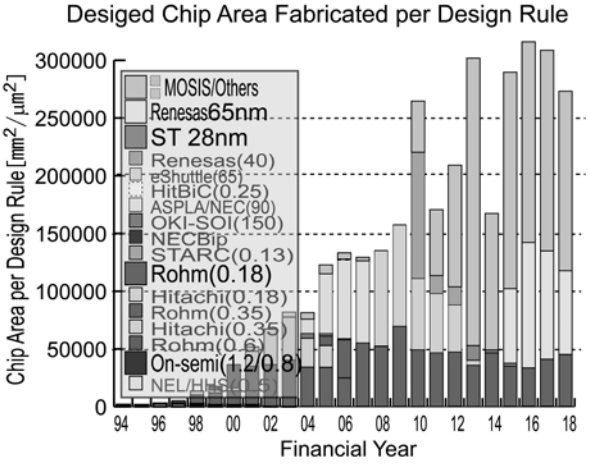
VLSI chip fabrication is limited to 0.5mm CMOS provided by NTT Electronics during the pilot project in 1994 and 1995. VDEC chip fabrication had started in 1996 with 1.2mm CMOS provided by Motorola Japan, which is now On-Semiconductor as well as the 0.5mm CMOS. In 1997, VDEC received cooperation from Rohm and has started 0.6mm CMOS process. In 1998, VDEC started chip fabrication services of 0.35mm CMOS by Hitachi, and in 1999, VDEC started 0.35mm CMOS by Rohm. We had a test chip fabrication of 0.13mm CMOS by STARC through "IP development project" in 2001. We added 0.18mm CMOS by Hitachi into our chip fabrication menu in 2001. From 2002, we started VDEC-MOSIS chip fabrication program initiated by Prof. Iwata of Hiroshima University. Under this program, VDEC member can access to TSMC and IBM processes with lower price. We also started Bipolar chip fabrication by NEC Compound Semiconductor Devices. In 2004, we started 0.15mm SOI-CMOS chip fabrication by Oki Electric as test chip fabrications. In the same year we started 90nm CMOS chip fabrication by ASPLA/STARC. In 2006, we started 0.18mm CMOS by Rohm and 0.25mm SiGeBiCMOS by Hitachi. In 2008, we started 65nm CMOS process by eShuttle, after closure of 90nm CMOS chip fabrication in 2007. In 2010, we started 40nm CMOS process by Renesas Electronics through "Next Generation Semiconductor Circuits & Architecture" project between METI and STAR. On the other hand, 1.2mm CMOS chip fabrication program came to end by the September 2011. 40nm CMOS by Renesas Electronics and 65nm by eShuttle also come to end by Oct. 2012 and Aug. 2013, respectively. We started CMOS0.8μm in Oct. 2012 by On-semiconductor-Sanyo as a test chip fabrication and opened it as the regular chip fabrication menu in 2012. We started FD-SOI 28nm CMOS by ST-Microelectronics through CMP, France, as the advanced CMOS process in 2013. We started SOTB 65nm CMOS by Renesas Electronics in 2015. We initiated two more chip fabrication trials in 2017, on CMOS 0.6um HV from Ricoh, and CMOS 40nm



(a) Trend of number of designs fabricated.



(b) Trend of designed area.



(c) Trend of designed area normalized by design rule.

Fig. 1.3.1 Trend of number of designs and designed chip area.

from Mie Fujitsu.

Fig. 1.3.1(a) shows trends of number of chip designed for VDEC chip fabrication. For the first 6 years until 2001, the number of designed chips shows steady increase, which means drastic improve of the effectiveness researches and education of LSI design, and we assume drastic increase of number of students related to LSI chip design and education. During few years of stable number around 400 chip designs per year, we can see transition of designs toward finer process. In 2007, we saw a large drop, which was caused by sudden process transition from 0.35mm CMOS to 0.18mm CMOS, and in 2008, we also saw another drop by process transition from 90nm CMOS to 65nm CMOS.

Fig. 1.3.1(b) shows trends of designed chip area, which shows much clear trends of drop by process migration. On the other hand, Fig. 1.3.1(c) shows trends of designed chip area normalized by design rule, which assume to be strong relation with design efforts. Coming from the fact that the normalized chip area is still growing, we assume the major reason for decrease of number of chips and designed area is increase of design effort per chip and per unit area due to process scaling.

Fig. 1.3.2 shows trends number of professors and universities fabricated chip. Number of professors who have contracted NDA for process technologies to access design rules and design libraries are, 88, 287, and 48, respectively, for 65nm CMOS, 0.18 mm CMOS, and 0.8um CMOS.

1.3.2 Overview of chip fabrication in 2018

Table 1.3.1 lists chip fabrication schedule in 2018. Please refer to list in Chapter 2 for details of designers and contents of chip designed.

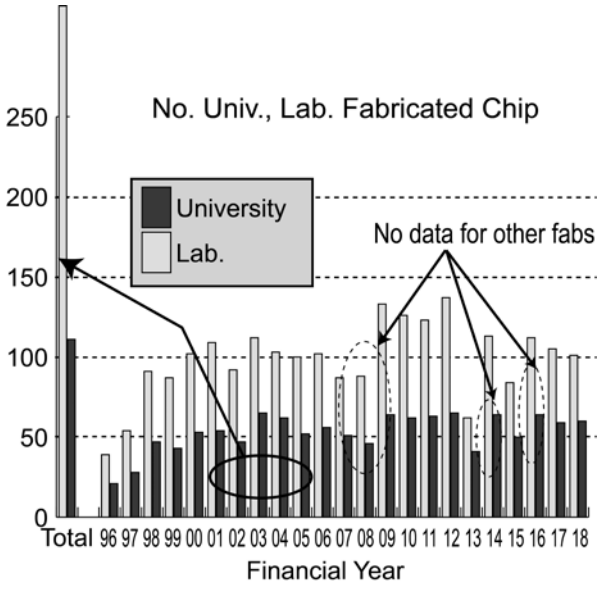


Fig. 1.3.2 Trend of number of processors and universities fabricated chip.

Table 1.3.1 Chip fabrication schedule in 2017

o0.8μm CMOS (On-Semiconductor - Sanyo)

	Chip application deadline	Design deadline	Chip delivery
2018 #1	2018/7/9	2018/9/10	2018/12/24
2018 #2	2019/1/15	2019/3/25	2019/6/E

o0.18μm CMOS (Rohm)

	Chip application deadline	Design deadline	Chip delivery
2018 #1	2018/4/2	2018/6/25	2018/9/26
2018 #4	2018/6/18	2018/9/10	2018/12/14
2018 #2	2018/8/13	2018/11/5	2019/2/15
2018 #3	2018/12/3	2019/2/25	2019/6/3

oSOTB 65nm CMOS

	Chip application deadline	Design deadline	Chip delivery
2018 #1	2018/6/18	2018/7/28	2019/1/28
2018 #2	2018/12/17	2019/2/23	2019/7E

1.3.3 Libraries and design flows

VDEC have been working to prepare design libraries and design flows for digital design and PDKs for analog design. Table 1.3.2 lists libraries available now.

Table 1.3.2 Libraries available for VDEC chip fabrication

Technology	Name	Author	Contents
0.18μm CMOS (Rohm)	Rohm library	Rohm Library Std. Cells, IO cells, RAM (Distributed with CDROM)	Synthesis(Synopsys)
			Simulation(VerilogXL)
			P&R(LEF/DEF)
	Kyodai Library	Onodera Lab., Kyoto University	Synthesis(Synopsys)
			Simulation(VerilogXL)
			P&R(Astro)
	Todai Library	VDEC Design flow based on library prepared by Onodera Lab., Kyoto University	Synthesis(RTL Compiler)
			Simulation(VerilogXL)
			P&R(Encounter)
	PDK	VDEC	PDK(IC6.1)

1.4 Seminar

Seminars are indispensable as the advancement of LSI design technology. In 2018, VDEC has held several seminars and a forum including technical seminar for CAD users, refreshing seminar for working people, and designer's forum for young professors and students.

【Technical Seminar for CAD Users】

In technical seminars for CAD users, VDEC invites lecturers from tool venders including Cadence, Synopsys and Keysight to give lectures on the use of CAD tools. VDEC also provides the courses on the design flow under the VDEC design environment by their staffs. A technical seminar for CAD users for the beginner was held in The University of Tokyo VDEC in August and September in 2018. This seminar took 4 days for 2 Cadence tools, 1 days for 1 Synopsys tool, 1 day for 1 Keysight tool. In addition, VDEC teachers gave lecturers on transistor level circuit design course, and digital circuit design course under the VDEC EDA design environment. Up to 40 students on average attended each course. Moreover, another technical seminar for CAD users for matured teachers and students was held in March by Cadence for 4 days, Synopsys for 3 days (Table 1.4.1). The demand for these CAD technical seminars is large, and VDEC has organized such a large-scale CAD technical seminar toward this situation. The seminar was held in the University of Tokyo and other VDEC branches simultaneously.

Table 1.4.1 CAD technical seminar in 2018 fiscal year

Date	Seminar	Venue	Attendees
8/21	Keysight ADS Fundamentals	The Univ. of Tokyo	8
8/21	Keysight ADS Fundamentals	Nagoya Univ.	4
8/21	Keysight ADS Fundamentals	Akita Prefectural Univ.	6
8/21	Keysight ADS Fundamentals	Shinshu Univ.	11
9/10	Synopsys Verdi	The Univ. of Tokyo	7
9/10	Synopsys Verdi	Kyoto Univ.	2
9/10	Synopsys Verdi	Hiroshima Univ.	1
9/10	Synopsys Verdi	Shinshu Univ.	7
9/18, 19	Cadence Virtuoso Layout Suite-L	The Univ. of Tokyo	18
9/18, 19	Cadence Virtuoso Layout Suite-L	Nagoya Univ.	8
9/18, 19	Cadence Virtuoso Layout Suite-L	Akita Prefectural Univ.	6
9/18, 19	Cadence Virtuoso Layout Suite-L	Shinshu Univ.	20
9/20, 21	Cadence Virtuoso Digital Implementation	The Univ. of Tokyo	15
9/20, 21	Cadence Virtuoso Digital Implementation	Kyoto Univ.	5
9/20, 21	Cadence Virtuoso Digital Implementation	Osaka Univ.	3
9/20, 21	Cadence Virtuoso Digital Implementation	Shinshu Univ.	19
3/1	Synopsys Designer Compiler	The Univ. of Tokyo	18
3/1	Synopsys Designer Compiler	Kanazawa Univ.	1
3/1	Synopsys Designer Compiler	Nagoya Univ.	4
3/1	Synopsys Designer Compiler	Hiroshima Univ.	2
3/1	Synopsys Designer Compiler	Shinshu Univ.	4
3/4	Cadence AMS Designer	The Univ. of Tokyo	14
3/4	Cadence AMS Designer	Kanazawa Univ.	0
3/4	Cadence AMS Designer	Nagoya Univ.	2
3/4	Cadence AMS Designer	Kyoto Univ.	2
3/4	Cadence AMS Designer	Hiroshima Univ.	1

3/4	Cadence AMS Designer	Shinshu Univ.	4
3/6	Cadence Genus	The Univ. of Tokyo	16
3/6	Cadence Genus	Kanazawa Univ.	0
3/6	Cadence Genus	Nagoya Univ.	1
3/6	Cadence Genus	Kyoto Univ.	1
3/6	Cadence Genus	Hiroshima Univ.	3
3/6	Cadence Genus	Shinshu Univ.	3
3/26, 27	Synopsys IC Compiler II	The Univ. of Tokyo	18
3/26, 27	Synopsys IC Compiler II	Kanazawa Univ.	1
3/26, 27	Synopsys IC Compiler II	Nagoya Univ.	3
3/26, 27	Synopsys IC Compiler II	Hiroshima Univ.	3
3/26, 27	Synopsys IC Compiler II	Shinshu Univ.	4
3/28, 29	Cadence Spectre RF	The Univ. of Tokyo	14
3/28, 29	Cadence Spectre RF	Kanazawa Univ.	1
3/28, 29	Cadence Spectre RF	Nagoya Univ.	1
3/28, 29	Cadence Spectre RF	Hiroshima Univ.	3
3/28, 29	Cadence Spectre RF	Shinshu Univ.	8
3/28, 29	Cadence Spectre RF	Akita Prefectural Univ.	3

【Refresh Seminar for Working People】

Teachers of universities and designers in the first line of the enterprise were invited to the lecturer at "VLSI design refresh seminar" which was held aiming at the latest, advanced knowledge and technical learning concerning VLSI design as a refreshing education for working people involved in the integrated circuit industry (Table 1.4.2). Started in year 1998, the seminar has been mainly supported by Ministry of Education Technical Education Division on purpose of giving practicing education of the latest VLSI design technology, it is now being continued with wide support from various societies.

Course A: analog integrated circuit design (6/18-20), Course M1: MEMS design (7/9-10), Course M2: MEMS fabrication (7/23-25), and Course R: RF circuit design (7/18-19). Teachers from industry and universities involved in the integrated circuit research and the education were invited as the lecturers, and they introduced a state-of-the-art and practical VLSI design knowledge and methodology. The participants for the course A, M1, M2, R were 8, 11, 4, 6, respectively.

Fig. 1.4.2 Refresh Seminar at VDEC seminar room at the University of Tokyo, VDEC.

Table 1.4.2 Refresh Seminar

Course A: Analog Circuit Design (3 days)
Analog Circuit Design and simulation Integrated Circuits Verification (LVS, DRC)
Masahiro Sugimoto (Chuo Univ.), Hidetoshi Onodera (Kyoto Univ.), Koji Kotani (Tohoku Univ.)

Course M1: MEMS Design (2 days)
MEMS Basic 1: Fabrication Process MEMS Basic 2: Operation Principle Structural Design Layout Design
Yoshio Mita (Univ. of Tokyo)

Course M2: MEMS Fabrication (3 days)
CAD Design and Analysis Lithography, Etching, Release Vibration measurement and analysis
Yoshio Mita (University of Tokyo)

Course R: CMOS-RF Circuit Design (2 days)
Modulation/Demodulation, Cascaded connection Basic Performance, Transceiver Architecture Circuit Element, Design Flow
Hiroyuki Ito (Tokyo Institute of Technology)

【Designer's Forum for Young Teachers and Students】

VDEC LSI designer forum intended for students and young teachers were held. The VDEC LSI designer forum has aimed to sharing the information that generally hard to be obtained common technical reports or academical papers, such as the failure an LSI designer had been through and the solution, the inside story of CAD industry, and the construction method in the design milieu in the laboratory. In this year, we held the forum in Noboribetsu Hot Spring in September. 27 participants were attended the forum.

Table 1.4.3 Program of Designers Forum in 2018

Sep. 27	Agenda
12:00-12:30	Reception
12:40-14:20	VDEC Design Award Presentation I
14:30-16:10	VDEC Design Award Presentation II
16:20-17:40	VDEC Design Award Presentation III
19:00-	VDEC Design Award Ceremony
Sep. 28	
9:00-10:00	Idea Contest Presentaion
10:00-12:00	Ph.D Session
12:00-13:00	Plenary Talk
13:00-13:10	Closing

1.5 Facilities

The VDEC has been providing the big facilities for universities in Japan from its establishment (1996). Big facilities refer to those which are impossible to acquire and or maintain by an individual research unit. Table 1.5.1 shows the available facilities of VLSI testers and some process machines, which are placed at the tester room (VDEC 104), the super clean room, the backend process room (VDEC 204) of the Takeda building. In 2004, the VLSI tester (T2000) and the EB lithography machine (F5112+VD01) were donated to the VDEC by the ADVANTEST. In the year 2012, VDEC joined MEXT (Ministry of Education)'s Nanotechnology platform to enforce its multi-use capability. (For Nanotechnology Platform refer section 1.8).

Major apparatuses purchased through VDEC and affiliated laboratories courtesy include: 3D Laser microscope (Olympus OLS-5000), Digital Microscopes (Keyence VHX-6000, VHX-7000), Laser direct lithography machine (Heidelberg DWL66+), Parylene Coarter (SCS PDS2010), High Density General Purpose Load-Lock Sputtering Machine (CFS-4EP-LL), and Nickel Electroplating Bath. Also, in collaboration with Faculty of Engineering, an Auger Electron Spectroscopy Apparatus (AES, ULVAC Phi680) is also installed.

The facilities can be used by user himself, after a couple of times' training by attendance of licensed users; also, by presence of licensed persons, a new user can readily use the machine.

Table1.5.1 Available facility list

Facility	Equipment name	Description	Status	Contact
Logic LSI test System	EB tester: IDS10000	The chip surface voltage during operation can be measured with the LST tester. The digital circuit with 384 pins, 1GHz can be tested.	Available	nanotech@so-go.t.u-tokyo.ac.jp
	LSI tester: ADVANTEST T2000	The digital circuit with 256 pins, 512MHz can be tested. Analog test is optional.	Available	nanotech@so-go.t.u-tokyo.ac.jp
	Auto prober: PM-90-A	Automated prober for testing LSI wafers, which can be used with the LSI testers. The probe card for LSIs with the VDEC standard pin connections is available.	Available	nanotech@so-go.t.u-tokyo.ac.jp
Analog/RF measurement system	Analog/RF measurement system: B1500A, 4156B, HP4284, etc	DC parameter measurement, Capacitance measurement, Network analyzer, Spectrum analyzer, etc.	Available	nanotech@so-go.t.u-tokyo.ac.jp
	Low-noize manual prober:	6 inch wafer can be measured with six DC probles and two RF probes upto 50 GHz.		
	Low-noize, temperature controlled semi-auto prober: Süss Microtec	8inch wafer can be measured. The chip temperature range is -50 to 200℃.		

Nanotechnology Platform Apparatuses	Mask lithography, Direct lithography: F5112+VD01	Minimum linewidth: 50nm. Lithography for 5 inch photomask (thickness: 2.3 mm), 2-8 inch wafers, and chips is possible.	Available	nanotech@sogo.t.u-tokyo.ac.jp
	Rapid Mask and Direct lithography: F7000S-VD02	Minimum linewidth: 1xnm. Lithography for 5 inch photomask (thickness: 2.3 mm), 2-8 inch wafers, and chips is possible. Stencil character projection of non-square shapes such as circle, triangle is possible.	Available	
	Chlorine ICP plasma etcher CE-S	High density plasma etching with Cl2 and BCl3 is possible.	Available	
	Silicon DRIE MUC-21 ASE-Pegasus	High speed, high aspect ratio etching of silicon is possible	Available	
FIB system	FIB: SII XVision200TB	Repair of photomask, sample etching, etc. (Through Nanotech. Platform and LCNet)	Available	
LSI FIB system	FIB: FEI V400ACE	Repair of VLSI from both frontside and backside, with CAD navigation and / or IR camera is possible. W/SiO2 deposition is possible.	Available	
Chip Bonding System	Wedge Bonder: Westbond 7476D	25μmϕAl or Au wire wedge bonding machine.	Available	
	Epoxy Die Bonder Westbond7200C	Precision Manupilator system. Epoxy and or Ag paste chip bonding and or glued wiring.		
	Semi-Auto Bonder Westbond4700E	18～25μmϕAu Ball bonding or bump creation.		
	Precision Manual Flip-Chip Bonder Finetech Fineplacer Lambda	Face-to-face bonding up to 15mm square chips. Alignment is through video camera. Bonding is by heating chips with TV camera. (Ultrasonic Unit can additionally be purchased.) XY±0.5μm, and θ=1mrad precision.		

1.6 Activity plan for 2019

VDEC will continue activities on chip fabrication services, CAD tool support, dispatching design related information and donated division "D2T", as has been previous years.

【Design related information dispatching/Seminar】

We will continue holding the following seminars: (1) CAD tools seminars which have been continued since 1997, (2) "Refresh seminar" since 1998, (3) "Designer' Forum" since 1997. We will also continue seminars for LSI tester usage at VDEC and sub-centers, workshops on LSI testing technologies initiated by D2T.

【CAD tool support】

We will continue Cadence tools, Synopsys tools and Mentor tools as the main stream design tools. We will continue analog RF design environment, GoldenGate and ADS by Agilent, C-based design environment, BachC by Sharp. In addition, we continue trial of several CAD tools, such as layout platform, Lavis by TOOL. Design debugging platform from SpringSoft has merged into Cadence tools and will be continued. SmartSpice by Silvaco, will be also continued.

【Chip fabrication services】

We will continue chip fabrication services for SOTB 65nm CMOS by Renesas Electronics, 0.18mm CMOS by Rohm, FD-SOI 28nm CMOS by ST Microelectronics through CMP and 0.8mm CMOS by On-semiconductor-Sanyo as the regular services.

Table 1.7.1 Chip fabrication schedule

【CMOS 1.2μm 2P2M】 On-Semiconductor(Former Motorola Japan)

	Chip application deadline	Design deadline	Chip delivery
2019#1	2019/7/8	2019/9/30	2019/12/23
2019#2	2020/1/6	2020/3/30	2020/6/29

【CMOS 0.18μm 1P5M(+MiM)】 Rohm

	Chip application deadline	Design deadline	Chip delivery
2019 #1	2019/4/1	2019/6/24	2019/10/11
2019 #2	2019/6/17	2019/9/9	2019/12/27
2019 #3	2019/8/5	2019/10/28	2020/2/14
2019 #4	2019/12/2	2020/2/24	2020/6/12

【FD-SOI CMOS 28nm 1P10M】ST Microelectronics

Based on the chip fabrication schedule through CMP.

【SOTB CMOS 65nm】 Renesas Electronics

	Chip application deadline	Design deadline	Chip delivery
2019 #1	2019/6/17	2019/7/29	2020/2/1
2019 #2	2020/1/27	2020/3/9	2020/9/5

1.7 Venture companies related to VDEC

Some professors related to VDEC started venture companies. The following is a list of the venture companies related to VDEC.

[1] AIL Co.,Ltd. (http://www.ailabo.co.jp/)

Related professor : Professor Kazuo Taki, Kobe Univ. (Representative Director)

Description of business : (1) LSI design service
(2) Engineer dispatching service

[2] Synthesis Corporation
(Merged with Soliton Systems on July 1st in 2017, http://www.synthesis.co.jp/)

Related professor : Professor Emeritus Isao Shirakawa, Osaka Univ. (Director)

Description of business : (1) System LSI development and design service
(2) IP development and sales
(3) Development and sales of IPs
(4) Development of EDA tools

[3] ASIP Solutions (http://www.asip-solutions.com/)

Related professor : Professor Masaharu Imai (Representative Director, CTO)

Description of business : (1) R&D, education and consulting of IoT application system
(2) Sales of ASIP design tool and consulting of ASIP development

[4] Nanodesign Corporation (http://www.nanodesign.co.jp/)

Related professor : Professor Kazuyuki Nakamura, Kyushu Institute of Technology. (Representative Director)

Description of business : (1) LSI design and development
(2) Design consulting, etc.

[5] A-R-Tec Corp. (http://www.a-r-tec.jp/)

Related professor : Professor Emeritus Atsushi Iwata, Hiroshima Univ. (Representative Director)

Description of business : (1) Design and measurement of IC and evaluation board
(2) Crosstalk noise analysis
(3) Develop human resources for new employees and beginners

[6] Ishijima Electronics (http://ishi.main.jp/)

Description of business : (1) Electronic circuit and board development
(2) Software development
(3) Consulting

1.8 "Nanotechnology Platform": Ultra Small Lithography and Nanometric Observation Site

VDEC is operating an open-use nanotechnology platform "Ultra Small Lithography and Nanometric Observation Site" together with the Institute of Engineering Innovation of Graduate School of Engineering. The site is supported by Japanese Ministry of Education (MEXT)'s Nanotechnology Platform grant. Any researchers in Japanese Universities, Laboratories, and Companies can take full advantage of The University of Tokyo's cutting-edge nanotechnology apparatuses and know-hows. The accessible technology includes Lithography and Etching environment, Ultra High-Voltage Acceleration (1MV) transmission electron microscope (TEM) that is capable of visualizing upto light materials such as Nitrogen. VDEC takes part in the lithography at Takeda Sentanchi Super Cleanroom. Through VDEC's key apparatus F5112+VD01 donated from Advantest Corporation as well as F7000S-VD02 purchased by national budget, VDEC is supporting post-VLSI activities such as MEMS. The machine is capable of rapidly writing patterns on arbitrary-shaped targets sizing from 1cm-sqare chip to 8-inch round wafers. The performance is measured by the number of research reports and machine use. The University of Tokyo site has received 153 research reports from 139 research groups. As shown in the Fig. 1, usage is monotonously increasing. "Open ratio", which is the number of days in which users outside the University of Tokyo came, divided by machine open days, was 99%. Due to the strong support of nanotech. Platform, even a novice user can obtain fine lithography result by using the apparatuses with the Platform engineering staffs of VDEC. Consequently, free machine time is decreasing so the team is trying to acquire financial support to increase the number of machines. Also from FY2017 to 2018, the French Nanotechnology Network project CNRS-RENATECH asked to the UTokyo VDEC to launch an engineer-class international exchange program. The program is financially fully supported by VDEC's project and one Ph.D-holding research engineer from France (FEMTO-ST, Besançon) is with VDEC Mita Lab for one year.

URL:http://nanotechnet.t.u-tokyo.ac.jp/

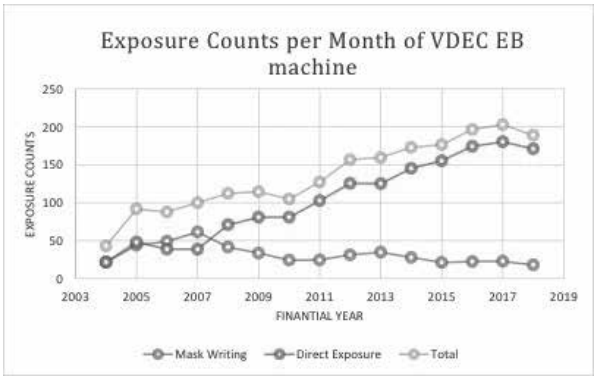


Figure 1: Monthly Average Exposure Count of EB Machine (s).

Chapter2 Activity Report of "ADVANTEST D2T Research Division"

2.1 Introduction of ADVANTEST D2T Research Division

2.1.1 Aim of the establishment of ADVANTEST D2T Research Division

The ADVANTEST D2T research division was established in VDEC in October 2007. As the name suggests, it is financially supported by ADVANTEST Corporation.

The aim of establishment of the ADVANTEST D2T research division is to promote the research and education environment of VLSI testing in all universities and colleges in Japan. "D2T" means that we consider not only design but also testing. Through our activities, we hope to provide expertise in design and testing for the industry. In addition, we are exchanging researchers with other universities and research institutes in both Japan and overseas. Moreover, the D2T research division is suitable for collaborations with the industry because the testing of VLSI is one of the most practical research topics in the industry. Based on these activities, our final goal is to become a center of excellence of VLSI testing in Japan.

The D2T research division has spent 10 years in total for the 1st (Oct. 2007 – Sep. 2010), 2nd (Oct. 2010 – Sep. 2013), and 3rd (Oct. 2013 – Sep. 2016) project phases, and now we are in the 4th phase of the D2T project courtesy of ADVANTEST Corporation.

In this financial year, we invited Professor Adit Singh from Auburn University (2018/1 – 5) and Professor Kalla Priyank (2018/5 – 8) from University of Utah for research and educational collaboration with VDEC.

The details of our group's activities are presented in the following sections.

2.1.2 Members of ADVANTEST D2T Research Division

Project Professor	Masahiro Fujita
Project Professor	Adit Singh (2018/1~5)
Project Professor	Kalla Priyank (2018/5~8)
Project Lecturer	Akio Higo
Researcher	Koji Asami (ADVANTEST Corporation)
Researcher	Takahiro Yamaguchi
Assistant Clerk	Makiko Okazaki

2.2 Report of 13th D2T Symposium

The 13th D2T Symposium was held on September 26th, 2018 at Takeda Hall.

This year, we invited four lecturers from overseas for their work on research topics related to biosystems, RF, IoT and machine learning: Assoc. Prof. Gilgueng Hwang from CNRS, University of Paris-Saclay, Prof. Sule Ozev from Arizona State University, Prof. Abhijit Chatterjee from Georgia Institute of Technology, Prof. Kwang-Ting (Tim) Cheng from Hong Kong University of Science and Technology and Prof. Adit Singh from Auburn University. The symposium also featured lectures by Assoc. Prof. Yasuyuki Ozeki and Assoc. Prof. Agnes Tixier-Mita from the University of Tokyo.

We sincerely appreciate every participant for their contribution at the symposium. We look forward to seeing many participants again at the next symposium.

13th D2T Symposium program

10:00	**Opening Remarks** Masahiro Fujita (Director, VDEC, The University of Tokyo) Toshiyuki Okayasu (Executive Officer, Senior Vice President, New Concept Product Initiative, ADVANTEST Corporation)
10:30	**Session 1** (Chairperson: Akio Higo, VDEC, The University of Tokyo) "On-chip micro/nanorobotic swimmers towards biomedical applications" Gilgueng Hwang (CNRS, University of Paris-Saclay) "Large-scale biological imaging of cells with ultrafast lasers" Yasuyuki Ozeki (Dept. of EEIS, The University of Tokyo) "Thin-Film-Transistor Technology: Display Technology for Biological Applications" Agnes Tixier-Mita (RCAST, The University of Tokyo)
12:30	**Lunch**
14:00	**Session 2** (Chairperson: Tetsuya Iizuka, VDEC, The University of Tokyo) "Ensuring Product Quality through Design for Test for Embedded Circuits" Sule Ozev(Arizona State University) "Power-Performance Aware, Off-Line and On-Line Adaptation of Mixed-Signal/RF Circuits and Systems: A Machine Learning Assisted Approach" Abhijit Chatterjee (Georgia Institute of Technology)
15:30	**Break**
16:00	**Session 3** (Chairman: Masahiro Fujita, VDEC, The University of Tokyo) "Hardware Security - Verification, Test, and Defense Mechanisms" K.-T. Tim Cheng (Hong Kong University of Science and Technology) "Are System Level Tests Unavoidable for High End Processors?" Adit Singh (Auburn University) Session 4 "Activities of D2T research division" Akio Higo (VDEC D2T, The University of Tokyo)
17:45	**Closing**
18:00	**Reception**

2.3 Research Activity Reports of ADVANTEST D2T Research Division

High-Resolution Analog-to-Digital Converter Based on Stochastic Comparators

Takahiro J. Yamaguchi, Parit Kanjanavirojkul, Rimon Ikeno, Tetsuya Iizuka, Kunihiro Asada

This project aimed to implement a high-resolution sub-ranging analog-to-digital converter (ADC) circuit based on stochastic comparators.

Process variations, together with many factors such as variations in voltage or temperature, lead to mismatched design parameters that produce input-referred offsets and hence cause non-linearity and missing output codes in an ADC. Instead of attempting to suppress such process variations as in conventional ADC, the stochastic ADC approach exploits process variations based on the assumption of a Gaussian distribution of comparator offset voltage. We identified the root cause of a voltage bounce of the source nodes of the comparator input PMOSFETs, which introduces a conversion error of the flash ADC circuit at the first stage in our sub-ranging ADC system, as quick signal transition. In order to validate the detection theory using median of probability, numerical experiments have been performed. The experiments use N comparators and detect level-crossing times of a ramp, under the condition of external noise = zero, non-zero internal noise with various process variations.

High-Performance Analog-to-Digital Conversion Using the Wideband Spread Spectrum and Its Application

Koji Asami, Byambadorj Zolboo, Akio Higo, Tetsuya Iizuka, Masahiro Fujita

To measure low-cost RF devices for IoT and other applications, analog-to-digital conversion techniques with a low cost and high efficiency are required. To acquire narrow-band modulation signals scattered in a wide frequency range, a compression sampling method is studied.

In this financial year, a configuration to implement a modulated wideband converter in automatic test equipment (ATE). The theoretical equation of the noise figure has been constructed, and its validity has been confirmed by the simulation. This research results have been submitted to IEEE journal as a technical paper. In the next step, we plan to apply the theory to further investigation of the noise budget in the measurement system, and to develop experimental circuits. We will also investigate the practical issues such as measurement error and compensation methods.

High-Throughput and High-Accuracy Electron-Beam Direct Writing (EBDW) Strategy for Wide Range of EBDW Applications

Akio Higo, Yoshio Mita, Masahiro Fujita

Maskless lithography by electron-beam direct writing (EBDW) is expected to be a low-cost lithography technology with a short turn-around time (TAT), but it has some drawbacks such as a low process throughput and low accuracy against the intended layout shapes. We are pursuing a high-speed and high-accuracy EBDW strategy utilizing the character projection (CP) method to overcome these concerns and to boost EBDW use in fields such as MEMS and photonics.

We investigated the fabrication process for the high-resolution observation of lithographic results by our high-throughput and high-accuracy EB exposure strategy that combines the CP and variable-shaped beam (VSB) methods. A new CP mask for the F7000S EB writing system in the VDEC Takeda Clean Room was designed for further performance improvement. We also measured silicon wire optical waveguides for the propagation loss of dependent on the line-edge (wall) condition.

2.4 Publications

International Conferences, Symposiums, Workshops

[1] Akio Higo, Tomoki Sawamura, Makoto Fujiwara, Etsuko Ota, Ayako Mizushima, Eric Lebrasseur, Taro Arakawa, and Yoshio Mita,"A Micro Racetrack Optical Resonator Test Structure to Optimize Pattern Approximation in Direct Lithography Technologies", 2019 IEEE Conference on Microelectronic Test Structures (ICMTS 2019), Kita-Kyushu, Japan (2019.03)

Chapter3 Research in VDEC

Fujita Laboratory
(http://www.cad.t.u-tokyo.ac.jp/)

"Application of Partial Synthesis to Program Parallelization"

Masahiro FUJITA, Yukio MIYASAKA, Ashish MITTAL

In recent years, many studies have been conducted to apply the partial synthesis method, which has been used for logic circuit synthesis, to program synthesis. In this study, we proposed to synthesize parallel programs from single-threaded programs according to parallel processing environment. For the problem that parallelization of a large program does not end in real time, we reduced the search space of synthesis problem by imposing constraints based on the solution obtained by parallelization of a small program, and the problem became feasible.

An optimization method of systems with template and state transition expression

Masahiro FUJITA, Akihiro GODA

A formal verification of sequential circuits is much more difficult than that of combinational circuits because a sequential comparison of inputs and outputs is necessary in the case of sequential circuits. A formal verification of an FSMD (Finite State Machine with Data-path) is also difficult since it inherently represents a sequential circuit. Therefore, a verification method of an FSMD, “Karfa’s method”, is proposed, which can execute an efficient formal verification of an FSMD although it is false negative. And thanks to that, a partial synthesis method of any systems, “Template-based Synthesis”, became to be able to be applied to an FSMD. In this work, the FSMD synthesis method is proposed with Karfa’s method and Template-based Synthesis. Moreover, we show that the synthesis with the proposed method is possible in the experiments.

High-level description generation method for ECO and its application

Masahiro FUJITA, Amir Masoud GHAREHBAGHI, Qinhao WANG, Yusuke KIMURA,

In VLSI design, ECO (Engineering Change order) may happen after optimizing a gate-level circuit. In this case, designers need to modify the gate-level circuit directly in order to preserve the optimization effort spent so far. In this research, we presented a method to generate a corresponding high-level description utilizing the modified gate-level circuit. The experimental results show that the method can be applied to the AES256 encryption program.

Signal fan-in selection for debugging logic circuit

Masahiro FUJITA, Amir Masoud GHAREHBAGHI, Yusuke KIMURA

When a bug found in gate-level circuit in VLSI design process, the designers sometimes need to modify the gate-level circuit directly with small changes. In this research, it is assumed that the gates (targets) to be modified are known, and the method to select fan-in signals for correction is proposed. Our proposed method can get a good quality solution for multiple targets, and the experimental results show that the method can be applied to the existing benchmark circuits within practical time.

Partial Logic Synthesis

Masahiro FUJITA, Amir Masoud GHAREHBAGHI, Xiaoran HAN

Partial logic synthesis is to synthesize the vacant portions in the given entire circuit and has been formulated with QBF (Quantified Boolean Formula) using LUT (Look up Table). As LUT can practically represent maximum 16 or so inputs, the vacant portions cannot have large number of inputs. In this work, we show a way to partial synthesis by using SOP (sum of product) and POS (product of sum) based QBF formulation. Any SOP/POS formulae with n variables and m products/sums are represented by a set of coefficients which are associated

with literals, and the synthesis problem is to find appropriate values for the coefficients by solving the QBF problems. The SOP and the POS perform better than the previous LUT based QBF method when the vacant portions have more than 16 inputs, however, depending on the circuit, the performance is different. We have performed the partial synthesis experiments on ISCAS89 circuits. The SOP based QBF method can synthesis up to 27 inputs, the POS based method can synthesis up to 24 inputs.

Template-Based High-Level Partial Synthesis

Masahiro FUJITA, Amir Masoud GHAREHBAGHI, Qinhao WANG

In this work, we present a techniques to automatically adjust Register-transfer level (RTL) implementation for Engineering Change Order (ECO) in high level. Our method focuses on the datapath structure, where circuit topologies are mostly, and only partial portions are replaced by programmable datapath. Exploring the correct configuration of the datapath is formulated as Quantified Boolean Formula (QBF) problem, and can be solved by using Satisfiability (SAT) /Satisfiability Modulo Theories (SMT) solver in an incremental way automatically. The experimental results with several example cases have confirmed that effectiveness of the proposed method.

Automatic Test Pattern Generation for Double Stuck-at Faults Based on Test Patterns of Single Faults

Masahiro FUJITA, Amir Masoud GHAREHBAGHI, Peikun WANG

In this work, an improved incremental ATPG method is proposed for DSA faults. Four steps of the proposed method are introduced, including the circuit initialization, ATPG initialization, finding the undetected DSA fault and generating the additional test patterns. According to the experimental results, the proposed method can generate complete test patterns for all the given benchmark circuits, with the processing speed that is more than two orders of magnitude faster than the previous work.

Ikeda Laboratory

(http://www.mos.t.u-tokyo.ac.jp)

Current Research Projects

Design of High-Performance Cryptographic Processor

M. Ikeda, H. Awano, S. Sugiyama, and F. Arakawa

We have studied scalable functional encryption engine applicable for cloud to sensor-nodes. For cloud applications, we have investigated fully homomorphic encryption, which makes any calculation possible to be on cipher-text space, is essential technique for complete secrecy of personal information. But it still needs speeding up for practical use. In this study, we investigated large-scale batch processing of polynomial operations on hardware such as ASIC and FPGA or GPGPU. In ASIC implementation, we achieved 1.45 times faster than CPU implementation. On the other case, in sensor-node, public-key cryptography design in limited hardware resources is required. For example, 256-bit multiplication is divided into several 32-bit or 16-bit multiplications. For further speed and area efficiency, we proposed an implementation of Montgomery multiplication using 256-bit times 2-bit multiplier, and achieved 2.3 times faster and 2.5 times more area-efficient than 32-bit multiplier.

Design of Functional Cryptographic Processor

M. Ikeda, H. Awano, T. Ichihashi, K. Koga, C. Cai, and R. Nakayama

Recently, with the popularization of IoT, the amount of intensive data in the cloud space has increased explosively, and simple data encryption can no more solve a wide range of security risks. Paillier Cryptography is a kind homomorphic, functional cryptograph algorithm, which has additive homomorphic properties, is regarded as a lightweight and high-speed homomorphic cryptography which is expected to be applicable in the areas of e-voting, secure biometrics, and so on. However, authentication and comparison require a huge amount of computational cost for huge amount of data in the database, so performance improvement are essential for the practical use of the the Paillier Cryptography. In

this study, a dedicated hardware architecture for the Paillier Encryption is investigated to improve computational time for Paillier, by utilizing high radix Montgomery multiplication and increasing the degree of parallelism in the encryption process.

Evaluation of Machine Learning Attack Vulnerability for PUF-based Device Authentication System and Examination of Design Guidelines

M. Ikeda, H. Awano, and T. Iizuka

Recently PUF (Physically Unclonable Function) has attracted a lot of attention as a method that is low cost and secure device authentication. Among PUFs, Double-Arbiter PUF (DAPUF) and PL-PUF are known to be highly resistant to machine learning attacks. We proposed a end-to-end deep neural network-based modeling attack for DAPUF and PL-PUF. Our model successfully predicted responses to unknown responses of DAPUF with probability 21.1% higher than the conventional method. Furthermore, we presented that prediction rate of PL-PUF depends on the response bit to be predicted and number of oscillation cycles. Based on experimental results, we examined the design guideline of PUF-based device authentication system to improve machine learning attack vulnerability.

Self-Synchronous Circuits Design

M. Ikeda, and D. Cui

We are working on the research of high throughput gate-level pipeline self-synchronous circuits free from timing errors. The dual-pipeline self-synchronous logic gate duplicates the DCVSL circuit into two identical pipelines and uses the same completion detection signal to control both pipelines. When one pipeline is in the evaluation phase, the other pipeline must be in the pre-charge phase, results in concealing of pre-charge time. Gate-level pipelining enables throughput enhancement. Based on the self-synchronous logic gate, we designed a high throughput self-synchronous arithmetic unit, and a self-synchronous CPU.

A Weak-Signal-Readout Integrated Circuit for Terahertz-Video-Imaging with Global Shutter Operation

M. Ikeda, and T. Kikkawa

We designed a readout integrated circuit (ROIC) for Terahertz-Video-Imaging which converts a weak signal detected by InAs MOS-HEMT to digital signal. The ROICs are integrated as 8x7 array on 180nm CMOS and utilized with the detectors stacked on them. Each ROIC contains low noise amplifier, lock-in amplifier and ΔΣ analog-to-digital converter as well as digital-to-analog converter to calibrate the detectors. In our work, several control parameters and digitized signals are serially communicated by serial peripheral interface (SPI). The SPI also realizes global shutter operation where the ΔΣADC output signals are captured in 8x7 clock cycles and serially read out in following cycles. Moreover, we implemented a temperature sensor by MOSFET whose IV characteristics depend on temperature variation.

Advanced 3-D Measurement System by Smart Image Sensors and Secure Sensing

M. Ikeda, U. Kim, V.G. Vishwa, N. Takeda, and Y. Liu

We are trying to propose new measurement methods, with advanced functionality, and secure sensing. In advanced measurement, we have proposed a new 3-D measurement method and a image sensor with the capability of selective light detection and background suppression, and are fabricating and measuring a CMOS image sensor in which polarizers are discretely arranged in specific pixels to obtain polarization information necessary for detection of specular reflection. Towards secure sensing, we are trying a unified architecture, merging the functions of A/D conversion and data encryption and authentication.

Takamiya Laboratory
(http://icdesign.iis.u-tokyo.ac.jp/)

Switched Capacitor DC–DC Converters Mounting Multilayer Ceramic Chip Capacitors on CMOS Die

Makoto Takamiya and Takayasu Sakurai

2/3 and 1/2 reconfigurable switched capacitor (SC) DC–DC converter is developed for a per-core dynamic voltage scaling of many-core microprocessors. In the fabricated 2.7-V input SC DC–DC converter mounting four 100-nF 0402 (0.4 mm × 0.2 mm × 0.2 mm) multilayer ceramic chip capacitors on 180-nm CMOS die achieves the highest efficiency of 92.9% at the output power density of 62 mW/mm2 in the published step-down SC DC–DC converters.

Programmable Gate Driver IC for IGBT

Makoto Takamiya and Takayasu Sakurai

A programmable gate driver IC for IGBT to dynamically change the gate driving current during the switching of IGBT is developed. In the proposed gate driver, the 6-bit gate control signals with four 160-ns time steps are globally optimized using a simulated annealing algorithm, reducing the collector current overshoot by 37% and the switching loss by 47% at the double pulse test of 300V, 50A IGBT.

Luciola: A Millimeter-Scale Light-Emitting Particle Moving in Mid-Air Based On Acoustic Levitation and Wireless Powering

Makoto Takamiya, Yasuaki Kakehi,
and Yoshihiro Kawahara

We present an approach to realize the levitation of a small object with an embedded electronic circuit. Luciola is a light-emitting particle with a diameter of 3.5mm and a weight of 16.2mg moving in mid-air. The novelty of Luciola is the ultrasonically levitated electronic object powered by resonant inductive coupling. To enable the levitation of a particle, a custom IC chip is essential in reducing the size and weight of the particle. Ths custom IC chip is designed to achieve an intermittent lighting of the LED, which increases the maximal distance between the transmitter and the receiver coils. Luciola is applied to a self-luminous pixel in a 3-dimensional (3D) mid-air display and the drawing of characters in mid-air is also demonstrated.

Iizuka Laboratory
(http://www.mos.t.u-tokyo.ac.jp)

Waveform Reconstruction Technique for Wideband Signal

Tetsuya Iizuka, Byambadorj Zolboo

The Modulated Wideband Converter (MWC) is one of the promising Sub-Nyquist sampling architectures for sparse wideband signal sensing, cognitive radio applications and so on. Since resources within Automatic Test Equipment (ATE) are limited on sampling rate, the MWC can be useful for testing devices with various frequency band.

In this research, we are investigating a feasibility of MWC to reconstruct a waveform of sparse wideband signals for measurement equipment. We created a simulation platform system of MWC in MATLAB environment and the MWC system perfectly reconstructs the waveform of original wideband signal under several ideal assumptions. But in practical implementation, it could suffer in some drawbacks due to non-ideal components and noisy situation.

In terms of noise performance, we proposed an average noise figure (ANF) theoretical notation to expect the noise figure of MWC. The accuracy of the analytical formula is ensured with MATLAB simulation results.

Design Automation and Optimization Techniques for Analog Integrated Circuits

Tetsuya Iizuka, Zule Xu, Naoki Ojima, Masaru Osada

Thanks to the exponential advancement of process technology, performance of digital logic circuits has been drastically improved, and hence most part of signal processing is now carried out with digital logic. However, some analog circuits remain in signal processing; data converters, phase locked loops, and power management circuits still require analog design flows. Thus, easier and faster implementation of them is needed for low cost and efficient development of signal process flows. In this work we propose the

design methods of them in which a commercial automatic place and route tool is utilized. We designed a successive approximation register analog-to-digital converter (SAR ADC), a phase locked loop (PLL), and a digital low-dropout regulator (LDO). In the SAR ADC, analog components such as resistive digital to analog converters (RDAC), a four-input clocked comparator, and track and hold (T/H) circuits are fully implemented with standard cells. The 6-bit resolution prototype is fabricated in a 65 nm standard CMOS technology, and its performance is measured. In the PLL, injection lock is utilized. The PLL is now in development to achieve the goal of low jitter and phase noise. In the digital LDO, with inverter chains as voltage-controlled delay lines, the difference between output and reference voltages is converted into delay difference, then compared in the time-domain. Since the time-domain difference is straightforwardly captured by a phase detector that consists of a D-FF, the proposed LDO does not need an analog voltage comparator, which requires careful manual design. The prototype of the proposed LDO is fabricated in a 65 nm standard CMOS technology. The measurement results show that this prototype exhibit good trackability of output with the fluctuation of the reference and load.

In this research, a DLL (Delay Locked Loop) was designed to produce a clock signal for a high-performance TDC (Time to Digital Converter). TDCs are used in various applications such as ADPLLs (All Digital Phase Locked Loop) and measurements. The DLL had a 1GHz input signal and consisted of 16 delay elements. In order to achieve high resolution for the TDC, the DLL was required to have less than 2ps offset between the input and output, and less than 2ps variation between the delays in each element. We first analyzed the effect of thermal noise in the CP (Charge Pump), PFD (Phase Frequency Detector), and Buffers through calculation and simulation, and showed that the produced jitter was within the requirements. We then used a cascode-multipath architecture for the CP to avoid current mismatch, and achieved an offset of 600fs in simulation. Finally we implemented a calibration technique using capacitor arrays to account for process variation, and showed through simulation that an offset within 10ps can be reduced to within 1ps.

Time Domain Approach for Analog Integrated Circuit Designs

Tetsuya Iizuka, Zule Xu, Meikan Chin, Jing Wang

While digital circuits directly benefit from advanced process technologies, analog circuits suffer from negative effects such as small voltage headroom. Time-domain circuits, where analog signals are represented by digital signal edge transitions, could be a solution to the problem of analog circuits in a nanometer process.

We have applied time-domain control methods to PLL circuit and its measurement. Especially for the IoT devices, the circuits start only when they are necessary for the entire system. While the whole system is going to be activated from the standby state where the PLL is acquiring lock, the power consumption in this period is just a waste, thus it should be reduced. Pulse-Width PLL (PWPLL) is an analog-digital mixed PLL, which controls the output frequency with Soft Thermometer Code (STC) without using a low pass filter. Most of the PWPLL is a digital PLL, which is compatible with P&R. In this research, to reduce the PWPLL startup time and reduce the power consumption of the system, a feedback system parameter (= target value) at the time of locking is stored and a method for reproducing the parameter at the next start is used There was. The conventional fast-start PWPLL creates a layout by manual design, but it takes time and the specification adjustment is difficult. In this research, in order to save labor on layout design, we created a layout using an automatic placement tool and designed a fast startup PWPLL with performance equivalent to manual design.

Time-to-Digital Converter (TDC) is a representative example of time-domain circuits. TDC basically converts a time interval between two rising edges into a digital code by using delay elements. In our research, we focus on a pulse-shrinking TDC, which is one kind of the sub-gate-delay resolution TDCs. In general, TDC has a trade-off between the time resolution and dynamic range, and the trade-off is particularly remarkable in the pulse-shrinking TDC.

Last year we designed and measured a TDC that improves the dynamic range while keeping the high resolution by using a hierarchical approach. We found that the TDC has a serious nonlinearity caused by process variation. So, we analyzed the impact of it by Monte Carlo simulation and designed a new TDC resistant to process variation.

TDC can be applied for various applications and Clock and Data Recovery (CDR) based on Cycle Lock Gated Oscillator (CLGO) is one example. Since the CDR consumes no dynamic power in its standby state and resumes from the standby state just after a 4-bit preamble, it can improve the total power efficiency of serial communication systems that work intermittently such as mobile and IoT sensor node applications which require not only low power consumption in operation but also in standby state and quick startup form the standby state. We proposed CDR using Delay Tunable Buffer (DTB) and Vernier TDC for tracking frequency range extension and low power consumption, designed and measured. While DTB and digital control work as designed, we found the deviation of timing in Vernier TDC. So we proposed new Vernier TDC whose reference level is tunable. The entire CDR system has been fabricated with 65nm CMOS process and 2.3Gbps operation is verified with measurement results.

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mm-Wave Circuit Design for Communication through Dielectric Waveguide

Tetsuya Iizuka, Nguyen Ngoc Mai-Khanh,
Yoshitaka Otsuki, Daisuke Yamazaki,
Takafumi Hara

High-speed communication with the millimeter-wave band has been actively researched. Wireline communication with a dielectric waveguide such as polymer has been proposed and expanded research. Because it is possible to increase the communication distance at low cost while maintaining the communication speed.

In this research, we designed a voltage controlled oscillator (VCO) oscillating at 140 GHz. Oscillator is essential circuit in all systems involving communication. In this circuit, it is difficult to operate in a superhigh frequency band exceeding 100 GHz, with a small area and low power consumption while maintaining low phase noise. In order to solve these problems, we studied to produce a signal of 140 GHz using a frequency doubler, and proposed a method to solve the above problem by removing the impedance matching circuit between each block. We confirmed by actual measurement that the proposed circuit solves this problem.

In a transceiver, it is necessary to modulate and amplify the signal generated by the oscillator. In this research, we adopted on-off-keying as a modulation and proposed an architecture of on-off-keying with low loss and high on-off ratio. We implemented this modulator with a 65 nm CMOS process and confirmed that it is operating with high on-off ratio and low loss by measurement. Furthermore, we implemented an power amplifier circuit in the same process and confirmed that it was possible to amplify a signal of 140 GHz.

In addition, we aim to reduce loss by substrate removal of on-chip antenna in dielectric waveguide communication. Then, building blocks necessary for actual measurement were fabricated using Rohm 0.18 μm process. Also, we evaluated the de-embedding methods required for actual measurement. The signal transfer characteristics of the dielectric waveguide were evaluated with measurement.

Signal Crosstalk Cancellation Technique for High-Speed Wireline Communications

Tetsuya Iizuka, Daigo Takahashi

With the improvement of the circuit performance due to the miniaturization of the semiconductor process, the speed of transmission has been improving. The data rate necessary for applications also has been improving because UHD TVs and automobiles with a lot of electrical equipment was developed.

It is necessary to speed up transmission from both aspects of technology and demand, crosstalk is one of the factors hindering this. As measures for crosstalk, a method for reducing crosstalk at the receiver was proposed in the previous research. In this research, we proposed a method for reducing crosstalk at the transmitter with a delay adjustment circuit and a high-pass filter based on the method in the previous

research. Using simulation, we showed that the proposed method can reduce crosstalk more effectively. The proposed crosstalk cancellation circuits have been implemented with 40nm CMOS technology.

Mita Laboratory

(http://www.if.t.u-tokyo.ac.jp)

Current Research Projects

Programmable Matter - Study on LSI-MEMS energy-autonomous distributed microsystems for realization of deformable matter

Y. Mita, N.Usami, G. Ulliac,
E. Lebrasseur (LIMMS, CNRS-UTokyo IIS),
J.Bourgeois, B.Piranda (FEMTO-ST, France),
S. Delalande (PSA-Peugeot)

As one example of integrated MEMS that is expected to open new research and industrial ap-plication fields, the authors are trying to show a top-down application of energy-autonomous dis-tributed microrobots. A number of identical tiny robots, sized below 1cm, will be released in an en-vironment. Individual robot can communicate with their neighbor, can stick each other, can share energy, to realize cooperative function. The PI has received a French National Research Center (ANR) grant on behalf of host professor of CNRS laboratory in the Institute of Industrial Science (LIMMS, CNRS-IIS, UMI 2820), together with FEMTO-ST Laboratory and PSA-Peugeot Laboratory for such "micro robots that can realize deformable substance by cooperative action, named Programmable Matter". In this year, an electrostatic actuation on tiny (1mm to 10mm) objects is performed and analyses were conducted.

Integration of electrode devices on MEMS fluidic devices

Y. Mita,A. Higo, Y.Takeshiro, Y.Okamoto,
N.Washizu (Advantest), A.Takada (Advantest),
M. Fujiwara, T.Sawamura

Towards the goal of production of brand-new sensor devices with higher sensitivity and func-tionality, the team is working on small-gap electrode fabrication process. The target of first year is reliable electrode integration on nanopore, as well as microactuator integrated nanopore system.

Fine Large-Area Electron Beam Lithography Exposure Methods

Y. Mita,A. Higo, M. Fujiwara, T.Sawamura,
M.Takizawa (Advantest), Y.Kudo (Advantest)

The team explores newly-acquired (in 2013) rapid electron beam writer F7000S-VD02. The ca-pability of high electron dose and sharp edge due to cell (character) projection machine configura-tion is being examined. The breakthrough in question is to extend the large-area EB lithography, whose pattern approximation have been limited to rectangular shapes, into expressing free-form smooth shapes and a number of periodical small patterns. This year's outcome include a micro race-track optical resonator test structure to quantify the quality of pattern approximation by optical absorbance spectrum.

University-Industry collaborative research on highly-functional system by MEMS post-process of CMOS-VLSI

Y. Mita, S. Inagaki, T. Kuriyama, Y.Sato (Nanox Japan),
T.Ono (Sony)

The research targets are new sensor devices, made by post-process at clearnrooms such as VDEC Takeda Supercleanroom and others, of VLSI wafer made through VDEC. The important finding has been that VLSI wafer acquired just after transistor fabrication could sustain processes even with heat treatment, such as deposition, ion implantation, and drive-in. In 2016, a VLSI de-vice made on Silicon-on-Insulator (SOI) wafer was successfully Deep-RIE processed. The in-dustrial interest is its versatility – many different types of application devices, which differ one from another according to request of market, can be fabricated by using the same technology. More and more companies are interested in the scheme and are working on the technology on the col-laborative research projects.

High-sensitive ultrasonic probe by integrated MEMS technology

Y. Mita, R.Yamaguchi, N.Usami, A.Higo,
T.Yoshimura (Osaka Prefectural University),
T.Mizuno (Konika Minolta),
K.Suzuki (Konika Minolta),
Y.Nakayama (Konika Minolta),
T.Endo (Nagoya Medical Center)

Using the same scheme as above mentioned CMOS-MEMS post process R&D scheme, this project aims at integrating piezoelectric material and MEMS post-processing to obtain a brand-new ultrasonic inspection probe, whose sensitivity is as 100 times as cutting-edge technology. From 2018, the team is accepting a public funding from Japan Agency of MEdical Research and Devel-opment (AMED) to accelerate research towards clinical application.

LSI hot-spots active cooling system

Y. Mita, Y. Okamoto, K. Fujimoto (Titech),
H.Ryoson (Titech), and T. Oba (Titech)

A hotspot, which is referred to a high-temperature area due to the overheating of a circuit block that excess passive cooling capability, is becoming a key limiting factor of LSI performance. An ac-tive cooling system that tries to actively remove such local heating by circulating liquid coolant is our research target. This year an electroosmotic pumping actuator and high-voltage generation CMOS MEMS device was independently proven to be working. Also, a zeta potential measure-ment system, which is mandatory for evaluating surfaces for electroosomotic flow, is developed. This system only have to stick-on the surface to be evaluated.

Test Pad post-processing for LSI diagnosys

Y. Mita,Y. Okamoto, A. Higo, A. Mizushima,
J.Kinoshita (Nexty Electronics)

An academic-industry collaborative project to enhance the capability of LSI post fabrication di-agnoses. In VDEC also, a Focused Io Beam (FIB) machine is installed to analyze and repair the LSI. The practical limit of such system is availability of wiring material, which is machine dependent. In case of VDEC's machine (FEI V400ACE), the material is limited to tungsten so it is impossible to wire bond on the post-fabricated pads. On the contrary, there exists needs for wire-bonding on the post-process FIB opened pads, in order to integrate it into the printed circuit testing board. To-wards that end, we developed a MEMS shadow masking methods to deposit wiring material through them. An assessment of transistor characteristics under such probe was performed and proved no mechanical impact.

"Zeolite-Electronics-Nanostructure (ZEN)" integrated chemical sensor

Y.Mita, K. Yamada, Y.Okamoto,
M.Denoual (ENSI de Caen, France),
Tixier Mita Agnès (UTokyo RCAST),
Eric Lebrasseur,
Hussein Awala (ENSI de Caen, France),
Julien Grand (ENSI de Caen, France),
Svetlana Mintova (ENSI de Caen, France)

One of the most important application field of MEMS is sensors that can detect physical and chemical amount that cannot be sensed by human beings. Following a long history of the group's research, the team was appointed in 2015 as a JSPS-CNRS bilateral cooperative research project grant. The goal of the research is to develop a chemical sensor by integrating Zeolite material that is new to VLSI, and applying post-process on it. Within one year, the team have successfully demonstrated two types of devices: a zeolite chemical sensor by resonant frequency shift detec-tion, and by thermal capacity change detection according chemical concentration. An improvement on the stress detection device by using LSI components is made.

Project PARIS: PARallel Integrated microSystem for High Frequency Action-Based Non-Invasive Multi-Modal Cell Analyses

Y.Mita, T.Tsuchiya, Y.Okamoto, A.Mizushima, E.Lebrasseur, C.Moslonka (ENS Paris-Saclay, VDEC internship student), B. le Pioufle C.Moslonka (ENS Paris-Saclay), Tixier Mita Agnès (UTokyo RCAST), Olivier Français (ESIEE, Univ. Paris Est), F.Marty (ESIEE, Univ. Paris Est)

Having granted again JSPS-CNRS bilateral project 2018, the team is developing a large-scale multi-modal cell analyses system (project name: PARIS). The electrorotation method, which is known to measure a mechanical rotational response to the incident rotational electrical field fre-quency is used. The method is non-invasive so the evaluated cells are possible to be used in fur-ther biological experiments. In this year fabrication of classical electrodes was first leaned by VDEC internship student. Then thicker electrodes were made in collaboration with ESIEE and ex-periments were done at ENS Paris-Saclay in Cachan. The measurement revealed the problem of Z-axis controllability so new device structure was proposed and proven to be efficient.

Colloidal integrated Infrared Detector

A.Higo, N. Usami, Y. Okamoto,

W. Haibin, N. Kubo, K. Segawa, Y. Mita

Electron devices using colloidal quantum dots are believed to open new application fields such as light emitting devices and or photovoltaics. Up to date, very few research activities have been done in sensors applications; if we can realize integrated photodiodes that have extended sensitive wavelength as long as 1.35μm-1.4μm wavelength, such devices can be used by many new appli-cations such as security cameras and / or Laser Radar (Lidar) under sunlight. The aim of this research is to find an integration method for beyond Si-LSI device. We try to integrate colloidal quantum dots of which absorption spectra can be designed through molecular design. By inte-gration, Silicon device will be able not only to capture infrared wavelength lights, which is impossi-ble by its original characteristics, but also my include information reading and computation circuits. For the first year's exploratory study, partly financed by the LIMMS internal project grant, spin coating integration method has been investigated. The enhancement of absorbance spectra at such wavelength has been experimentally confirmed.

Development of zero power multiple-threshold maximum acceleration sensor for cyber physical system

Y. Mita, R Ranga Reddy

VDEC is awarded a Japanese JST – Indian DST joint grant (SICORP) for cyber physical systems research, in cooperation with IIT Bombay campus. The team is participating the project through a Shock Resonant Spectrum (SRS) sensor, which has been a research theme of 2012-2014. A new Ph.D student from India is assigned and fabrication process was recovered. This year we have developed complete system to record 10-levels of maximum acceleration in MEMS device.

Development of LSI post-processing for hybrid integration

Y. Mita, N.Usami, E. Ohta, A.Higo,

T. Momose (Material Eng.)

To provide new capability to Nanotechnology Platform Users, a couple of process technologies for LSI hybrid integration is under development. In FY2016, a stable gold electroplating system was purchased and a bump plating for LSI flip-chip bonding was developed. In parallel, a supercritical fluid deposition (SCFD) machine was restored to investigate trench embedding deposition with metal. This year, we have obtained a reliable protocol of surface treatment, with which the SCFD Cu stick sufficiently strong to be used as seed material for following processes (such as electroplating).

Takagi-Takenaka Laboratory

(http://www.mosfet.k.u-tokyo.ac.jp/)

III-V/Ge Metal-Oxide-Semiconductor (MOS) FETs and the 3 dimensional integration

S. Takagi, M. Takenaka, Kasidit Toprasertpong, Ke Mengan, Kwangwon Jo, Cheol-Min Lim, Tsung-En Lee, Sanghee Yoon, Chiaki Yokoyama, Zilong Wang, Kei Sumita, Jun Takeyasu

We have conducted the research on high-performance III-V/Ge MOSFETs and the 3 dimensional stacked CMOS structures by using these high mobility MOSFETs. We have investigated Smart-cut technology for forming an high-mobility ultrathin InAs channel. By optimizing the condition of hydrogen ion implantation, we have successfully achieved InAs Smart-cut, and obtained ultrathin InAs-on-insulator wafer. We have also conducted the research of Ge condensation for Ge-on-insulator MOSFETs. We found that the slow cooling procedure after the condensation resulted in high compressive strained in the condensed Ge-OI layer.

Tunnel FET

S. Takagi, M. Takenaka, Kasidit Toprasertpong, Kimihiko Kato, Taeeon Bae, Daehwan Ahn, Ryotaro Takaguchi

We have investigated tunnel FETs (TFETs) which can exhibit steep subthreshold slope for low-power operation. Lateral InGaAs TFETs, Ge TFET, GaAsSb/InGaAs hetero-junction, Ge/strained Si hetero-junction and ZnO/(Si, Ge) TFETs have been explored. We have successfully demonstrated the subthreshold slope of 49 mV/dec. by EOT scaling of InGaAs TFET with ZrO2 high gate dielectric.

Ferroelectric gate insulator MOSFETs

S. Takagi, M. Takenaka, Kasidit Toprasertpong, Kimihiko Kato, Zaoyang Lin, Kento Tahara

We have conducted the research for MOSFETs using ferroelectric gate insulators. We have confirmed ferroelectricity of ALD HfZrO2 films on Si and the operation of MOSFETs with these gate insulators.

On-chip/Off-chip optical interconnect

M. Takenaka, S. Takagi, Kasidit Toprasertpong, Qiang Li, Naoki Sekine, Pengyuan Cheng, Dongheng Lyu, Qianfeng Chen, Dongrui Wu, Yuto Miyatake

We have investigated Si photonics for on-chip and off-chip optical interconnection for CMOS LSI. We have revealed that an efficient optical phase was available in reverse-biased III-V/Si hybrid MOS capacitor through carrier depletion and Franz-Keldysh effect. We have also found that an efficient grating coupler can be automatically designed using one of the artificial intelligence, that is, evolution strategy. We have also investigated the III-V CMOS photonics platform by using III-V on insulator wafer. We have numerically analyzed the modulation properties of InP-slot optical modulator with EO polymer.

Si photonic integrated circuit for AI

M. Takenaka, S. Takagi, Kasidit Toprasertpong, Qiang Li, Shuhei Ohno

We have investigated programmable photonic integrated circuits (PICs) including a universal PIC for deep learning. We have proposed programmable PICs integrated with III-V/Si hybrid MOS optical phase shifters and revealed its learning capability. We have also proposed ring resonator crossbar array Si PIC for deep learning.

Ge mid-infrared photonic integrated circuit

M. Takenaka, S. Takagi, Kasidit Toprasertpong, Chong Pei Ho, Ziqiang Zhao, Takumi Fujigaki

We have also conducted the research of the mid-infrared photonic integrated circuits based on Ge-on-Insulator (GeOI) wafer fabricated by wafer bonding. We have achieved high-quality GeOI wafer, enabling high-Q micro ring cavity on GeOI. We have also demonstrated efficient Ge thermo-optic phase shifters on GeOI wafer.

2D material devices

M. Takenaka, S. Takagi, Kasidit Toprasertpong,
Roda Nur, Hanzhi Tang, Xiaoxuan Zhang

We have investigated 2D materials such as graphene and MoS2 for semiconductor devices. We have proposed a black-body thermal emitter using graphene coupled into a Si waveguide. We have numerically analyzed graphene thermal emitter.

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