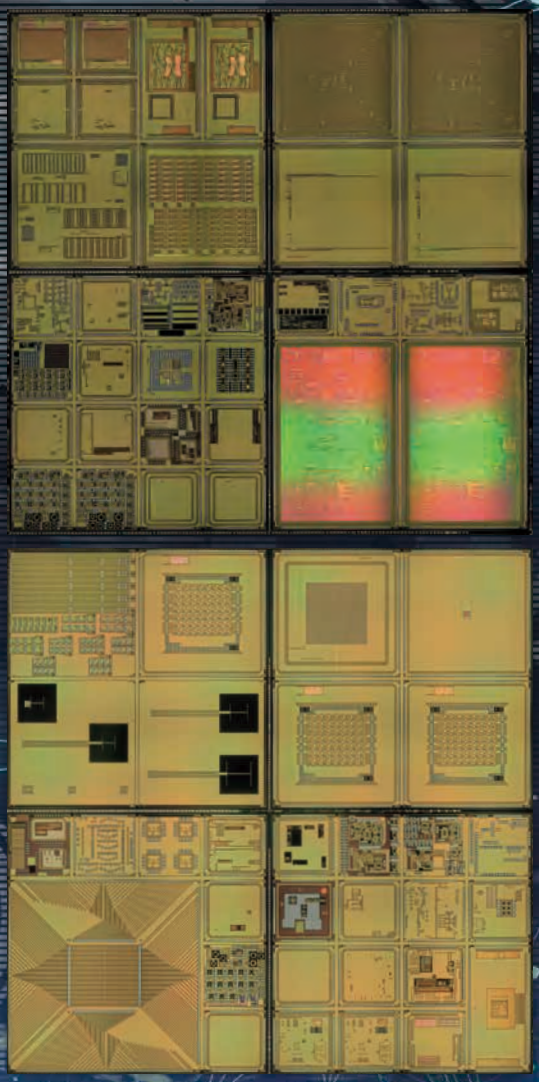
VDEC

東京大学工学系研究科附属
システムデザイン研究センター
基盤設計研究部門・基盤デバイス研究部門
（大規模集積システム設計教育研究センター）

年　報

令和２年度

2020
Systems Design Lab, School of Engineering, (VLSI Design and Education Center), The University of Tokyo
Annual Report



Systems Design Lab, School of Engineering
(VLSI Design and Education Center), The University of Tokyo 2020

Message from Director of VDEC

VLSI Design and Education Center (VDEC), The University of Tokyo
Director

Masahiro Fujita

VLSI Design and Education Center (VDEC) was established in 1996 in the University of Tokyo as an organization that provides nation-wide services. Its mission is to provide all Japanese academia with practical educational and research environments through semiconductor development, manufacturing and prototyping of new devices. Unique opportunities to learn about real semiconductor development, design and manufacturing that cannot be obtained from desk-based learning and exercises have been provided. Through such opportunities, one can acquire knowledge in all aspects related to semiconductor systems. As a result, it is expected that the various technical capabilities of Japan in the semiconductor from design to manufacturing can be significantly improved.

In fact, there are organizations all over the world that are considered to have the same mission as VDEC. There are organizations and mechanisms in the United States, Canada, Europe (two), South Korea, Taiwan, and most recently in mainland China. These organizations hold meetings for information exchange and cooperation basically twice a year. Each organization has various strengths based on the situation in the region, and cooperative activities to make the most of these strengths are carried out. As a result, we are now able to carry out international joint chip prototyping smoothly, and we will be able to work more closely together in the future to launch international joint projects.

On the other hand, VDEC differs from the other similar organizations around the world in that it not only supports designs and prototyping of semiconductor chips, but also a research and development environment in a clean room for new semiconductors and device by providing a variety of advanced equipment that is funded by governmental projects. Users can research and develop new semiconductor-related technologies on their own in a clean room. Normally, the design and prototyping of a semiconductor chip is based on the devices that have already been developed. Although this refers to prototyping, VDEC is not only limited to prototyping, but also to implementing chips in combination with new devices. This has made it possible to realize new semiconductor systems that give previously unimaginable performance and shape, and has made it possible for us to develop products that lead the world. However, the research and development of semiconductor technology using the two environments provided by VDEC is never performed, and hence it is not at all easy. The truth is that the users of those two environments do not know much about each other. We have realized that it would be difficult for VDEC alone to achieve it. Therefore, in coordination with developments within School of Engineering, VDEC was re-born on October 1, 2019 as System Design Research Center within School of Engineering.

In the future, it will become normal to collaborate with the engineering departments and the information science and technology departments for the integrated use of the two environments. Through this we would like to become the center of semiconductor technology in Japan and also in the world. We look forward to your support so that we can work better.

Message from Director of d.lab

System Design Lab (d.lab) Center, School of Engineering, The University of Tokyo
Director

Tadahiro Kuroda

Even what appears to be a discontinuous event has a story with well-connected pieces leading up to it. The Systems Design Lab (d.lab) was established in October of last year. You must be wondering what happened to VDEC with this sudden reorganization. Let me provide you with the background.

From 1996, for a quarter century the VLSI Design and Education Center (VDCE) offered unparalleled, outstanding education and produced excellent minds for the semiconductor industry. Every year, its design environment and chip prototyping service were employed at more than 300 research labs across the country, while its clean room and related facilities were utilized by more than 200 research labs.

However, our outstanding graduates who have entered the semiconductor industry are not always able to fully realize their potential. In this quarter century, while the worldwide semiconductor industry maintained a high annual growth rate of 7%, Japan's semiconductor industry was on the decline. Why is it that even with the world's top minds we have not been able to compete neck and neck with the rest of the world?

While there are various theories, mine is that Japan lost the competition of capital investment.

As you know, semiconductor is a low margin business which relies on volume from mass-produced, general-purpose chips for profit. The demand for large volume of general-purpose chips is fueled by the adoption of the von Neumann computer architecture. A majority of the industry' s revenue is generated from the sale of large volume of low-price processors and memory. With the adoption of big data gaining momentum, sensors should also be added to the fold.

In such a business you compete on capital investment. When a device like DRAM, flash, CPU or GPU is invented, and its large business potential is recognized, fierce competition follows immediately, resulting in industry realignment and eventually consolidation.

Japan won in device innovation but lost in capital investment competition.

However, we are now on the cusp of a new era with a game changer on the horizon. Convinced that it is impossible to win by employing only general-purpose chips from dedicated chipmakers the like of Intel and Qualcomm, IT giants such as GAFA have embarked on in-house development of specialized chips.

There are 3 reasons for that. The first is the unique energy crisis faced by data companies. As a result of the crisis, only those who can improve energy efficiency 10-fold can achieve 10-fold increase in computing performance, or 10-fold increase in smartphone battery life. Compared to general-purpose chips which can be used to perform every possible function, specialized chips can achieve a more than 10-fold increase in energy efficiency by eliminating unnecessary circuits.

The second reason is the rise of AI. AI in the form of neural networks and deep learning offers a new way of information processing to owners of data. Similar to our brain, neural networks are based on wired logic where functionality is defined by how the components are wired together. Furthermore, data is processed in a parallel fashion which enables a more than 10-fold improvement in power efficiency compared to the sequential data processing of von Neumann architecture.

The third reason is the adoption of the fabless model by the industry. Under this model, pure-play foundries such as TSMC offer manufacturing services to the world, which enables any user adopting a business model of providing proprietary chips with maximum AI performance to develop their own chips. For companies offering a hardware platform solution that drives the demand for sufficiently large chip volumes, in-house development allows them to acquire more quickly higher performance chips at lower cost than procuring from dedicated chipmakers.

As a result, a game changer in the form of a shift from general-purpose to specialized chips is happening.

The rise of general-purpose chips is initiated by device innovation, while its fall results from capital investment competition. Meanwhile, the rise of specialized chips is initiated by design and development innovation, while its fall is driven by Moore's Law.

ASIC (Application Specific Integrated Circuit) had a sizable market between 1985 and 2000. In the 1980' s, research and development efforts led by the University of California at Berkeley resulted in the creation of automatic layout and logic synthesis technology as well as the birth of chip design tools vendors. Furthermore, a semi-custom manufacturing process like the one used in tailoring clothes was developed where a semi-finished chip was made first like a standard product, which was then tailored towards different applications by customizing the interconnect layers.

Using these design and development innovations, chip development productivity improved dramatically by three orders-of-magnitude in total. Nevertheless, with Moore' s Law increasing integration density by three orders-of-magnitude in 15 years, even with computer-aided design chip development took more man-hours than ever. This contributed to profit erosion of the ASIC business which eventually resulted in its demise.

However, Moore' s Law is now slowing. In the next quarter century, we expect winners in the new arena to be those who lead in design and development innovation.

The development of specialized chips requires academic knowledge instead of capital investment. Development of automatic layout and logic synthesis was previously driven by the University of California at Berkeley. Similarly, university research will play an integral role in creating the foundational knowledge required for automatic generation of functionalities, systems, and so on.

The 20th Century was dominated by "general-purpose." After the war, in a quest for material gratification and economic efficiency, economic growth was driven by mass production of standardized products.

However, as modern society matures, what we value has shifted from collective growth to personal fulfillment. This has resulted in the transition from an industrial to a knowledge-based society.

While this transition was spreading from developed to developing countries, Japan was able to enjoy a period of prosperity by continuing to mass-produce standardized products. But eventually when the transition was complete, Japan fell behind other Asian nations due to its slow adaptation to the transition. This is what I believe to be the societal background for the decline of Japan' s semiconductor industry.

The 21st century looks to be the century of "specialization". The center of our value is shifting from being capital-intensive to being knowledge-intensive, from scale to knowledge, from increase in quantity to improvement in quality, from material to spirit, from convenience to joy, from products to services, from large volume to large variety, from standardization to individualization, from what everyone can do to what no one else can do.

How should the manufacturing industry adapt to such a shift? It is d.lab's mission to search for an answer.

In addition to education, we strive to utilize the power of our scholarship to contribute to the advance of industry and society. With the newly established Advanced Design Research Division and Advanced Device Research Division focusing on collaboration with industry, in addition to the Platform Design Research Division (formerly VDEC) and Platform Device Research Division (formerly Takeda Cleanroom) focusing on education, we at d.lab are embarking on this new journey.

VDEC

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C O N T E N T S

Chapter1 Introduction of d.lab

The Systems Design Lab (d.lab) was established in October of last year. In addition to education, we strive to utilize the power of our scholarship to contribute to the advance of industry and society. We are embarking on this journey with the newly established Advanced Design Research Division and Advanced Device Research Division focusing on collaboration with industry, in addition to the Platform Design Research Division (formerly VDEC) and Platform Device Research Division (formerly Takeda Cleanroom) focusing on education.

From 1996, for a quarter century VDEC offered unparalleled, outstanding education and produced excellent minds for the semiconductor industry. Every year, its design environment and chip prototyping service were employed at more than 300 research labs across the country, while its clean room and related facilities were utilized by more than 200 research labs. In this annual report, we will summarize its activities and accomplishments in the 2019 fiscal year.

This annual report is structured as follows. Chapter 2 introduces the operation of VDEC and reports on its activities in 2019. Chapter 3 summarizes the activities of the Advantest D2T Research Division. Chapter 4 provides an overview of the research conducted at the individual labs within VDEC.

Chapter2 Activity Report of VDEC

2.1 Introduction of VDEC activities and activity report of FY2019

VLSI Design and Education Center(VDEC), University of Tokyo was established in May 1996. VDEC has been operating for the following 3 major roles: “spreading the latest information on VLSI design and education,” “providing licenses of CAD tools,” and “supporting on VLSI chip fabrications for academic use.” VDEC has been reorganized, to empower VLSI design activities in the University of Tokyo, as Systems Design Lab(d.lab), Graduate School of Engineering, the University of Tokyo, and VDEC activities has been continued as the VDEC functionality in the Fundamental design division of d.lab. The VDEC activity report of FY 2019 is described hereafter according to Fig. 2.1.

The missions of VDEC are for advancement of researches and education on LSI design in public and private universities and colleges in Japan and send many distinguished VLSI designers into industry. After 24 years of VDEC establishment, educations on CAD software, LSI design and design flow in universities have been well established. On the other hand, advancement on nano-meter CMOS technologies forces design flow and CAD software complicated. We have been continuing CAD tool seminar by the lecturers from EDA vendors for twice a year. We hold the seminar in VDEC and provide distance learning through video streaming. We expect spread of the up-to-date LSI design methodology by using CAD tools.

We assume our LSI design flow seminars as educations on basic LSI design concepts and practical experience of LSI design with CAD tool chain. VDEC holds “LSI design education seminar”, a.k.a. VDEC Refresh Seminar, once a year. This year we hold 3 courses, “Analog design course” and “RF design course”, and initiated “MEMS design course” in July-September time frame. We invite experienced professors among universities as lecturers for the courses to conduct LSI design education courses with practical experience. We also hold “Transistor level design

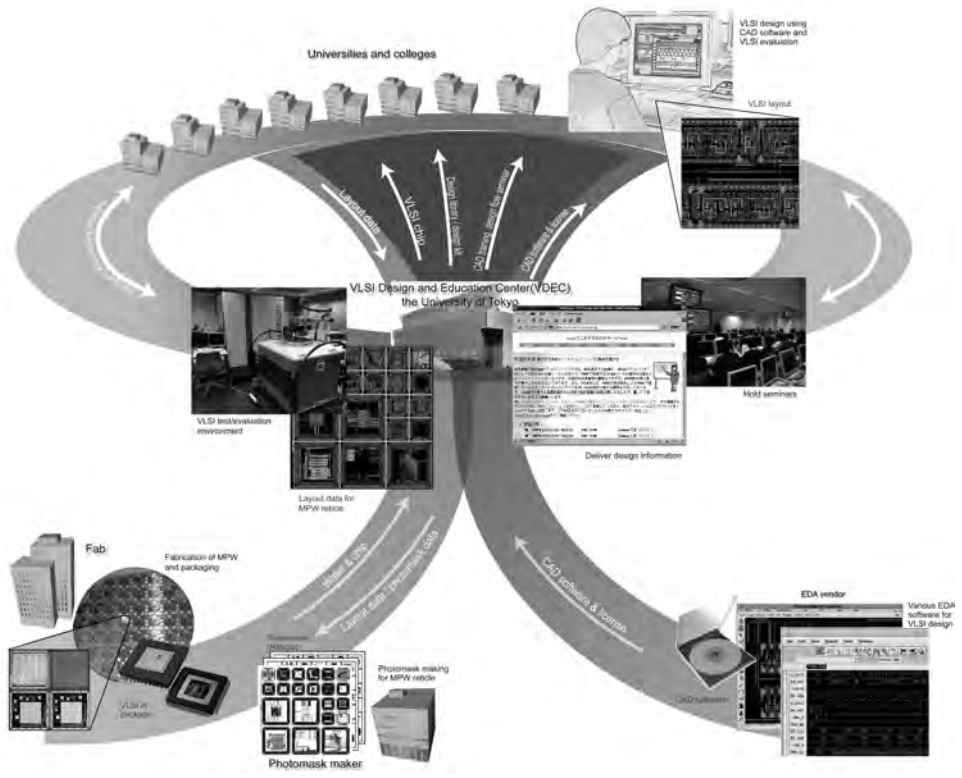


Fig. 2.1 VDEC activities

flow in VDEC" and "Digital design flow in VDEC EDA environment" for designers in universities. We started to charge these two LSI design education courses, as well as VDEC Refresh Seminars.

In addition to the above seminars, we hold "VDEC Designer' Forum" among young professors and students annually. This is a workshop that the participants exchange their design examples with not only success stories but also their failure stories, in addition to invited talks. We expect students and professors who will start designs to learn kinds of know-hows. We have initiated "IEEE SSCS Japan Chapter VDEC Design Award" this year, and final examination and awarding have carried out during the "VDEC Designer' Forum". Mr. Y. Fujiwara(Tohoku Univ.) is awarded as "IEEE SSCS Japan Chapter VDEC Design Award" winner, and Mr. Y. Fujiwara(Tohoku Univ.), Mr. H. Zhang(Tokyo Institute of Technology), and K. Sugie(Nara Institute of Science and Technology) are awarded as "the best VDEC Design Award", and Ms. J. Pang(Tokyo Institute of Technology), Mr. H. Kawauchi(Shizuoka Univ.), and Mr. K. Matsuyama(Shizuoka Univ.) are awarded as the "VDEC Design Award."

LSI designers come up against various difficulties during actual LSI design scene, even after the basic educations through various seminars and the forum. One of the biggest problems for beginners is the setup of CAD softwares. Many of them also get confused by "Esoteric messages" come out from CAD softwares, even after they successfully setup CAD tools. In such situations, VDEC mailing-lists make significant contributions. VDEC users can register to VDEC mailing-lists on CAD tools, and process dependent groups through VDEC web pages, and can ask questions and helps on their facing issues. It is not a responsibility for the registrant of such mailing-lists to give answers to questions, however, in most cases, replies are given by the experienced users of CAD tools and experienced designers within a couple of hours to a couple of days. Moreover, emails are accumulated and are open to the VDEC users, as shown in Fig. 2.2, who have registered VDEC accounts, as the important educational assets. We expect all the VDEC users to make the full use of this mechanism to help solve problems.

We continue chip fabrication services on SOTB CMOS 65nm by Renesas Electronics, 0.18μm CMOS by Rohm and 0.8μm CMOS by On-semi Sanyo Semiconductor.

Our donated division "Design To Test(D2T)", which was founded by donation from Advantest in Oct. 2008, focuses on enrichment of education on LSI testing and bridging between design and testing.

Fig. 2.3 shows trends of number of papers through VDEC activities. Number of papers is increasing, which means researches in the field of VLSI design have been encouraged after VDEC establishment.

Fig. 2.4 shows number of papers related to CAD usage,

Fig. 2.2 Archives of emails of VDEC mailing-list.

chip fabrications and VDEC facility usages. CAD tools are widely used to write papers. CAD tools are used not only chip designs themselves but also used for preparation of chip fabrication and they contribute to verify fundamental ideas of researches.

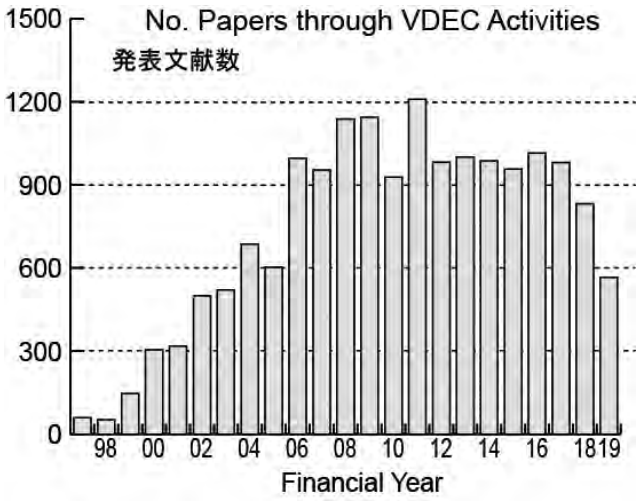


Fig. 2.3 Trends of number of papers through VDEC activities.

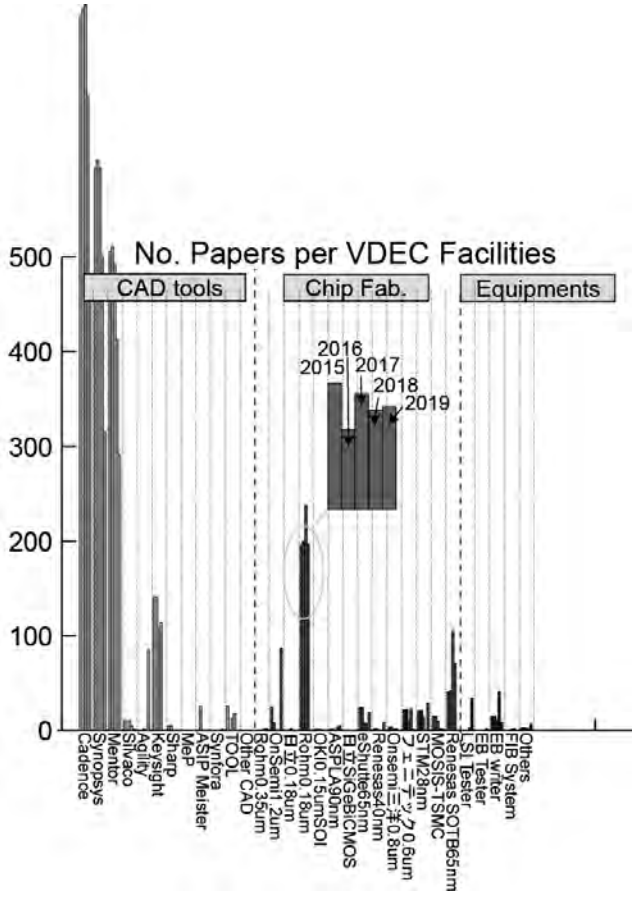


Fig. 2.4 Number of papers related to VDEC facilities.

2.2 VDEC CAD Tools

Since 1996, VDEC has provided CAD software licenses to the registered researchers in universities and colleges in Japan. The CAD tools we provided in 2020 through the activities of VDEC in Systems Design Lab (d.lab) are shown in Table 2.2.1. The researchers can use those CAD tools when their local machines, whose IP addresses are registered in advance, are authorized by one of VDEC license server located in the ten VDEC subcenters shown in Figure 2.2.1. For each CAD tool, VDEC provides 10-100 floating licenses. Those CAD tools can be utilized only for research and education activities in national universities, other public universities, private universities, and colleges.

When one is going to use VDEC CAD tools and chip fabrication service (the details are described in Section 1-3), some faculty member of his/her research group in a university or a collage needs to do user registration. Figure 2.2.2 shows (a) the number of registrants, (b) the number of distinguished universities/colleges of the registrants, and (c) the number of registrants who applied VDEC CAD tools, (d) the number of applied licenses of all CAD tools.

Table 2.2.1 VDEC CAD tools

Name	Function	Vendor
Cadence tool set	Verilog-HDL/VHDL entry, Simlation, Logic synthesis, Test pattern generation, Cell-based (including macros) place, route, and back-annotation, Interactive schematic and layout editor, Analog circuit simulation, Logic verification, Circuit extraction	Cadence Design Systems, Inc.
Synopsys tool set	Verilog-HDL/VHDK simulation, Logic synthesis, Test pattern generation, Cell-based (including macros) place, route, and back-annotation, Circuit simulation, Device simulation	Synopsys, Inc.
Mentor tool set	Layout verification, Design rule check	Mentor Graphics Co. Ltd.
Silvaco tool set	Fast circuit simulation	Silvaco
ADS/Golden Gate	Design and verification of high-frequency circuits	Keysight Technologies
Bach system	BachC-based design, synthesis, and verification	Sharp
LAVIS	Layout visualization platform	TOOL

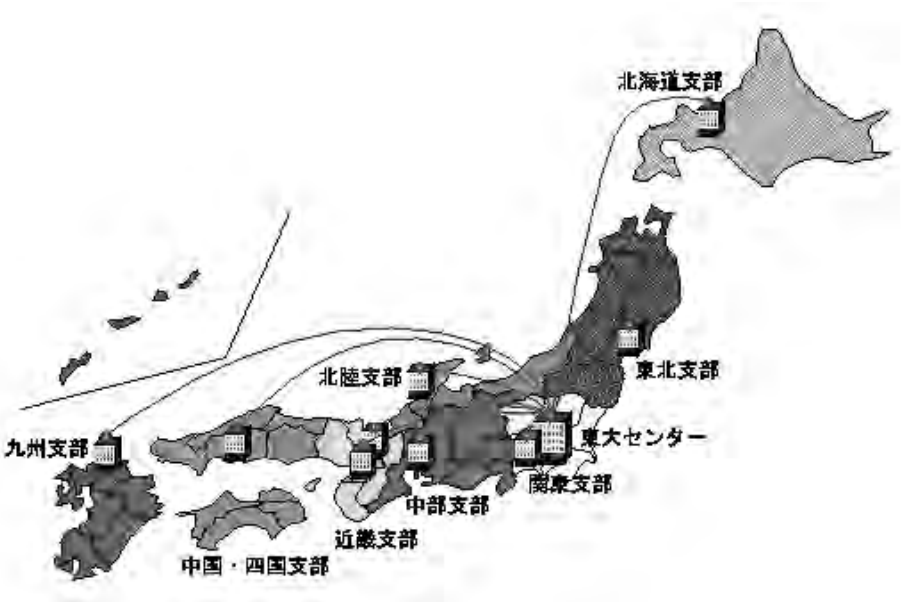
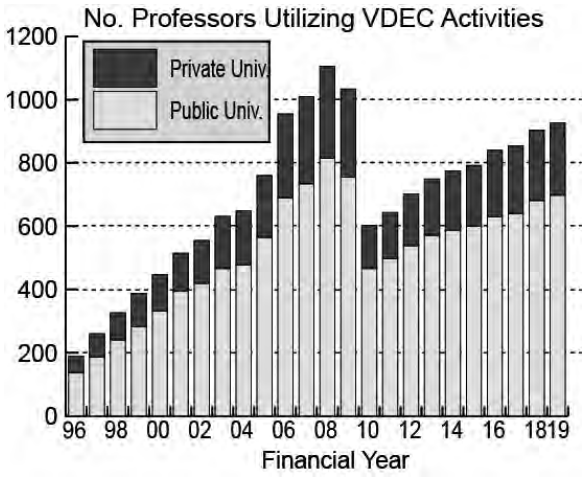
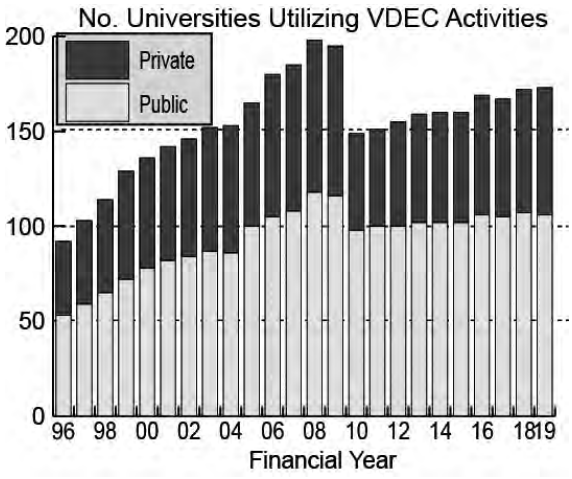


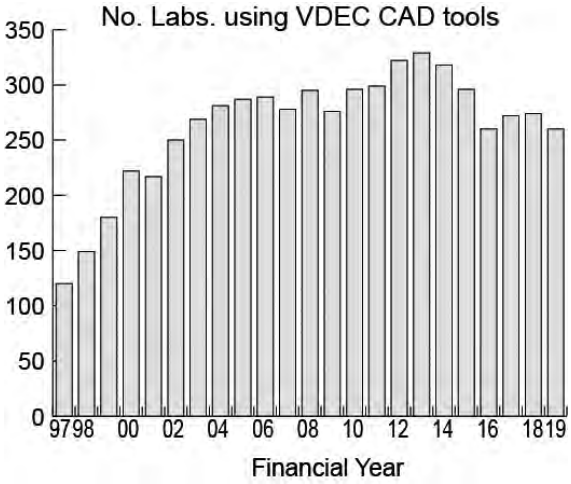
Fig. 2.2.1 VDEC Subcenters



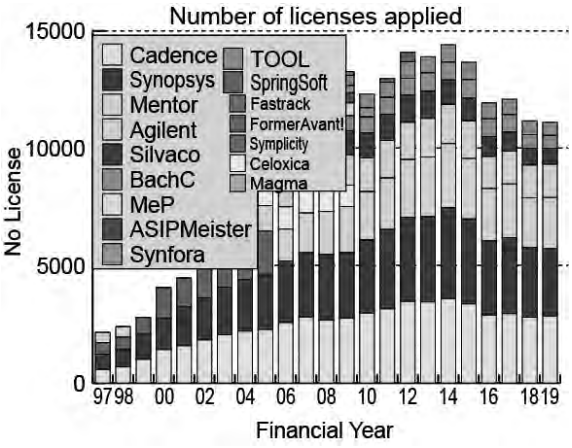
(a) The number of registrants



(b) The number of universities colleges of the registrants



(c) The number of research group applied CAD tools



(d) The number of applied licenses of all CAD tools

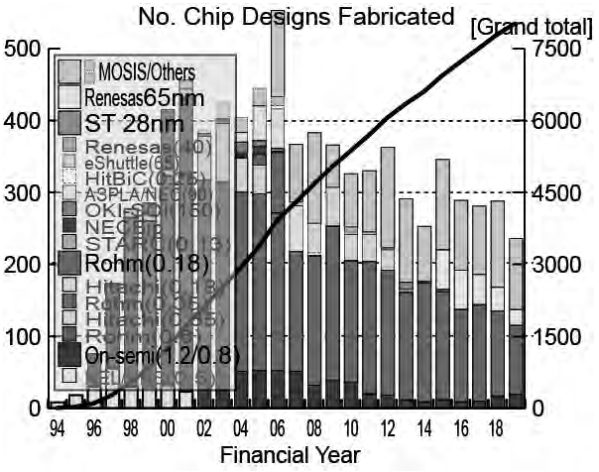
Fig. 2.2.2 The numbers of VDEC CAD Applications

2.3 VLSI Chip Fabrication

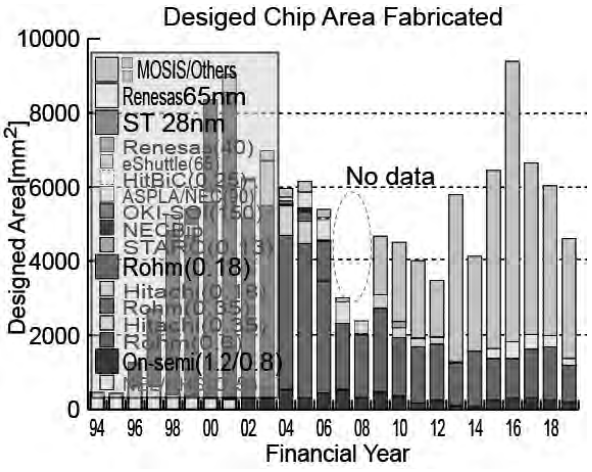
2.3.1 Trends of VLSI Chip Fabrication Services

Fig. 2.3.1 shows a trend of number of designed chips for VDEC chip fabrication services, including pilot project prior to VDEC establishment.

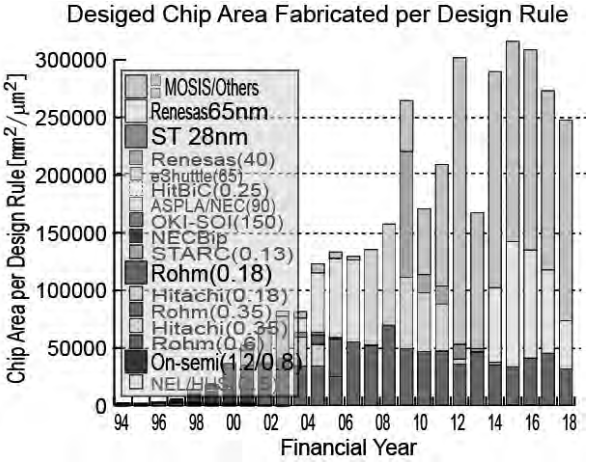
VLSI chip fabrication is limited to 0.5μm CMOS provided by NTT Electronics during the pilot project in 1994 and 1995. VDEC chip fabrication had started in 1996 with 1.2μm CMOS provided by Motorola Japan, which is now On-Semiconductor as well as the 0.5μm CMOS. In 1997, VDEC received cooperation from Rohm and has started 0.6μm CMOS process. In 1998, VDEC started chip fabrication services of 0.35μm CMOS by Hitachi, and in 1999, VDEC started 0.35μm CMOS by Rohm. We had a test chip fabrication of 0.13μm CMOS by STARC through "IP development project" in 2001. We added 0.18μm CMOS by Hitachi into our chip fabrication menu in 2001. From 2002, we started VDEC-MOSIS chip fabrication program initiated by Prof. Iwata of Hiroshima University. Under this program, VDEC member can access to TSMC and IBM processes with lower price. We also started Bipolar chip fabrication by NEC Compound Semiconductor Devices. In 2004, we started 0.15μm SOI-CMOS chip fabrication by Oki Electric as test chip fabrications. In the same year we started 90nm CMOS chip fabrication by ASPLA/STARC. In 2006, we started 0.18μm CMOS by Rohm and 0.25μm SiGeBiCMOS by Hitachi. In 2008, we started 65nm CMOS process by eShuttle, after closure of 90nm CMOS chip fabrication in 2007. In 2010, we started 40nm CMOS process by Renesas Electronics through "Next Generation Semiconductor Circuits & Architecture" project between METI and STAR. On the other hand, 1.2μm CMOS chip fabrication program came to end by the September 2011. 40nm CMOS by Renesas Electronics and 65nm by eShuttle also come to end by Oct. 2012 and Aug. 2013, respectively. We started CMOS0.8μm in Oct. 2012 by On-semiconductor-Sanyo as a test chip fabrication and opened it as the regular chip fabrication menu in 2012. We started FD-SOI 28nm CMOS by ST-Microelectronics through CMP, France, as the advanced CMOS process in 2013. We started SOTB 65nm CMOS by Renesas Electronics in 2015. We initiated two more chip fabrication trials in 2017, on CMOS 0.6um HV from Ricoh, and CMOS 40nm



(a) Trend of number of designs fabricated.



(b) Trend of designed area.



(c) Trend of designed area normalized by design rule.

Fig. 2.3.1 Trend of number of designs and designed chip area.

from Mie Fujitsu.

Fig. 2.3.1(a) shows trends of number of chip designed for VDEC chip fabrication. For the first 6 years until 2001, the number of designed chips shows steady increase, which means drastic improve of the effectiveness researches and education of LSI design, and we assume drastic increase of number of students related to LSI chip design and education. During few years of stable number around 400 chip designs per year, we can see transition of designs toward finer process. In 2007, we saw a large drop, which was caused by sudden process transition from 0.35μm CMOS to 0.18μm CMOS, and in 2008, we also saw another drop by process transition from 90nm CMOS to 65nm CMOS.

Fig. 2.3.1(b) shows trends of designed chip area, which shows much clear trends of drop by process migration. On the other hand, Fig. 2.3.1(c) shows trends of designed chip area normalized by design rule, which assume to be strong relation with design efforts. Coming from the fact that the normalized chip area is still growing, we assume the major reason for decrease of number of chips and designed area is increase of design effort per chip and per unit area due to process scaling.

Fig. 2.3.2 shows trends number of professors and universities fabricated chip. Number of professors who have contracted NDA for process technologies to access design rules and design libraries are, 91, 287, and 48, respectively, for 65nm CMOS, 0.18μm CMOS, and 0.8um CMOS.

2.3.2 Overview of chip fabrication in 2018

Table 2.3.1 lists chip fabrication schedule in 2019. Please refer to list in Chapter 2 for details of designers and contents of chip designed.

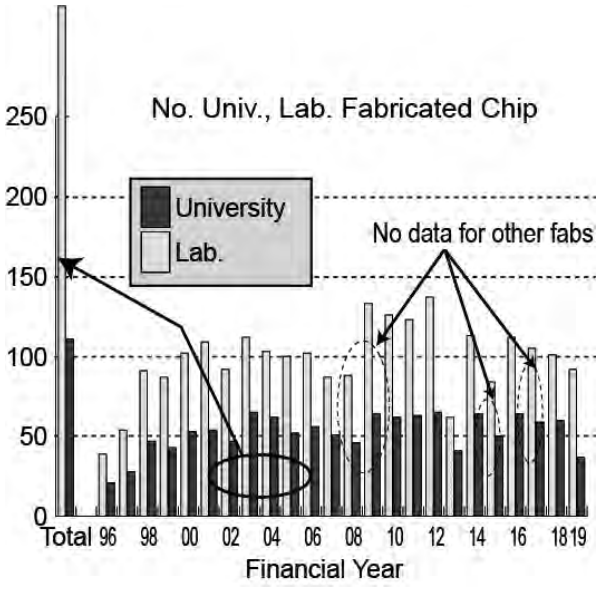


Fig. 2.3.2 Trend of number of processors and universities fabricated chip.

Table 2.3.1 Chip fabrication schedule in 2017

o0.8μm CMOS (On-Semiconductor - Sanyo)

	Chip application deadline	Design deadline	Chip delivery
2019 #1	2019/7/8	2019/9/30	2019/12/23
2019 #2	2020/1/6	2020/3/30	2020/6/18

o0.18μm CMOS (Rohm)

	Chip application deadline	Design deadline	Chip delivery
2019 #1	2019/4/1	2019/6/24	2019/10/9
2019 #4	2019/6/17	2019/9/9	2019/12/18
2019 #2	2019/8/5	2019/10/28	2020/2/20
2019 #3	2019/12/2	2020/2/24	2020/6/18

oSOTB 65nm CMOS

	Chip application deadline	Design deadline	Chip delivery
2019 #1	2019/6/17	2019/7/29	2020/2/25
2019 #2	2020/1/27	2020/3/9	2020/7E

2.3.3 Libraries and design flows

VDEC have been working to prepare design libraries and design flows for digital design and PDKs for analog design. Table 2.3.2 lists libraries available now.

Table 2.3.2 Libraries available for VDEC chip fabrication

Technology	Name	Author	Contents
0.18μm CMOS (Rohm)	Rohm library	Rohm Library Std. Cells, IO cells, RAM (Distributed with CDROM)	Synthesis(Synopsys)
			Simulation(VerilogXL)
			P&R(LEF/DEF)
	Kyodai Library	Onodera Lab., Kyoto University	Synthesis(Synopsys)
			Simulation(VerilogXL)
			P&R(Astro)
	Todai Library	VDEC Design flow based on library prepared by Onodera Lab., Kyoto University	Synthesis(RTL Compiler)
			Simulation(VerilogXL)
			P&R(Encounter)
	PDK	VDEC	PDK(IC6.1)

2.4 Seminar

Seminars are always needed as the advancement of LSI design technology. In 2019, VDEC has held CAD Seminar, Refresh Seminar, and Designer's Forum, for academic and industrial circuit designers.

2.4.1 CAD Seminar for VDEC users

Along with advancement of circuit design CAD tools, tutorials on these tools are highly demanded. VDEC offers the CAD Seminar twice per year. In the CAD Seminar, VDEC invites lecturers from venders including Cadence, Synopsys and Keysight to give tutorials on their CAD tools. The seminar is held in VDEC, The University of Tokyo and VDEC sub-centers simultaneously in several universities nationally, August, September, and March of one fiscal year. Each tutorial takes one or two days.

Table 2.4.1 CAD technical seminar in 2019 fiscal year
CAD Seminar I

Date	Seminar	Venue	Attendees
8/21	Synopsys Sentaurus (TCAD)	The Univ. of Tokyo	10
8/21	Synopsys Sentaurus (TCAD)	Nagoya Univ.	0
8/21	Synopsys Sentaurus (TCAD)	Osaka Univ.	2
8/21	Synopsys Sentaurus (TCAD)	Akita Prefectural Univ.	4
8/21	Synopsys Sentaurus (TCAD)	Shinshu Univ.	3
8/28	Synopsys HSPICE	The Univ. of Tokyo	8
8/29	Keysight GoldenGate	The Univ. of Tokyo	2
8/29	Keysight GoldenGate	Hiroshima Univ.	5
8/29	Keysight GoldenGate	Akita Prefectural Univ.	4
8/29	Keysight GoldenGate	Shinshu Univ.	6
9/17, 18	Cadence Virtuoso Analog Design Environment (ADE) Explorer	The Univ. of Tokyo	7
9/17, 18	Cadence Virtuoso Analog Design Environment (ADE) Explorer	Kyoto University	5
9/17, 18	Cadence Virtuoso Analog Design Environment (ADE) Explorer	Hiroshima Univ.	1
9/17, 18	Cadence Virtuoso Analog Design Environment (ADE) Explorer	Akita Prefectural Univ.	3
9/17, 18	Cadence Virtuoso Analog Design Environment (ADE) Explorer	Shinshu Univ.	6
44094	Synopsys PrimeTime (Basic)	The Univ. of Tokyo	6
44094	Synopsys PrimeTime (Basic)	Hiroshima Univ.	1
9/24, 25	Cadence Virtuoso Analog Design Environment (ADE) Assembler	The Univ. of Tokyo	6
9/24, 25	Cadence Virtuoso Analog Design Environment (ADE) Assembler	Nagoya Univ.	0
9/24, 25	Cadence Virtuoso Analog Design Environment (ADE) Assembler	Kyoto University	6
9/24, 25	Cadence Virtuoso Analog Design Environment (ADE) Assembler	Hiroshima Univ.	1
9/24, 25	Cadence Virtuoso Analog Design Environment (ADE) Assembler	Akita Prefectural Univ.	2
9/24, 25	Cadence Virtuoso Analog Design Environment (ADE) Assembler	Shinshu Univ.	7

CAD Seminar II
In this fiscal year, CAD Seminar II was held online due to the pandemic of COVID-19.

Date	Seminar	Venue	Attendees
3/12	Cadence PVS	WebEx	21
3/13	Cadence Quantus	WebEx	15
3/16	Cadence System Verilog Real-Number Modeling	WebEx	17
3/19	Synopsys SiliconSmart	WebEx	13
3/24, 25	Cadence SKILL	WebEx	24
3/16	Synopsys StarRC	WebEx	14

2.4.2 Refresh Seminar for industry and academia

The fundamental and advanced knowledges are both imperative to integrated circuit design. VDEC offers the Refresh Seminar for industrial and academic people. University professors and highly experienced engineers are invited to give lectures on circuit design, covering the topics on analog, digital, RF, MEMs, and basic design flow. The seminar was originally launched in 1998, with the support of Ministry of Education Technical Education Division. It is now being supported by several industrial/academic societies.

Fig. 2.4.2 Refresh Seminar at VDEC seminar room at the University of Tokyo, VDEC.

Table 2.4.2 Refresh Seminar

Date	Course	Contents	Lecture	Attendees
6/24, 26	Analog Circuit Design	Analog Circuit Design and simulation Integrated Circuits Verification (LVS, DRC)	Masahiro Sugimoto (Chuo Univ.) Hidetoshi Onodera (Kyoto Univ.) Koji Kotani (Tohoku Univ.)	45
6/11, 12	MEMS Design	MEMS Basic 1: Fabrication Process MEMS Basic 2: Operation Principle Structural Design Layout Design	Yoshio Mita (The Univ. of Tokyo)	8
7/9, 10, 11	MEMS Fabrication	CAD Design and Analysis Lithography, Etching, Release Vibration measurement and analysis	Yoshio Mita (The Univ. of Tokyo)	4
8/5, 6	CMOS-RF Circuit Design	Modulation/Demodulation Cascaded connection Basic Performance Transceiver Architecture Circuit Element Design Flow	Hiroyuki Ito (Tokyo Inst. of Tech.)	10
8/8, 9	VDEC Transistor-Level Circuit Design Flow	Custom circuit design flow using VDEC-collaborated CAD environment and process	Toru Nakura (Fukuoka Univ.)	7
8/19, 20	VDEC Digital Circuit Design Flow	Digital circuit design flow using VDEC-collaborated CAD environment and process	Kazutoshi Kobayashi (Kyoto Institute of Technology)	3

2.4.3 Designer's Forum for academia

VDEC LSI designer forum intended for students and young teachers were held. The VDEC LSI designer forum has aimed to sharing the information that generally hard to be obtained common technical reports or academical papers, such as the failure an LSI designer had been through and the solution, and the construction method in the design milieu in the laboratory.

Table 2.4.3 Program of Designers Forum in 2019

9/27, 28 Tendo Hot Spring, Yamagata Attendees: 27	
9/27	
12:00-12:30	Reception
12:40-14:20	VDEC Design Award Presentation I
14:30-16:10	VDEC Design Award Presentation II
16:20-17:40	VDEC Design Award Presentation III
19:00-	VDEC Design Award Ceremony
9/28	
9:00-10:00	Idea Contest Presentation
10:00-12:00	Ph.D Session
12:00-13:00	Plenary Talk
13:00-13:10	Closing

2.5 Facilities

The dlab/VDEC has been providing the big facilities for universities in Japan from its establishment (1996). Big facilities refer to those which are impossible to acquire and or maintain by an individual research unit. Table 1.5.1 shows the available facilities of VLSI testers and some process machines, which are placed at the tester room (VDEC 104), the super clean room, the backend process room (VDEC 204) of the Takeda building. In 2004, the VLSI tester (T2000) and the EB lithography machine (F5112+VD01) were donated to the VDEC by the ADVANTEST. In the year 2012, VDEC joined MEXT (Ministry of Education)'s Nanotechnology platform to enforce its multi-use capability. (For Nanotechnology Platform refer section 1.8).

Major apparatuses purchased through VDEC and affiliated laboratories courtesy include: High definition Scanning Electron Microscope (SEM) Hitachi Regulus SU-8230 and SEM with Energy dispersive X-ray spectroscopy (EDX) JSM-6610LV. Also, a 1kW CO_2 Laser cutter capable of cutting 3mm-thick Aluminum plates has been moved to VDEC backend room (204) The facilities can be used by user himself, after a couple of times' training by attendance of licensed users; also, by presence of licensed persons, a new user can readily use the machine.

Table2.5.1 Available facility list

Facility	Equipment name	Description	Status	Contact
Logic LSI test System	EB tester: IDS10000	The chip surface voltage during operation can be measured with the LST tester. The digital circuit with 384 pins, 1GHz can be tested.	Available	nanotech@so-go.t.u-tokyo.ac.jp
	LSI tester: ADVANTEST T2000	The digital circuit with 256 pins, 512MHz can be tested. Analog test is optional.	Available	nanotech@so-go.t.u-tokyo.ac.jp
	Auto prober: PM-90-A	Automated prober for testing LSI wafers, which can be used with the LSI testers. The probe card for LSIs with the VDEC standard pin connections is available.	Available	nanotech@so-go.t.u-tokyo.ac.jp
Analog/RF measurement system	Analog/RF measurement system: B1500A, 4156B, HP4284, etc	DC parameter measurement, Capacitance measurement, Network analyzer, Spectrum analyzer, etc.	Available	nanotech@so-go.t.u-tokyo.ac.jp
	Low-noize manual prober: Cascade Microtec	6 inch wafer can be measured with six DC probles and two RF probes upto 50 GHz.		
	Low-noize, temperature controlled semi-auto prober: Süss Microtec	8inch wafer can be measured. The chip temperature range is -50 to 200℃.		

Nanotechnology Platform Apparatuses	Mask lithography, Direct lithography: F5112+VD01	Minimum linewidth: 50nm. Lithography for 5 inch photomask (thickness: 2.3 mm), 2-8 inch wafers, and chips is possible.	Available	nanotech@sogo.t.u-tokyo.ac.jp
	Rapid Mask and Direct lithography: F7000S-VD02	Minimum linewidth: 1xnm. Lithography for 5 inch photomask (thickness: 2.3 mm), 2-8 inch wafers, and chips is possible. Stencil character projection of non-square shapes such as circle, triangle is possible.	Available	
	Chlorine ICP plasma etcher CE-S	High density plasma etching with Cl2 and BCl3 is possible.	Available	
	Silicon DRIE MUC-21 ASE-Pegasus	High speed, high aspect ratio etching of silicon is possible	Available	
FIB system	FIB: SII XVision200TB	Repair of photomask, sample etching, etc. (Through Nanotech. Platform and LCNet)	Available	
LSI FIB system	FIB: FEI V400ACE	Repair of VLSI from both frontside and backside, with CAD navigation and / or IR camera is possible. W/SiO_2 deposition is possible.	Available	
Chip Bonding System	Wedge Bonder: Westbond 7476D	25μmϕAl or Au wire wedge bonding machine.	Available	
	Epoxy Die Bonder Westbond7200C	Precision Manupilator system. Epoxy and or Ag paste chip bonding and or glued wiring.		
	Semi-Auto Bonder Westbond4700E	18～25μmϕAu Ball bonding or bump creation.		
	Precision Manual Flip-Chip Bonder Finetech Fineplacer Lambda	Face-to-face bonding up to 15mm square chips. Alignment is through video camera. Bonding is by heating chips with TV camera. (Ultrasonic Unit can additionally be purchased.) XY±0.5μm, and θ=1mrad precision.		

2.6 Activity plan for 2020

VDEC will continue activities on chip fabrication services, CAD tool support, dispatching design related information and dovnated division "D2T", as has been previous years.

【Design related information dispatching/Seminar】

We will continue holding the following seminars: (1) CAD tools seminars which have been continued since 1997, (2) "Refresh seminar" since 1998, (3) "Designer' Forum" since 1997. We will also continue seminars for LSI tester usage at VDEC and subcenters, workshops on LSI testing technologies initiated by D2T.

【CAD tool support】

We will continue Cadence tools, Synopsys tools and Mentor tools as the main stream design tools. We will continue analog RF design environment, GoldenGate and ADS by Agilent, C-based design environment, BachC by Sharp. In addition, we continue trial of several CAD tools, such as layout platform, Lavis by TOOL. Design debugging platform from SpringSoft has merged into Cadence tools and will be continued.

【Chip fabrication services】

We will continue chip fabrication services for 0.18μm CMOS by Rohm and 0.8μm CMOS by On-semiconductor-Sanyo as the regular services. Chip fabrication services for SOTB 65nm CMOS by Renesas Electronics will be terminated.

Table 2.6.1 Chip fabrication schedule

【CMOS 1.2μm 2P2M】 On-Semiconductor(Former Motorola Japan)

	Chip application deadline	Design deadline	Chip delivery
2020#1	2020/4/13	2020/7/6	2020/9/28
2020#2	2020/10/12	2021/1/12	2021/3/29

【CMOS 0.18μm 1P5M(+MiM)】 Rohm

	Chip application deadline	Design deadline	Chip delivery
2020 #1		2020/3/16	2020/6/8→6/29
2020 #2		2020/6/15	2020/9/7
2020 #3	2020/5/11	2020/8/3	2020/10/26
2020 #4	2020/9/7	2020/11/30	2021/2/22

【SOTB CMOS 65nm】 Renesas Electronics

	Chip application deadline	Design deadline	Chip delivery
2020 #1		2020/7/20	2020/8/24

2.7 Venture companies related to VDEC

Some professors related to VDEC started venture companies. The following is a list of the venture companies related to VDEC.

[1] AIL Co.,Ltd. (http://www.ailabo.co.jp/)

Related professor : Professor Kazuo Taki, Kobe Univ. (Representative Director)

Description of business : (1) LSI design service
(2) Engineer dispatching service

[2] Synthesis Corporation
(Merged with Soliton Systems on July 1st in 2017, http://www.synthesis.co.jp/)

Related professor : Professor Emeritus Isao Shirakawa, Osaka Univ. (Director)

Description of business : (1) System LSI development and design service
(2) IP development and sales
(3) Development and sales of IPs
(4) Development of EDA tools

[3] ASIP Solutions (http://www.asip-solutions.com/)

Related professor : Professor Masaharu Imai (Representative Director, CTO)

Description of business : (1) R&D, education and consulting of IoT application system
(2) Sales of ASIP design tool and consulting of ASIP development

[4] Nanodesign Corporation (http://www.nanodesign.co.jp/)

Related professor : Professor Kazuyuki Nakamura, Kyushu Institute of Technology. (Rep-resentative Director)

Description of business : (1) LSI design and development
(2) Design consulting, etc.

[5] A-R-Tec Corp. (http://www.a-r-tec.jp/)

Related professor : Professor Emeritus Atsushi Iwata, Hiroshima Univ. (Representative Director)

Description of business : (1) Design and measurement of IC and evaluation board
(2) Crosstalk noise analysis
(3) Develop human resources for new employees and beginners

[6] Ishijima Electronics (http://ishi.main.jp/)

Description of business : (1) Electronic circuit and board development
(2) Software development
(3) Consulting

2.8 "Nanotechnology Platform": Ultra Small Lithography and Nanometric Observation Site

d.lab/VDEC is operating an open-use nanotechnology platform "Ultra Small Lithography and Nanometric Observation Site" together with the Institute of Engineering Innovation of Graduate School of Engineering. The site is supported by Japanese Ministry of Education (MEXT)'s Nanotechnology Platform grant. Any researchers in Japanese Universities, Laboratories, and Companies can take full advantage of The University of Tokyo's cutting-edge nanotechnology apparatuses and know-hows. The accessible technology includes Lithography and Etching environment, Ultra High-Voltage Acceleration (1MV) transmission electron microscope (TEM) that is capable of visualizing upto light materials such as Nitrogen. VDEC takes part in the lithography at Takeda Sentanchi Super Cleanroom. Through VDEC's key apparatus F5112+VD01 donated from Advantest Corporation as well as F7000S-VD02 purchased by national budget, VDEC is supporting post-VLSI activities such as MEMS. The machine is capable of rapidly writing patterns on arbitrary-shaped targets sizing from 1cm-sqare chip to 8-inch round wafers. The performance is measured by the number of research reports and machine use. The University of Tokyo site has received 158 research reports from 158 research groups. As shown in example of EB writer exposure count per month (that exceeds 210 per month) in the Fig. 1, machine usage is monotonously increasing. "Open ratio", which is the number of days in which users outside the University of Tokyo came, divided by machine open days, was 99%. Due to the strong support of nanotech. Platform, even a novice user can obtain fine lithography result by using the apparatuses with the Platform engineering staffs of VDEC. Consequently, free machine time is decreasing so the team is trying to acquire financial support to increase the number of machines. Also from FY2019, the French Nanotechnology Network project CNRS-RENATECH asked to the UTokyo VDEC to share the good practice. Also d.lab was invited by Organisation for Economic Co-operation and Development (OECD)'s international workshop for national infrastructure strategy.

URL:http://nanotechnet.t.u-tokyo.ac.jp/

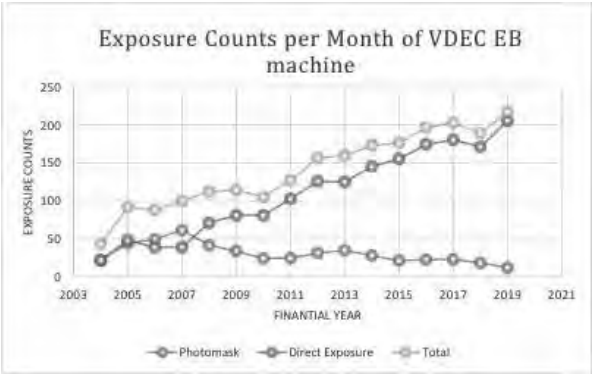


Figure 1: Monthly Average Exposure Count of EB Machine (s).

Chapter3 Activity Report of ADVANTEST D2T Research Division

3.1 Introduction of ADVANTEST D2T Research Division

3.1.1 Aim of establishing ADVANTEST D2T Division

ADVANTEST D2T research division was established in VDEC in October 2007. As the name suggests, it is financially supported by ADVANTEST Corporation.

The aim of establishing ADVANTEST D2T research division was to promote the research and education environment with regard to VLSI testing in all universities and colleges in Japan. "D2T" signifies that we consider not only design but also testing. Through our activities, we hope to provide expertise in design and testing for the industry. In addition, we are exchanging researchers with those of other universities and research institutes both in Japan and overseas. Moreover, D2T research division is suitable for collaborations with the industry because VLSI testing is one of the most practical research topics in the industry. On the basis of these activities, our final goal is to become a center of excellence of VLSI testing in Japan.

D2T research division has spent a total of 12 years to develop the first (Oct. 2007 – Sep. 2010), second (Oct. 2010 – Sep. 2013), third (Oct. 2013 – Sep. 2016), and fourth (Oct. 2016 – Sep. 2019) phases. D2T activity report of 2019 presents the last financial year, i.e., Oct. 2018 – Sep. 2019, of the fourth phase. Systems Design Center, School of Engineering, the University of Tokyo has been established in Oct. 2019, and Advantest D2T research department is within the center. D2T research department primarily focuses on D2T research activities and education. The fifth project phase (Oct. 2019 onwards) of D2T project will be commenced by courtesy of ADVANTEST Corporation.

In this financial year, we invited Professor Gilgueng Hwang from CNRS, University of Paris-Saclay (2019/7 – 9) and Professor Tsung-Hsein Lin (2019/8 – present) from National Taiwan University for research and educational collaboration with d.lab-VDEC.

The details pertaining to the activities of our group are presented in the following sections.

3.1.2 Members of ADVANTEST D2T Division

Project Professor	Masahiro Fujita
Project Associate Professor	Gilgueng Hwang (2019/7 – 9)
Project Professor	Tsung-Hsein Lin (2019/8 – present)
Project Lecturer	Akio Higo
Researcher	Koji Asami (Advantest Laboratories Ltd.)
Researcher	Takahiro Yamaguchi
Assistant Clerk	Makiko Okazaki

3.2 Report of the 14th D2T Symposium

The 14th D2T Symposium was held on September 6, 2019, at Takeda Hall. This year, we invited the following overseas lecturers to introduce their research on biosystems, RF, IoT, and machine learning: Alan Mishchenko, University of California, Berkeley; Prof. Degang Cheng, Iowa State University; Prof. Tsung-Hsien Lin, National Taiwan University; Assoc. Prof. Gilgueng Hwang, CNRS, University of Paris-Saclay; Prof. Priyank Kalla, The University of Utah; Prof. Kwang-Ting (Tim) Cheng, Hong Kong University of Science and Technology; and Prof. Adit Singh, Auburn University.

We sincerely appreciate each participant for their contributions to the symposium. We look forward to greater participation again at the next symposium.

14th D2T Symposium program

10:00	**Opening Remarks** **Masahiro Fujita** (Director, VDEC, The University of Tokyo) **Yoshiaki Yoshida** (President & CEO, ADVANTEST CORPORATION)
10:15	**Session 1** (Chairpersons: Masahiro Fujita, Zule Xu, Nguyen Ngoc MAI-KHANH VDEC The University of Tokyo) Circuit-Based Intrinsic Methods to Detect Overfitting **Alan Mishchenko**, Full researcher (University of California, Berkeley) Effective and practical AMS DfT techniques for achieving robust performance and life-time reliability Degang Chen, Professor (Iowa State University) Sensor Readout Circuits for IoT/Bio-Medical Applications **Tsung-Hsien Lin,** Professor (National Taiwan University)
12:30	**Lunch**
14:00	**Session 2** (Chairperson: Yoshio Mita, VDEC, The University of Tokyo) Design, Fabrication and Characterizations of On-chip Micro/nanorobotic Swimmers Toward Biological Applications **Gilgueng Hwang**, Associate professor (CNRS, University of Paris-Saclay) Design Automation for Silicon Nanophotonic Integration **Priyank Kalla** (The University of Utah)
15:30	**Break**
16:00	**Session 3** (Chairperson: Virendra Singh, Dept. of EE, Indian Institite of Technology Bombay) Electronic-Photonic Design Automation **K.-T. Tim Cheng**, Professor (Hong Kong University of Science and Technology) The Next Major Test Challenge: Low Power Designs Adit Singh, Professor (Auburn University) **Session 4** Recent D2T research division progress **Akio Higo**, Lecturer (VDEC, The University of Tokyo)
17:55	**Closing**
18:00	**Reception**

3.3 Research Activity Reports of the ADVANTEST D2T Research Division

High-Resolution Analog-to-Digital Converter Based on Stochastic Comparators

Takahiro J. Yamaguchi, Akio Higo, Tetsuya Iizuka

This project aimed to explore stochastic analog-to-digital converter (ADC) architectures. Process variations, along with many factors such as voltage or temperature variations, lead to mismatched design parameters that in turn result in input-referred offsets. Thereby, non-linearity and missing output codes occur in an ADC. Instead of attempting to suppress such process variations as in conventional ADCs, the stochastic ADC approach exploits the stochastic properties of several comparators, such as the random variation of input-referred offset and Gaussianity of the internal noise, to enhance the quantization accuracy. To validate the theory for detecting the level-crossing time using a stochastic median, both numerical experiments and experiments using the CMOS comparator array were performed. These experiments use N comparators and detect the level-crossing times of a ramp input under the condition of external noise = zero, and non-zero internal noise with various process variations. The theory has been verified experimentally using a prototype CMOS comparator array, which consists of 256 differential comparators. The experiments were performed under the conditions of external signal in the form of a step input, zero external noise, and non-zero internal noise with process variations. The theory was also validated in the voltage domain via application of the step input to the comparator array. This allowed for the prevention of complicated and time-consuming measurement processes in the time domain.

High-Performance Analog-to-Digital Conversion Using the Wideband Spread Spectrum and Its Applications

Koji Asami, Byambadorj Zolboo, Akio Higo,
Tetsuya Iizuka, Masahiro Fujita

To measure low-cost RF devices for IoT and other applications, low-cost and high-efficiency analog-to-digital conversion techniques are required. To acquire narrow-band modulation signals scattered over a wide frequency range, a compression sampling method was investigated herein.

In this financial year, we constructed a theoretical formula for the Noise Figure and confirmed its validity using actual experimental equipment. This result was submitted to the IEEE TCAS-I. Moreover, via analysis of the performance degradation factors involved in the implementation, we devised a calibration method and confirmed its use by means of simulation.

High-Throughput and High-Accuracy Electron-Beam Direct Writing (EBDW) Strategy for Wide Range of EBDW Applications

Akio Higo, Yoshio Mita, Masahiro Fujita

Maskless lithography via electron-beam direct writing (EBDW) is expected to be a low-cost lithography technology with a short turn-around time (TAT). However, it presents some drawbacks such as low process throughput and low accuracy against the intended layout shapes. We are pursuing a high-speed and high-accuracy EBDW strategy utilizing the character projection (CP) method to overcome these concerns and boost EBDW use in fields such as MEMS and photonics.

We investigated the fabrication process for the high-resolution observation of lithographic results using our high-throughput and high-accuracy EB exposure strategy, which combines the CP and variable-shaped beam (VSB) methods. We fabricated aluminum thin film periodic CP/VSB nanostructures on a quartz plate via CP and VSB on a glass substrate and measured the optical characteristics.

3.4 Publications

International Journals

[1] Akio Higo, Tomoki Sawamura, Makoto Fujiwara, Eric Lebrasseur, Ayako Mizushima, Etsuko Ota, Yoshio Mita, "Experimental Comparison of Rapid Large-area Direct Electron Beam Exposure Methods with Plasmonic Devices," Sensors and Materials, Vol.31, No.8, pp.2511-2525, 2019 (2019.05) doi: 10.18494/SAM.2019.2443

Kuroda Laboratory

(http://www.kuroda.t.u-tokyo.ac.jp/index.html)

TCI:ThruChip Interface

T. Kuroda, M. Hamada, T. Shidei, M. Okada, Wai-Yeung Yip

TCI is a 3D integration technology that employs inductive coupling between coils created with on-chip metal line patterns for data communication across stacked chips. It realizes the same or better performance as TSV (Through Silicon Via) but at a lower cost. Last year, we presented the HDSV (Highly Doped Silicon Via) technology which enables power delivery without using TSV for TCI stacked chips, and the TCI 2.5-D integration technology.

TLC:Transmission Line Coupler

T. Kuroda, M. Hamada, T. Shidei, M. Okada, Wai-Yeung Yip

TLC is a data communication technique between circuit boards by utilizing electromagnetic coupling between transmission lines on them. It solves the issues in conventional connectors such as wearing, reliability against vibration, and impedance mismatch, realizing wireless connectors. Last year, we successfully realized a demonstration of wireless connectors for USB3.0 signals.

Ikeda Laboratory

(http://www.mos.t.u-tokyo.ac.jp)

Current Research Projects

Design Optimization of High-Performance Cryptographic Engine

M. Ikeda, K. Ikeda, F. Arakawa

We have explored the optimal design of data-path for high-performance encryption engine for such application spanning from cloud to sensor-node. One of the issues for such high-performance cryptographic design in ASIC is the manufacturing cost, and there exists difficulty of re-implementation of mathematical formulas and parameters used for cryptography, according to the standard change. In this study, we have explored design spaces with parameters such as cryptographic curves, structure of arithmetic units, and the number of parallel operations, and obtained optimal design parameters in terms of throughput and latency. We established HDL generation for the obtained optimal designs. On the other hand, it is also important to build Trusted Execution Environment (TEE) for systems using cryptographic engines. we participated in the task group to extend the specifications for TEE of the RISC-V architecture and proposed specifications suitable for IoT systems. We also evaluated the area overhead of hardware for TEE and examined its applicability to small-scale processors for IoT.

Functional Encryption Engine Design

M. Ikeda, C.Cai, S. Sugiyama, and R. Nakayama

High-functional cryptography exemplified by searchable encryption and ID and attribute-based encryption is the basis of privacy guard, that is the biggest concern in cloud services. Functional cryptography has a disadvantage that the cryptographic algorithms used for its implementation has high computational cost. In this study, we implemented and optimized two main algorithms, optimal Ate pairing on elliptic curve and fully homomorphic encryption (FHE). In both cases, we employed operations on quotient ring as the unit of arithmetic, and constructed pipeline by unrolling loop that is small but repeated many times in the algorithms. By optimizing data flow of the pipeline, we have realized 8.2 us per pairing. For the case of FHE, we achieved 19.2 times better throughput (synthesize result) compared to GPU.

A study on hardware implementation of reservoir computing system

M. Ikeda, C.Cai and B. Amartuvshin

The hardware realization of artificial neural networks (ANNs) is a challenging task due to large re-

source requirements of the involved operations. Reservoir computing (RC), based on a random recurrent neural network (RNN), is a simple yet powerful model that is well suited for time-series data processing. It consists of a reservoir for mapping inputs into a high-dimensional space and a readout for pattern analysis from the high-dimensional states in the reservoir. The reservoir is fixed and only the readout is trained with a simple method such as linear regression and classification. Thus, the major advantage of reservoir computing compared to other recurrent neural networks is fast learning, resulting in low training cost. We are trying to propose digital hardware implementations of echo state network (ESN) designed for brain-computer interface based on EEG time-series data with online learning capability.

Self-Synchronous Circuits Design

M. Ikeda, and D. Cui

We have been working on the research of high throughput gate-level pipeline self-synchronous circuits free from timing errors. The dual-pipeline self-synchronous logic gate duplicates the DCVSL circuit into two identical pipelines and uses the same completion detection signal to control both pipelines. When one pipeline is in the evaluation phase, the other pipeline must be in the pre-charge phase, results in concealing of pre-charge time and control. Gate-level pipeline enables throughput enhancement. Besides the high-throughput operation, we are trying to design the self-synchronous arithmetic units which can also allow for latency reduction and area utilization improvement.

Advanced 3-D Measurement System by Smart Image Sensors and Secure Sensing

M. Ikeda, N. Takeda, Y. Liu,
D. Jiang, and N. Watanabe

We have been working toward the advanced 3-D measurement system with secure sensing scheme by integrating smart signal processing functionality onto the smart image sensors. We have studied ToF image sensor with current mode background suppression capability for modulated light projection. We have also studied ToF image sensor with light to pulse frequency modulation pixel for both background suppression and digital signal selection capabilities.

Design and Measurement of Weak-Signal-Readout Integrated Circuit for Terahertz-Video-Imaging

M. Ikeda, and T. Kikkawa

We designed a readout integrated circuit (ROIC) for Terahertz-Video-Imaging which converts a weak signal detected by InAs MOS-HEMT to digital signal. The ROICs are integrated as 8x7 array on 180nm CMOS and utilized with the detectors stacked on them. Each ROIC contains transimpedance amplifier, lock-in amplifier and ΔΣ analog-to-digital converter as well as digital-to-analog converter to calibrate the detectors. In our work, several control parameters and digitized signals are serially communicated by serial peripheral interface (SPI). The fabricated chip is stacked with array of antennas and InAs MOS-HEMT detectors integrated on a glass substrate by stud bumps. By measurement with a THz signal generator, we realized synchronous-detection of the signal under a noise equivalent power (NEP) of 0.215pW/√Hz.

Fujita Laboratory

(http://www.cad.t.u-tokyo.ac.jp/)

Synthesis and Generalization of Parallel Algorithm for Matrix-vector Multiplication

Masahiro FUJITA, Akihiro GODA, Ashish MITTAL,
Yukio MIYASAKA

Recently, there have been more chances to calculate matrix-vector multiplication due to the growing use of the neural network. We have proposed the method to automatically synthesize the optimum parallel algorithm for the given environment and synthesized an algorithm for matrix-vector multiplication of a specific size matrix with 4 nodes connected in a one-way ring. This work proposes a method to generalize the synthesized algorithm to deal with any size matrix. We generalized the synthesized algorithm for the 32 × 32 matrix to calculate N × N matrix-vector multiplication.

Synthesis and Generalization of Parallel Algorithms Considering Communication Constraints

Masahiro FUJITA, Yukio MIYASAKA,
Amir Masoud GHAREHBAGHI, Akihiro GODA

Recently, the opportunities of parallel computing are expanding rapidly in various applications including neural networks and machine learning. It is, however, not at all straightforward to develop an efficient algorithm for each parallel computing environment since communications always introduce overhead in computation. In this work, we propose a design method of optimum parallel computing under user-specified communication constraints. The basic strategy is to automatically generate optimum scheduling from small instances of the target problem and then they are semi-automatically generalized to much larger problems. Several experiments targeting matrix vector multiplication and convolutional neural networks have been conducted. Their results show the correctness and usefulness of the proposed method as well as its scalability.

Signal Selection Methods for Debugging Gate-Level Sequential Circuits

Masahiro FUJITA,
Amir Masoud GHAREHBAGHI, Yusuke KIMURA

This work introduces methods to modify a buggy sequential gate-level circuit to conform to the specification. In order to preserve the optimization efforts, the modifications should be as small as possible. Assuming that the locations to be modified are given, our proposed method finds an appropriate set of fan-in signals for the patch function of those locations by iteratively calculating the state correspondence between the specification and the buggy circuit and applying a method for debugging combinational circuits. The experiments are conducted on ITC99 benchmark circuits, and it is shown that our proposed method can work when there are at most 30,000 corresponding reachable state pairs between two circuits. Moreover, a heuristic method using the information of data-path FFs is proposed, which can find a correct set of fan-ins for all the benchmark circuits within practical time.

Approximate Arithmetic Circuit Design Using a Fast and Scalable Method

Masahiro FUJITA, Amir Masoud GHAREHBAGHI,
Qi LU

Approximate computing can be applied to error tolerant applications, by trading off accuracy for lower power consumption, shorter delay and smaller area. In this work, we focus on the approximate arithmetic circuit design especially targeting combinational multipliers and adders, which are essential computing components in machine learning such as neural network computation. We propose a novel approach to generate approximate circuits from the given correct circuits. The basic idea is to study the circuit's characteristics from the small instances of the circuits and then establish a common algorithm for larger circuits with the same architectures. We propose two different methods and apply them to adders and multipliers with different architectures. The experimental results demonstrate that our method outperforms the state-of-art methods in terms of the quality of the circuits with orders of magnitude shorter processing time.

An Automatic Test Pattern Generation Method for Multiple Stuck-at Faults by Incrementally Extending the Test Patterns

Masahiro FUJITA, Amir Masoud GHAREHBAGHI,
Peikun WANG

As the number of transistors in the fabricated circuits becomes extremely larger, not only single stuck-at faults, but also multiple stuck-at faults are likely to happen in the circuits, especially for the large-scale circuit. Multiple faults are difficult to be fully covered due to the exponentially enormous number of all possible faults. Although there are methods proposed to deal with the multiple faults, they fail to generate compact test patterns to detect all faults within an acceptable running time. In order to solve these problems, this work proposes an incremental Automatic Test Pattern Generation method to deal with multiple stuck-at faults. Instead of traversing the entire n multiple fault list, the proposed method only selects the faults undetected by the existing test patterns for n-1faults, and then generates addi-

tional test patterns. Staring from a complete test set for single faults, the proposed ATPG method can be incrementally applied to handle all multiple faults. Moreover, since the number of undetected faults that are selected is extremely smaller comparing to the total number of the entire fault list, the proposed method can generate compact test patterns to cover all faults within an acceptable running time.

Kobayashi Laboratory
(http://nano-lsi.iis.u-tokyo.ac.jp/)

Device Physics on Negative Capacitance Transistor

Masaharu Kobayashi and Toshiro Hiramoto

Negative capacitance transistor (NCFET) using ferroelectric-HfO_2 gate insulator is a promising transistor technology that can realize sub-60 subthreshold slope (SS) for low voltage operation. However, the physical mechanism of sub-60 SS and unique phenomenon in NCFET remains to be understood. In this work, by using the transient negative capacitance theory based on the dynamics of ferroelectric material, we successfully built the model of negative differential conductance and reverse DIBL uniquely seen in NCFET.

Demonstration of an IGZO Channel FeFET for 3D-Stacked High-Density Memory Application

Masaharu Kobayashi and Toshiro Hiramoto

Ferroelectric transistor (FeFET) memory is a promising low-power and high-density memory by using CMOS-compatible HfO_2 material. To compete with flash memory for storage application, it is important to solve reliability issues and realize 3D-stacked low-cost and high-density memory. In this work, for 3D-stacked FeFET, we proposed FeFET by using IGZO channel instead of poly-Si channel. We were able to fabricate FeFET device by low temperature process below 400oC without forming an interfacial layer which can be the cause of reliability issues. We demonstrated low voltage switching at less than 3V with nearly ideal subthreshold slope.

Modeling and Design of Nonvolatile SRAM and FeFET Using Ferroelectric HfO_2.

Kiyoshi Takeuchi,

Masaharu Kobayashi and Toshiro Hiramoto

Ferroelectric memory device using ferroelectric-HfO_2 is expected to be CMOS-compatible, low-cost and low-power memory. Although the researches on a single memory device have been extensively done, only a few studies have been done addressing technical challenges in memory device scaling and cell array. In this work, we built models taking into account the variability in ferroelectric HfO_2 memory devices. We revealed the scalability and an optimum design of nonvolatile SRAM for normally-off computing in IoT applications. We also proposed optimum FeFET cell designs considering read and write disturb in a cell array configuration.

Iizuka Laboratory
(http://www.mos.t.u-tokyo.ac.jp)

Waveform Reconstruction Technique for Wideband Signal

Tetsuya Iizuka, Byambadorj Zolboo

The Modulated Wideband Converter (MWC) is one of the promising Sub-Nyquist sampling architectures for sparse wideband signal sensing, cognitive radio applications and so on. Since resources within Automatic Test Equipment (ATE) are limited on sampling rate, the MWC can be useful for testing devices with various frequency band.

In this research, we are investigating a feasibility of MWC to reconstruct a waveform of sparse wideband signals for measurement equipment. We created a simulation platform system of MWC in MATLAB environment and the MWC system perfectly reconstructs the waveform of original wideband signal under several ideal assumptions. But in practical implementation, it could suffer in some drawbacks due to non-ideal components and noisy situation.

Therefore, we implemented a single-channel MWC using off-the-shelf analog components. The reconstruction performance based on the ideal sensing matrix was not acceptable due to the non-ideal hardware components. The conventional way of the

calibration is to stimulate the MWC with sequential single-tone signals then estimates the actual sensing matric components. This method is quiet time-consuming and inaccurate. Thus, we proposed novel calibration method for the MWC using multi-tone signal to estimate the actual sensing matrix from a single-measurement to reduce the calibration time and the timing noise. In terms of NMSE performance, the proposed calibration method has reasonably good performance compared to the conventional one.

In terms of noise performance, we proposed an average noise figure (ANF) theoretical notation to expect the noise figure of MWC. The accuracy of the analytical formula is ensured with MATLAB simulation results. We have also verified the feasibility of the analysis with the measurement in the practical implementations.

Design Automation and Optimization Techniques for Analog Integrated Circuits

Tetsuya Iizuka, Zule Xu, Naoki Ojima, Masaru Osada, Akira Matsuoka

Designing analog integrated circuits often requires time and effort, due to manual layout and parameter search. In order to reduce the burden and improve the performance, we conducted researches on the techniques for analog integrated circuits, such as design automation and circuit optimization.

We researched an automated design flow of successive approximation register (SAR) type ADC and its suitable architecture. By automating the design of ADCs, which are indispensable for signal processing systems, it is possible to quickly implement a whole system and greatly contribute to reducing costs. This year, we devised some methods for improving the performance of each circuit building block, which is fully composed of standard cells. In particular, a pre-distortion method for inverter-based resistive DACs made it possible to greatly improve the conversion linearity. We designed a 10-bit resolution SAR ADC using the proposed automated design flow and confirmed its operation by simulation. According to the simulation results, the power consumption per conversion step was estimated to be about 2.3 pJ.

In another research topic, we proposed a new loop architecture for a fractional-N PLL that achieves low phase noise and spurs in a more compact manner when compared to prior arts. By employing a dual feedback architecture based on a Harmonic Mixer (HM), the proposed PLL prevents amplification of the quantization noise generated by the fractional frequency divider (MMD; Multi-Modulus Divider), and spurs caused by the PFD/CP nonlinearity. The effects of the technique were demonstrated through measurements and simulations. Furthermore, the PLL was designed to optimize the trade-off between phase noise and power consumption.

We have also tried to optimize the ΔΣ ADC performance. We focused on Cyclic Assisted MASH (Multi-stAge noise SHaping) ADC for applications such as sensor interface, which has advantages in small area and high SNR. In this research, we analyzed the performance deterioration caused by the nonidealities such as capacitance mismatch and the finite DC gain of the amplifiers so that we could find the most significant parameter of this circuit. The first stage of this circuit is 1st order delta sigma ADC, and the second stage is cyclic ADC. The results of Simulink simulation showed that the effect of cyclic ADC's finite DC gain of the amplifier was smaller than that of other parameters, and other parameters contributed to the degradation of SNDR by 10dB from the ideal value in the worst case. In addition, we showed that the linearity requirement of the cyclic ADC was relaxed because the cyclic ADC input is only the quantization noise from the first stage.

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mm-Wave Circuit Design for Communication through Dielectric Waveguide

Tetsuya Iizuka, Nguyen Ngoc Mai-Khanh, Yoshitaka Otsuki, Daisuke Yamazaki, Takafumi Hara, Takamichi Horikawa

High-speed communication with the millimeter-wave band has been actively researched. Wireline communication with a dielectric waveguide such as polymer has been proposed and many researches have been conducted recently. It enables to increase the communication distance at low cost while maintaining the communication speed.

A power amplifier circuit is one of the most important circuit building blocks in a transmitter, and as its output power increases, the communication distance and the BER improve. In this research, we designed a power amplifier circuit with high output power using a passive power combiner, and optimized the limit of the output power. We fabricated and measured the prototype chip using CMOS 65nm process and presented the issues in parallelization.

Noise figure is an important factor in receiver design, and the amplifier at the most antenna side is by far the most important. Analyzing the transistor as linear network, its size was optimized by the available minimum noise factor, and was matched by transmission line network. However during this process it became apparent that at this frequency the insertion loss of the matching network itself is a big factor in amplifier design. In addition, multiple modulation schemes were compared by simulating with the measured frequency response of dielectric waveguide.

Signal Crosstalk Cancellation Technique for High-Speed Wireline Communications

Tetsuya Iizuka, Daigo Takahashi

With the improvement of the circuit performance due to the miniaturization of the semiconductor process, the speed of transmission has been improving. The data rate necessary for applications also has been improving because UHD TVs and automobiles with a lot of electrical equipment have been developed.

It is necessary to speed up transmission from both aspects of technology and demand, crosstalk is one of the factors hindering this. As measures for crosstalk, a method for reducing crosstalk at the receiver was proposed in the previous research. In this research, we proposed a method for reducing crosstalk at the transmitter with a delay adjustment circuit and a high-pass filter. Using simulation, we showed that the proposed method can reduce crosstalk more effectively with minimal additional circuits. The proposed crosstalk cancellation circuits have been implemented with 40nm CMOS technology. The effectiveness of the proposed crosstalk cancellation circuit even with the performance variations has been demonstrated through the detailed simulation with measured characteristics of the actual flat cables.

Takagi-Takenaka Laboratory

(http://www.mosfet.k.u-tokyo.ac.jp/)

III-V/Ge Metal-Oxide-Semiconductor (MOS) FETs and the 3 dimensional integration

S. Takagi, M. Takenaka, Kasidit Toprasertpong, Kwangwon Jo, Cheol-Min Lim, Tsung-En Lee, Sanghee Yoon, Chia Tsong Chen, Zilong Wang, Kei Sumita, Jun Takeyasu, Xueyang Han

We have conducted the research on high-performance III-V/Ge MOSFETs and the 3 dimensional stacked CMOS structures by using these high mobility MOSFETs. We have proposed the accurate evaluation method of a metal S/D formed on high-electron mobility InAs membrane channel formed by Smart-cut technology. We have also found that 0.5% tensile strain was introduced into the condensed Ge layer during additional oxidation after the initial compressive strain in condensed SiGe layer relaxed. We have also found the electron effective mobility increased when the Ge thickness was thinned down to 2.5 nm. In conjunction with the tensile strain and the thinning effect, the large electron mobility of 777 cm2/Vs in GeOI nFET was successfully obtained.

Ferroelectric gate insulator MOSFETs

S. Takagi, M. Takenaka, Kasidit Toprasertpong, Xuan Luo, Zaoyang Lin, Kento Tahara, Zeyu Wang, Eishin Nako

We have conducted the research for MOSFETs using ferroelectric gate insulators. We have confirmed ferroelectricity of ALD Hf1-xZrxO2 films on Si and the operation of MOSFETs with ferroelectric hysteresis characteristics. We have found that the Si interface with low interface trap density can be achieved by decreasing the crystallization temperature of Hf1-xZrxO2 and proposed the process design of ferroelectric-gate MOSFETs for improving memory characteristics. We have proposed a measurement technique to evaluate the charge density under the MOSFET ferroelectric gate and found the

strong coupling between the ferroelectric polarization and the interface charge traps. For the edge AI application, by utilizing the memory effect and nonlinear properties of ferroelectric insulators, we have proposed a low-training-cost reservoir computing using ferroelectric-gate MOSFETs, and successfully demonstrated the reservoir computing operation in our fabricated ferroelectric-gate MOSFETs.

On-chip/Off-chip optical interconnec

M. Takenaka, S. Takagi, Kasidit Toprasertpong, Qiang Li, Naoki Sekine, Hanzhi Tang, Dongheng Lyu, Qianfeng Chen, Dongrui Wu, Yuto Miyataket

We have investigated Si photonics for on-chip and off-chip optical interconnection for CMOS LSI. We have demonstrated a racetrack optical modulator with a III-V/Si hybrid MOS optical phase shifter for the first time. The parasitic capacitance was also successfully removed by introducing a SiO2-embedded Si waveguide for a III-V/Si hybrid MOS optical phase shifter, resulting in 10 Gbps optical modulation. We have proposed a taper-less hybrid MOS optical phase shifter using an ultrathin III-V membrane. We have also numerically analyzed an ultrathin InGaAs membrane photodetector monolithically integrated with a slot waveguide.

Si photonic integrated circuit for AI

M. Takenaka, S. Takagi, Kasidit Toprasertpong, Qiang Li, Hanzhi Tang, Shuhei Ohno, Yuto Miyatake, Kohei Watanabe

We have investigated programmable photonic integrated circuits (PICs) including a universal PIC for deep learning. We have fabricated a programmable Si PICs based on micro ring crossbar array and confirmed the fundamental operation of the deep learning.

Ge mid-infrared photonic integrated circuit

M. Takenaka, S. Takagi, Kasidit Toprasertpong, Chong Pei Ho, Ziqiang Zhao, Yuto Miyatake

We have also conducted the research of the mid-infrared photonic integrated circuits based on Ge-on-Insulator (GeOI) wafer fabricated by wafer bonding. By using SOG doping to form a lateral PIN junction, we have improved the modulation efficiency of a carrier-injection Ge optical modulator. We have also found that a reverse-biased Ge PIN junction enabled the detection of 2 μm-wavelength optical signal through the defect-mediated optical absorption.

2D material devices

M. Takenaka, S. Takagi, Kasidit Toprasertpong, Roda Nur, Hanzhi Tang, Xiaoxuan Zhang, Tipat Piyapatarakul

We have investigated 2D materials such as graphene and MoS2 for semiconductor devices. We have revealed that the high photo responsivity can been obtained in the MoS2 phototransistor with HfO_2 gate dielectric due to the photo-gating effect. We have also successfully evaluate the impurity concentration of MoS2 by making a thick-body MoS2 Schottky junction by exfoliation.

Mita Laboratory

(http://www.if.t.u-tokyo.ac.jp)

Current Research Projects

Programmable Matter - Study on LSI-MEMS energy-autonomous distributed microsystems for realization of deformable matter

Y. Mita, K.Misumi, N.Usami, E. Lebrasseur G. Ulliac, (LIMMS, CNRS-UTokyo IIS), J.Bourgeois, B.Piranda (FEMTO-ST, France), S. Delalande (PSA-Peugeot)

As one example of future integrated MEMS that is expected to open new research and industrial application fields, the authors are trying to show a topdown application of energy-autonomous dis-tributed microrobots. A number of identical tiny robots, sized below 1cm, will be released in an en-vironment. Individual robot can communicate with their neighbor, stick each other, and share ener-gy, to realize cooperative function. The PI is receiving a French National Research Center (ANR) grant on behalf of host professor of CNRS laboratory in the Institute of Industrial Science (LIMMS, CNRS-IIS, UMI 2820), together with FEMTO-ST Laboratory and PSA-Peu-

geot Laboratory for such “micro robots that can realize deformable substance by cooperative action, named Programmable Matter”. In year 2019, an electrostatic chucking actuator system that attaches and detaches the external skeleton of the Matter has been developed, by on tiny (1mm to 10mm) objects is performed and analyses were conducted. The actuation force has been electromagnetically analyzed. Fabrication technology of flexible electrode has been investigated in order to realize electrodes in arbitral facets of the Matter by rolling technology.

Integration of electrode devices on MEMS fluidic devices

Y. Mita,A. Higo, T.Ezawa, E.Ota, Y.Okamoto,
N.Washizu (Advantest), T.Takada (Advantest),
M. Fujiwara, T.Sawamura

Towards the goal of production of brand-new sensor devices with higher sensitivity and func-tionality, the team is working on small-gap electrode fabrication process. The target of the second year was reliable water penetration in the nanopores.

Fine Large-Area Electron Beam Lithography Exposure Methods

Y. Mita,A. Higo, M. Fujiwara, T.Sawamura,
M.Takizawa (Advantest), Y.Kudo (Advantest)

The team explores newly-acquired (in 2013) rapid electron beam writer F7000S-VD02. The ca-pability of high electron dose and sharp edge due to cell (character) projection machine configura-tion is being examined. The breakthrough in question is to extend the large-area EB lithography, whose pattern approximation have been limited to rectangular shapes, into expressing free-form smooth shapes and a number of periodical small patterns. This year’s outcome include a reliable investigation method of repetitive pattern size, pitch, and distribution through a simple optical spec-tral measurement.

University-Industry collaborative research on highly-functional system by MEMS post-process of CMOS-VLSI

Y. Mita, S. Inagaki, T. Kuriyama, Y.Sato (Nanox Japan)

The research targets are new sensor devices, made by post-process at clearnrooms such as VDEC Takeda Supercleanroom and others, of VLSI wafer made through VDEC. The important finding has been that VLSI wafer acquired just after transistor fabrication could sustain processes even with heat treatment, such as deposition, ion implantation, and drive-in. In 2016, a VLSI de-vice made on Silicon-on-Insulator (SOI) wafer was successfully Deep-RIE processed. The in-dustrial interest is its versatility – many different types of application devices, which differ one from another according to request of market, can be fabricated by using the same technology. More and more companies are interested in the scheme and are working on the technology on the col-laborative research projects. One of the research works have been awarded this year.

High-sensitive ultrasonic probe by integrated MEMS technology

Y. Mita, R.Yamaguchi, N.Usami, A.Higo,
T.Yoshimura (Osaka Prefectural University),
T.Mizuno (Konika Minolta),
K.Suzuki (Konika Minolta),
Y.Nakayama (Konika Minolta),
T.Endo (Nagoya Medical Center)

Using the same scheme as above mentioned CMOS-MEMS post process R&D scheme, this pro-ject aims at integrating piezoelectric material and MEMS post-processing to obtain a brand-new ultrasonic inspection probe, whose sensitivity is as 100 times as cutting-edge technology. In year 2019, the team was highly ranked in the evaluation from a public funding from Japan Agency of MEdical Research and Development (AMED), followed by supplemental budget that was used for design and fabrication of high-voltage electronic circuit for integration. The work has been awarded in the IEEJ 36th Sensor symposium.

LSI hot-spots active cooling system

Y. Mita, Y. Okamoto, K. Fujimoto (Titech),
H.Ryoson (Titech), and T. Oba (Titech)

A hotspot, which is referred to a high-temperature area due to the overheating of a circuit block that excess passive cooling capability, is becoming a key

limiting factor of LSI performance. An ac-tive cooling system that tries to actively remove such local heating by circulating liquid coolant is our research target. To conclude the five-year research, electroosmotic MEMS device fully inte-grated with functionalized LSI high voltage circuity has been demonstrated. To our knowledge, the highest pumping volume per driving voltage, as well as flow speed has been achieved. Using elec-troosmotic flow, an LSI component cooling (heater and sensor) has been demonstrated. An inter-esting cooling phenomenon has been found and has been analyzed.

Project PARIS: PARallel Integrated microSystem for High Frequency Action-Based Non-Invasive Multi-Modal Cell Analyses

Y.Mita, T.Tsuchiya, Y.Okamoto, A.Mizushima, E.Lebrasseur,
T.Bauvent (ENS Paris-Saclay, exchange student),
C.Moslonka (ENS Paris-Saclay, VDEC internship student), B. le Pioufle C.Moslonka (ENS Paris-Saclay), Tixier Mita Agnès (UTokyo RCAST),
Olivier Français (ESI-EE, Univ. Paris Est),
F.Marty (ESIEE, Univ. Paris Est)

Having granted again JSPS-CNRS bilateral project 2018, the team is developing a large-scale multi-modal cell analyses system (project name: PARIS). The electrorotation method, which is known to measure a mechanical rotational response to the incident rotational electrical field fre-quency is used. The method is non-invasive so the evaluated cells are possible to be used in fur-ther biological experiments. In this year fabrication of classical electrodes was first leaned by VDEC internship student. Then thicker electrodes were made in collaboration with ESIEE and ex-periments were done at ENS Paris-Saclay. LSI has been designed in order to integrate with driving electrodes..

Colloidal integrated Infrared Detector

A.Higo, N.Miyazawa, N. Usami, Y. Okamoto,
W. Haibin, N. Kubo, K. Segawa, Y. Mita

Electron devices using colloidal quantum dots are believed to open new application fields such as light emitting devices and or photovoltaics. Up to date, very few research activities have been done in sensors applications; if we can realize integrated photodiodes that have extended sensitive wavelength as long as 1.35μm-1.4μm wavelength, such devices can be used by many new appli-cations such as security cameras and / or Laser Radar (Lidar) under sunlight. The aim of this research is to find an integration method for beyond Si-LSI device. We try to integrate colloidal quantum dots of which absorption spectra can be designed through molecular design. By inte-gration, Silicon device will be able not only to capture infrared wavelength lights, which is impossi-ble by its original characteristics, but also my include information reading and computation circuits. For the first year's exploratory study, partly financed by the LIMMS internal project grant, spin coating integration method has been investigated. Root cause that prevented Electrical Quantum Efficiency has been identified to an unexpected reverse Schottky junction. Test structure was proposed and proved to be efficient to quantitatively analyze such unexpected parasitic compo-nent in the device.

Development of zero power multiple-threshold maximum acceleration sensor for cyber physical system

Y. Mita, R Ranga Reddy

VDEC is awarded a Japanese JST – Indian DST joint grant (SICORP) for cyber physical systems re-search, in cooperation with IIT Bombay campus. The team is participating the project through a Shock Resonant Spectrum (SRS) sensor, which has been a research theme of 2012-2014. A new Ph.D student from India is assigned and fabrication process was recovered. This year we have analyzed complete system to record 10-levels of maximum acceleration in MEMS device. Based on the result, we have started collaboration with India. We have hosted an internship student from IITB for two weeks, two students from IITH for three months and started device design.

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