Systems Design Lab

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附属システムデザイン研究センター
先端設計研究部門・先端デバイス研究部門
(旧VDEC)基盤設計研究部門・基盤デバイス研究部門

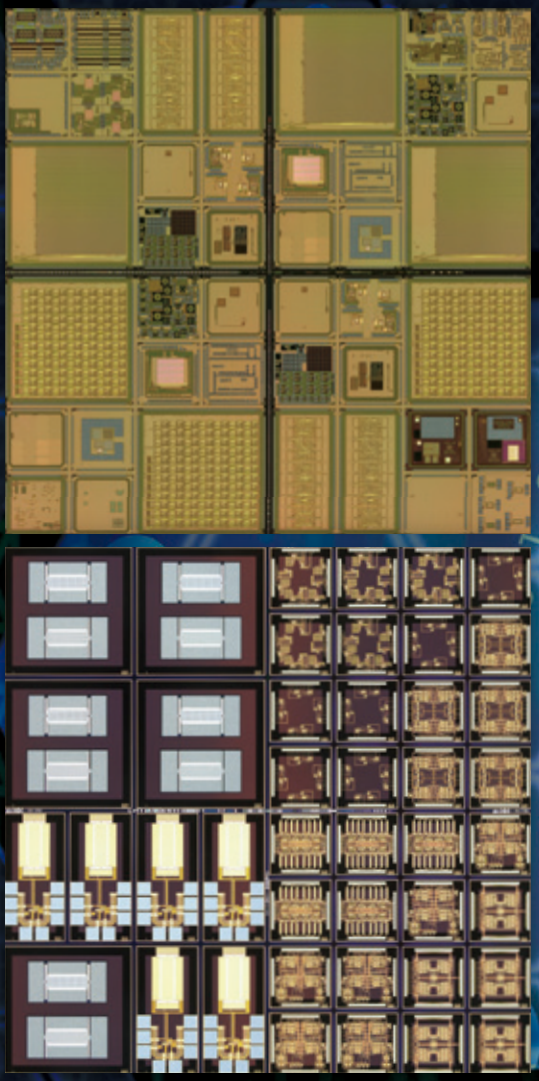
年　報

令和３年度

2021

Systems Design Lab, School of Engineering, (VLSI Design and Education Center), The University of Tokyo

Annual Report



Systems Design Lab, School of Engineering
The University of Tokyo 2021

Message from Director of d.lab

System Design Lab (d.lab) Center, School of Engineering, The University of Tokyo
Director

Tadahiro Kuroda

In Japan, semiconductors are called "the rice of industry" to indicate their necessity. But is that really the case?

Japan is able to produce 100% of the rice it consumes as a staple food. In fact, rice is the only crop for which Japan maintains self-sufficiency. However, as the diet of the Japanese people diversifies, rice consumption has been on the decline year after year. For the current consumption level, it takes only 60% of the country' s paddy fields to produce the rice needed as a staple food.

Meanwhile, Japan' s self-sufficiency rate in semiconductor production has only been falling in the last 30 years. There are predictions that at the current rate it will drop to 0% by 2030. On the other hand, semiconductor consumption has been increasing every year. The deepened recognition of the importance of digital transformation (DX) under the COVID pandemic has fueled additional growth in semiconductor demand. As a result, reports of fire, power outage, or water supply shortage at semiconductor fabs, or the fragmentation of the world' s supply chain often create considerable anxiety about semiconductor supply disruptions.

In such a current state, the expression "the rice of industry" seems to be out of step with the times. Outside of Japan, "oil" may be a better analogy for necessity than "rice." But what is emerging as the next "oil" of the world is not semiconductors but data.

So what is a more appropriate way to describe semiconductors going forward?

For me, it is "the brain cell (neuron) of society." There are three reasons.

Firstly, it is because of the shift of value from things to knowledge and information. As we transform from a capital-intensive to a knowledge-intensive society, semiconductors are assuming a more important role by changing from being a component to a means of knowledge creation and dissemination.

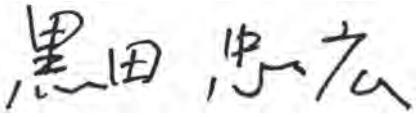
Secondly, it is because the application of semiconductors is broadening from industry to society. The infrastructure of a digital society consists of information networks for which semiconductors are indispensable.

Thirdly, it is because the semiconductor industry' s battleground is shifting from the general purpose to specialized chip market. The shift is driven by the ability of specialized chips to reduce energy consumption by orders of magnitude. The change is necessary to protect the environment given the large energy consumption required by the application of AI to big data analysis. Energy conservation is top priority for any green growth strategy.

While it is acceptable to rely on imports for "the rice of industry," a nation should be able to create its own "brain cell of society." For Japan' s Ministry of Economy, Trade and Industry (METI), digitization is not a goal to shoot for, but a necessary condition for Japan' s future. As a result, it is formulating policies with the digital industry, digital infrastructure, and semiconductor industry as the country' s three core pillars.

US President Biden recently talked passionately about the importance of semiconductors while holding a chip in his hand. Meanwhile in Japan, the ruling Liberal Democratic Party is launching a caucus of lawmakers to discuss the future of the country' s semiconductor industry under the belief that whoever controls semiconductors controls the world.

Iron was once considered to be what makes a country. Will silicon become what makes a country in the future?



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C O N T E N T S

Chapter1 Introduction to d.lab

The VLSI Design and Education Center (VDEC) was established at the University of Tokyo in 1996. At the time of its founding, Japan's semiconductor industry held a 50% share of the USD 50-billion global market, and engineers who could hit the ground running were in high demand. VDEC has since provided unparalleled, outstanding education to develop many high-caliber engineers for the semiconductor industry.

However, have these graduates of VDEC been able to fully realize their potential? In the last quarter century, even though the global semiconductor market enjoyed a rapid 7% annual growth rate, Japan's share continued to shrink, falling to the current level of about 10% of a market that is now approaching USD 500 billion.

The current semiconductor business is one of mass production of high volume, low margin general purpose chips. General purpose chips have been able to achieve large volumes because of the wide adoption of the von Neumann computer architecture constructed with the combination of memory and processor chips. While Japan led the world in memory device innovation, it lost the business competition on capital investment.

The mass production, mass consumption model has its limits. Because of the excessive burdens it places on the environment, the world is now facing an energy crisis. The recent trend of applying AI to big data analysis is fueling further growth in energy consumption.

In the middle of this development, a game changer has emerged. Recognizing that it is hard to compete by using general purpose chips procured from semiconductor makers, technology giants including GAFA have started to develop their own specialized logic chips in-house.

In response to this paradigm shift, the University of Tokyo established the Systems Design Lab (d.lab) in October of 2019 and formed a strategic alliance with TSMC a month later. d.lab was formed by establishing the Advanced Design Research Division and the Advanced Device Research Division and adding them to the existing Platform Design Research Division and Platform Device Research Division which had been operating VDEC and the Takeda Clean Room. Subsequently in October of 2020, d.lab started an industrial partnership program which has grown to include more than 40 corporate members.

Furthermore, the Research Association for Advanced Systems (RaaS) was founded in August of 2020 to lay out the framework for the university to collaborate with both the industry and the government. Using d.lab and RaaS to realize a two-pronged strategy of open and closed collaboration respectively, the university is actively promoting cooperation between academia and society as well as collaborative creation with industry. Our research aims to boost the time-performance of semiconductors, with target goals of 10x increase in both energy and development efficiencies.

Japan is aiming to transition from the current industrial/information society to Society 5.0, a human-centric society where knowledge is value. In this knowledge-based society, semiconductors will evolve from being a necessity of industry to the brain cell of society.

What strategy should the semiconductor industry pursue to address this evolution? It is d.lab's mission to find the answer.

Chapter2 Activity Report of d.lab

2.1 Advanced Design Research Division

2.1.1 Division Overview

The Advanced Design Research Division faculty consists of four professors, one associate professor, one lecturer, one project professor, and one senior fellow (joint-appointment included). Its goal is to enable the design of integrated circuits with both high energy efficiency and high design efficiency. In addition to its research effort, it has two organizational responsibilities. First, it operates the d.lab Partnership Program with help from other d.lab divisions. Second, it founded and operates the Research Association for Advanced Systems. The following section is the FY2020 report on these two operations.

2.1.2. d.lab Partnership Program Activities

The d.lab Partnership Program was launched to establish an international center of knowledge-value where system designers and members of the semiconductor industry meet to exchange information and ideas and to engage in open discussion of collaboration between academia and society. The Program aims to create a hub that brings together ideas from system designers in industries including IoT, AI, 5G, automated driving, and healthcare, advanced semiconductor technologies such as advanced CMOS processes and 3D integration technologies, as well as enablers of such technologies including materials and manufacturing equipment. For FY2020, the Program started recruiting members in July and was able to achieve a membership of 21 corporations. Table 2.1.1 contains the list of FY2020 corporate members. We would like to thank these members again for their participation.

In our original vision for the Program, we planned to not only create a platform for the dissemination of the research accomplishment of d.lab, but also to turn our Mejirodai campus into a new venue for interaction and learning. We planned to host various events to enable Program members to interact with renowned professors and students of the University of Tokyo, with universities and research organizations from around the world, and with other industrial executives and leaders, as well as events to share information and knowledge from international conferences and introduce and assess the most advanced technologies from the likes of TSMC. Unfortunately, because of COIVD-19, we were forced to center our activities around seminars which could be held in the form of webinars. Below is a summary of our activities in FY2020.

Because we started the membership drive for FY2020 late, our activities were limited to the second half of the year from last October to March of this year. Table 2.1.2 lists the seminars we organized in FY2020. Particularly worth mentioning is the inaugural seminar held on Oct 28, 2020. In that seminar Professor Tadahiro Kuroda, Director of d.lab, discussed the new strategy for the semiconductor industry. He explained how the international and societal state of affairs as well as geopolitical factors are driving further growth in the already rising dependence of every application on semiconductors. The focus of his discussion was on how Japan could thrive under such an environment.

On Nov 11, we held a briefing on the 2020 International Conference on Solid State Devices and Materials (SSDM2020). Professor Ken Uchida, Program Committee Chair of this long-running conference, led an analysis of the future trends in semiconductor device and material technologies. Because materials have the potential to help the industry overcome the limits faced by Moore's Law, the analysis focused on the possibility, through the search for new materials, of discovering the technology that will take us to the next century.

On Nov 28, we held a discussion of TSMC's technology. We welcomed President Onodera, Mr. Alex Hsiao, and Mr. Masahiro Koike from TSMC Japan on live stage to provide an introduction of TSMC's latest technologies, which was followed by a Q&A session. Because of TSMC's leading role in advanced semiconductor technology development, it was an invaluable experience to be able to hear directly from key members of the company the latest development trends.

On Dec 25, we held a briefing on the 66th IEEE International Electron Devices Meeting (IEDM2020). IEDM is the world's preeminent conference on device technolo-

gy. In this briefing, professors from d.lab analyzed papers from the conference and elaborated on various topics including More Moore and More than Moore technology trends, emerging devices such as those based on quantum effects, as well as co-design of device and circuit to meet the needs of novel computing, Their presentations were delivered in an easy-to-understand manner for even non-experts in the field.

Soon after the New Year on Jan 13, we organized an IBM Day with the theme "Thinking about Quantum Computing." We invited speakers from IBM which has already launched a quantum computing business. Together with Associate Professor Shuntaro Takeda from the Graduate School of Engineering at the University of Tokyo, they presented on the current state of quantum computing technology and its future outlook. It was a balanced presentation, with Professor Takeda providing an easy-to-understand explanation of quantum computing technology, followed by the IBM speakers elaborating on its practical application.

The FY2020 seminar series closed with a briefing on the 2021 International Solid-State Circuits Conference (ISSCC2021). The world's preeminent conference on integrated circuits technology was held in February. Professors from d.lab, led by Professor Makoto Ikeda who served as ISSCC2021's Technical Program Committee Chair, explained the latest trends seen in the conference including the flourishing of machine learning processor development, ICs that enable novel computing exemplified by quantum computers, as well as ICs for 5G, AI, and game consoles which will drive the future semiconductor market. In addition to providing a summary of the papers, the speakers also positioned them within the context of the technology trends in their respective disciplines to make it easy for even non-experts to understand.

Unfortunately, it appears that we will have to continue to focus on remote seminars in FY2021. Nevertheless, we are considering adding something new by planning networking events for intellectual exchange between members and the university as well as among members of the Program.

2.1.3. Research Association for Advanced Systems Activities

We started preparation in FY2019 and launched the Research Association for Advanced Systems (RaaS) on Aug 17, 2020. The founding members are the University of Tokyo, Toppan, Panasonic, Hitachi, and MIRISE Technologies. It is the goal of RaaS to create a design platform for the specialized chips required to enable a data-driven society. It aims to increase 10-fold the development efficiency of such specialized chips by adopting open architecture in the design platform. Furthermore, through the research and development of 3D integration technology for stacking in the same package multiple chips made with the latest 7nm CMOS process, it strives to achieve a 10-fold increase in energy efficiency.

We believe that leading semiconductor businesses are transitioning back from general purpose to specialized chips. This is being driven by the unique energy crisis faced by a data society. The energy crisis is spurred by the explosive growth in data volume and the increasing sophistication of AI processing. At the current pace, IT equipment alone is projected to consume almost two times the total power consumption of today by the year 2030, increasing to 200 times by the year 2050. We cannot really hope for a sustainable future if digital transformation consumes so much energy as to destroy the environment.

Under such a condition, only those who can increase energy efficiency 10-fold can boost computer performance 10-fold, or extend smartphone battery life 10-fold. Compared to general purpose chips which can be used for any task, specialized chips achieve orders-of-magnitude better energy efficiency by eliminating superfluous circuits. That is why specialized chips are in demand. Meanwhile, since the neural networks used for AI processing process data in parallel, they cannot be efficiently implemented using the von Neumann architecture which processes data sequentially. As a result, specialized chips are being developed all over the world to serve as AI accelerators. Furthermore, the slowing of Moore's Law is providing another favorable condition for the rise of specialized chips.

Unfortunately, specialized chips development is not for everyone. The number of transistors integrated on a chip has exceeded the world's population. IC development has seen its cost dramatically increase in recent years, reaching 100 million dollars. Even with a team of several hundred designers, it can take several years to develop a chip. It is an unacceptably long turnaround time given how fast technology advances nowadays.

With software, even if there is a bug, it can be patched later after the software's release. In contrast, hardware must be bug-free before it is released. Hardware development is indeed "hard" since the design is more difficult and the risk higher than software.

Software development has been aided by the use of compilers. If a similar technology, in other words a silicon compiler, is available to hardware development, it should be possible to reduce its cost and lower its risk. Furthermore, it will expand the pool of hardware designers. Eventually, with the open source culture taking roots, and the expansion of the hardware ecosystem network across its hierarchy, we expect to see the rise of mass collaboration, and we will be able to develop chips the way software is written.

Alan Kay once said, "People who are really serious about software should make their own hardware." System development requires both hardware and software development.

Our goal is to democratize access to silicon technology. To that end, we will innovate on silicon compiler technology to enable designing chips like writing software and create a platform for quick prototype development (agile authentic prototyping).

Our technology target is 10-fold increase in both development and energy efficiency. We will create an agile design platform and adopt open architecture to improve development efficiency. At the same time, we will employ the most advanced CMOS manufacturing technology and 3D integration to boost energy efficiency.

We believe that semiconductors should be provided as a service instead of being sold as a product. The mission of RaaS is to research and develop the necessary technologies.

We had planned to have researchers from member companies to conduct research at our Mejirodai International Village location so as to create an environment that stimulates cross-pollination. Unfortunately, we had to change that plan too into one centered around remote work. Our most significant accomplishment of the year was to put in place the environment for prototype design using the most advanced CMOS technology which included closing use agreements with foundry and CAD vendors and acquiring hardware tools for the design work.

Table 2.1.1 List of FY2020 d.lab Partnership Program Members

Cadence Design Systems, Japan
Dai Nippon Printing Co., Ltd.
Daikin Industries, Ltd.
FUJIFILM Corporation
Fujitsu Ltd.
Hitachi, Ltd.
JSR Corporation
KIOXIA Corporation
MIRISE Technologies Corporation
Mitsubishi Chemical Corporation
Nihon Synopsys G.K.
NIKON CORPORATION
Panasonic Corporation
ROHM Co., Ltd.
Semiconductor Energy Laboratory Co., Ltd.
Shin-Etsu Chemical Co., Ltd.
Sony Corporation
Sumitomo Corporation
Tokyo Electron Ltd.
TOKYO OHKA KOGYO CO., LTD.
Toppan Printing CO., LTD.

Table 2.1.2 List of FY2020 d.lab Partnership Program Seminars

Date	Title	Presenter(s)
10/28/2020	d.lab Partnership Program Kickoff Meeting	Prof. Tadahiro Kuroda, d.lab
11/11/2020	SSDM Report	Prof. Ken Uchida, d.lab Prof. Toshiro Hiramoto, d.lab Prof. Tadahiro Kuroda, d.lab Masaaki Niwa, Senior Fellow, d.lab
11/25/2020	TSMC Day -TSMC Technology Chat	Mr. Makoto Onodera, TSMC Japan Mr. Masahiro Koike, TSMC Japan Mr. Alex Hsiao, TSMC Japan
12/25/2020	IEDM2020 Report - Unraveling IEDM	Prof. Shinichi Takagi, d.lab Prof. Ken Takeuchi, d.lab Prof. Ken Uchida, d.lab Takeshi Takagi, Principal Researcher, d.lab
1/13/2021	IBM Day - Thinking About Quantum Computing	Shuntaro Takeda, Associate Professor, Graduate School of Engineering Mr. Roh Mitsuhashi, IBM Mr. Shintaro Yamamichi, IBM
3/3/2021	ISSCC Report	Prof. Makoto Ikeda, d.lab Prof. Ken Takeuchi, d.lab Tetsuya Iizuka, Associate Professor, d.lab Atsutake Kosuge, Lecturer, d.lab Mototsugu Hamada, Project Professor, d.lab

2.2 Advanced Device Research Division

Advanced Device Research Division is working for the development of three-dimensional (3D) integration technology and advanced device technology aiming at ten times higher energy efficiency of semiconductor systems in the data-driven systems.

In 2020, we discussed the launch of a new project of the next-generation 3D integration technology. Recently, the computing technology for processing large amount of data is becoming more important and the energy consumption by frequent data transfer between memories and processors is a severe problem. To solve this problem, the direct bonding 3D stack technology, where the data transfer distance is shortened by direct bonding of chips or wafers, has attracted much attention. One of the examples is the hybrid bonding technology that enables WoW (Wafer on Wafer), where same kinds of wafers such as memories are multiply stacked, and CoW (Chip on Wafer), where multiple chips with different sizes, types, or nodes are stacked in a 3D manner. We are at a major turning point from package-level 3D integration with micro-bump connections to direct bonding 3D integration based on bumpless direct bonding technology. We are planning to propose a new project of solving main technological challenges of hybrid bonding by excellent original technologies in Japan and apply for the national project.

2.3 Platform Design Research Division (VDEC Function) FY 2020 Report and FY 2021 plan

2-3.1 Overview of Platform Design Research Division

Since its establishment in 1996, the VLSI Design and Education Center (VDEC) at the University of Tokyo has been developing projects that contribute to integrated circuit design education at universities and technical colleges in Japan, based on the three major roles: ”spreading the latest information on VLSI design and education,” ”providing licenses of CAD tools,” and ”supporting on VLSI chip fabrications for academic use.” On October 1, 2019, VDEC has been re-organized into Systems Design Lab (d.lab), Graduate School of Engineering, the University of Tokyo as part of an organizational restructuring aimed at strengthening integrated circuit related activities in the University of Tokyo's semiconductor integrated circuit-related activities. The Platform Design Research Division of d.lab continues to carry out the functions of the VDEC and continues “VDEC activities” seamlessly. Here, the outline of “VDEC activities” of the FY2020 is reported below.

The missions of VDEC are for advancement of researches and education on LSI design in public and private universities and colleges in Japan and send many distinguished VLSI designers into industry. After 25 years of VDEC establishment, educations on CAD software, LSI design and design flow in universities have been well established. On the other hand, advancement on nano-meter CMOS technologies forces design flow and CAD software complicated. We have been continuing CAD tool seminar by the lecturers from EDA vendors for twice a year. We hold the seminar in VDEC and provide distance learning through video streaming. We expect spread of the up-to-date LSI design methodology by using CAD tools.

In order to make it more convenient for the participants, the seminars have been held only in Tokyo since 2009, and at the same time, the seminars have been broadcasted to individual participating lab. The VDEC expects that the latest CAD use-case will be shared among labs through the seminar organized by VDEC, and will be a trigger to spread the technology nationwide. In FY2020, all seminars will be conducted online. Some items were conducted in the form of on-demand plus live Q&A sessions to improve the convenience of participation. In addition, in view of the current situation where the tool-chains of various companies are becoming more complex and it is difficult to fully use the introduced tools, lectures on the tool-chains recommended by each tool vendor were also held in conjunction with the individual tool seminars. From the end of FY2019, we received permission from each EDA vendor to use EDA tools from home, to avoid delay&slowdown in integrated circuit design research and education in Japan.

2-3.2 Status of Education at Platform Design Research Division

The LSI Design Flow Seminar is designed to educate the basic concepts of LSI design and to provide hands-on experience of practical design examples using multiple CAD tools. For this purpose, VDEC has been organizing LSI design education seminars as well as “Refresh Seminar” for re-education programs for engineers. “Analog Design Course”, “RF Design Course,” and “MEMS Design Course,” which started in 2012, were held from June to September. All of these courses are experiential education courses with exercises, and experienced instructors from major universities are invited as lecturers. In addition, “Transistor Level Design in VDEC Environment (Course VT)” and “Digital Design Methodology in VDEC EDA Environment (Course VD Course VT)” and “VDEC Digital Design Methodology Course (Course VD)” are conducted for designers in universities. The “Refresh Seminar” are all held online in FY2020, and as a result, the number of participants has increased compared to previous years.

In addition to these seminars, VDEC holds the “VDEC Designers’ Forum” once a year, mainly for young faculty members and students. This is a workshop-style meeting, where participants bring their design cases and exchange their successes and failures, in addition to invited lectures from companies and universities. In FY2020, the VDEC Designer Forum had been held online. Since FY2011, the “IEEE SSCS Japan Chapter VDEC Design Award” has been presented as an award for VDEC activities. The final judging and awarding of the “IEEE SSCS Japan Chapter

VDEC Design Award" has been held at VDEC Designers' Forum since 2011, and in 2020, the IEEE SSCS Japan Chapter VDEC Design Award will be presented to Mr. Koki Ishida of Kyushu University. Three VDEC Design Award Excellence Awards, (Mr. Koki Ishida (Kyushu University), Mr.Naoki Ojima(The University of Tokyo), and Mr. Masaru Osada(The University of Tokyo)), and two VDEC Design Award Encouragement Prizes (Mr. Kentaro Nagai(Kyoto University), Mr. Kenji Sugie(Nara Institute of Science and Technology)), and five VDEC Design Award Commendation Prizes for Idea Contest (Dr. Junichiro Kadomoto(The University of Tokyo), Mr. Ryuki Shigemasu (Shizuoka University), Mr. Takuya Murakami(Nagoya University), Mr. Kosuke Fukumitsu(Kyushu University), and Mr.Tatsuya Nomura(Shizuoka University).

Although the educational system through such seminars and forums has enabled students to learn the basics of LSI design, they still face various difficulties in actual LSI design situations. For beginners, setting up the CAD software is the biggest problem. Even after setting up the software, they are often baffled by the "difficult error messages" issued by the CAD software. VDEC users can register for the "CAD mail group" and the "Prototyping Technology User Group" on the VDEC website, where they can post their questions and ask for help. The registered users of the mail groups are not obligated to respond, but in most cases they can get help from experienced users within a few hours or days. We hope that you will take advantage of this system to help solve your problems.

2-3.3 Publications related to Platform Design Research Division

Figure 2.1 shows the trend of number of papers through VDEC activities. Figure 2.2 show the number of papers related to VDEC facilities. It can be confirmed that CAD software is widely used in writing papers. Since CAD software is often used not only in chip design but also in the preparation stage of chip prototyping, its contribution as a tool to demonstrate the basic idea of the research is also significant.

2-3.4 Report on AI Chip Design Center

VDEC and the AIST have been jointly commissioned by NEDO to develop a common platform technology for accelerating AI chip development under the "Innovation

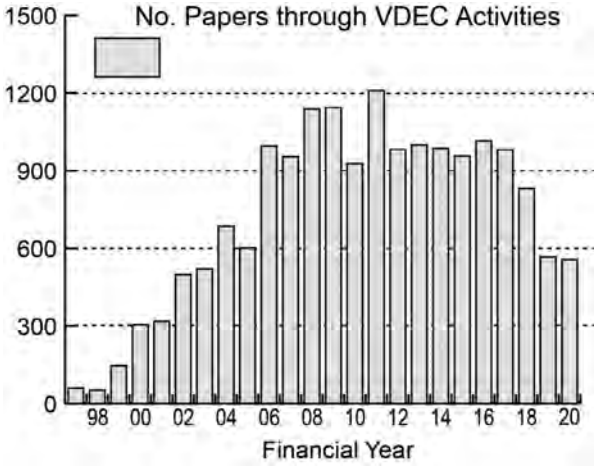

Fig. 2.1 Trends of number of papers through VDEC activities.

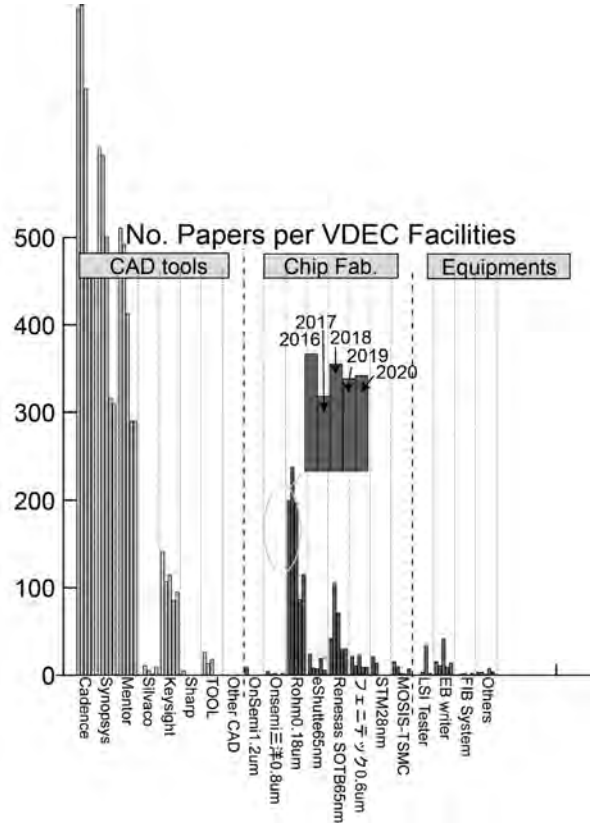

Fig. 2.2 Number of papers related to VDEC facilities.

Promotion Project for Accelerating AI Chip Development / R&D Item 2: Development of Common Platform Technology for Accelerating AI Chip Development" since 2018. In this project, we have established an EDA utilization and design environment for venture companies and small and medium-sized enterprises(SMEs) in Japan, and are working as an "AI chip design center(AIDC)". In this activity, in addition to the introduction of EDA tool licenses that allow venture companies and small and medium-sized companies to prototype up to engineering samples, we have introduced IP for 40nm and 28nm, and are also providing a large-scale, high-speed design and verification environment using a hardware emulator, which was introduced with a subsidy from the Ministry of Economy, Trade and Industry at the start of this project. In FY2020, we have designed a SoC platform with NoC, PCIe, DDR4, etc., and multiple functional IP cores, and taped out the platform as a SoC with multiple AI IP cores designed by multiple users. In order to further strengthen this activity, we are accelerating our research by establishing the "AIST-The University of Tokyo AI Chip Design Open Innovation Laboratory" (AIDL) in the Takeda Building, Asano Campus, The University of Tokyo on September 1, 2019.

2-3.5 Plan for FY 2021 "VDEC Activities" of Platform Design Research Division

In FY2021, we will continue the VDEC Activities for academics as before.

【Design related information dispatching/Seminar】

We will continue holding the following seminars: (1) CAD tools seminars which have been continued since 1997, (2) "Refresh seminar" since 1998, (3) "Designer' Forum" since 1997. We will also continue seminars for LSI tester usage at VDEC and sub-centers, workshops on LSI testing technologies initiated by D2T.

【CAD tool support】

We will continue Cadence tools, Synopsys tools and Mentor tools as the main stream design tools. We will continue analog RF design environment, GoldenGate and ADS by Agilent, C-based design environment, BachC by Sharp. In addition, we continue trial of several CAD tools, such as layout platform, Lavis by TOOL. Design debugging platform from SpringSoft has merged into Cadence tools and will be continued.

【Chip fabrication services】

We will continue chip fabrication services for 0.18μm CMOS by Rohm and 0.8μm CMOS by On-semiconductor-Sanyo as the regular services. Chip fabrication services for SOTB 65nm CMOS by Renesas Electronics will be terminated.

In addition to the above. We will continue to develop an "AIDC" activities, in collaboration with AIST. We will introduce a logic emulator for large-scale AI digital chip design verification, and maintain and operate EDA licenses for industrial applications. The main objective of this project is to provide small and medium-sized venture companies with a development environment for AI chip design, evaluation, and verification in order to accelerate the development of AI chips, but we also plan to improve the environment for use by universities in order to promote university-originated companies in the field of AI-related integrated circuits.

Table 2.1 Chip fabrication schedule

【CMOS 1.2μm 2P2M】 On-Semiconductor(Former Motorola Japan)

	Chip application deadline	Design deadline	Chip delivery
2021#1	2021/7/5	2021/9/27	2021/12/20
2021#2	2022/1/11	2022/3/28	2022/6/27

【CMOS 0.18μm 1P5M(+MiM)】 Rohm

	Chip application deadline	Design deadline	Chip delivery
2021 #1	2021/4/5	2021/6/28	2021/10/15
2021 #2	2021/6/14	2021/9/6	2021/12/24
2021 #3	2021/8/4	2021/10/27	2022/2/13
2021 #4	2021/12/6	2022/2/28	2022/6/17

【SOTB CMOS 65nm】

	Chip application deadline	Design deadline	Chip delivery
2021 #1	2021/6/14	2021/7/26	2022/1/22
2021 #2	2022/1/24	2022/3/7	2022/8/27

2.4 Platform Device Research Division

2.4.1 Mission

D.lab platform device research division aims at providing every researcher with three essential elements for research on new devices. The division is with around 20 staffs, powered by Dr. Yoshio Mita, the playing division director who himself actively performs experiments in the Cleanroom as a leading researcher, and operated in collaboration with related departments (such as Institute of Engineering Innovation, Electrical Engineering and Information Systems, and Mechanical Engineering) in terms of human and budget resources. Research in emerging fields of semiconductor electronics devices (such as integrated circuits), sensors and microsystems requires three essential elements: (1) fabrication machines with stupendous amount of budget, (2) rich accumulation of fabrication technology knowledges, and (3) research capability to develop new technologies required for new devices. In Japan, these three elements had been prepared and kept in an individual research group until the end of 20th century. However, due to the technology trends towards advanced fabrication over larger-scale wafers, it has become almost impossible for a research group to purchase and maintain the cutting-edge fabrication machine line, in the 21st century. Originally, it was impossible for every research group in universities, companies, research institutes, and NPOs, to individually "own" such large-scale facility and necessary budget by themselves; If researchers wish to "cooperate" with the other researchers in a platform, which is equally open to everybody, they can "effectively own" the most advanced "open platform", and thereby the cutting-edge research activities can be held anywhere in Japan. This is the principle of d.lab's open device platform, which is in fact a lateral expansion of "shared economy model in VLSI design and fabrication" to micro-nano fabrication and measurement research field, originally established by VDEC for Japan in 1996.

Towards that end, d.lab Platform Device Research Division takes full advantages of spaces (of its own and of open rental) in Takeda Sentanchi Building. The building was inaugurated in December 2003, thanks to the enormous donation in 2001 from Mr. Ikuo Takeda (founder of Advantest) to the faculty of engineering (Dean was Professor Hiroshi Komiyama) as well as VDEC (director was Professor Kunihiro Asada). In the building, a 600m^2-square supercleanroom including "official ISO3 (a.k.a. federal class 1. Once measured as ISO1)" area (Fig.1). The cleanroom and affiliated experimental rooms are equipped with cutting-edge nanofabrication and measurement machines,

Fig2.4.1 Development of Takeda Sentanchi Supercleanroom

Fig.2.4.2 List of equipment under d.lab Platform Device Research Division

total valued over 3.6 billion yens (30M euros). The users can openly use such nice machines really inexpensively.

Over 70 apparatuses are openly accessible (Fig.2), including, "world's fastest" large-area direct electron beam (EB) writing machine Advantest F5112+VD01, which has been donated according to the wise decision of Mr Oura, a chairman of Advantest, fine EB writer Advantest F7000S-VD02 and Silicon Deep Reactive Ion Etching machine SPTS MUC-21 ASE-Pegasus, both purchased by Japanese government's supplemental budget (known as Abenomics, the first arrow), and the scanning electron microscope (SEM) Hitachi Regulus SU8230 that provides highest-class resolution among those obtainable by research laboratory. The machines can cover most of the research steps in nanotechnology, which are cleaning, film deposition, lithography, etching, packaging and characterization. Not all apparatuses are yet installed in Takeda Building, however due to nationwide platform network, researchers can access in another equivalent nanofabrication platform center(s).

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2.4.2 "Takeda Sentanchi Supercleanroom" cooperation platform

The platform is called "Nanotechnology Platform UTokyo Nanofabrication site" according to the MEXT's national project, or simply "Takeda Sentanchi Cleanroom" (in short, Takeda CR). The platform is widely open to those who share the "value of cooperation". The most important understanding for every user is the platform must not be considered as a simple outsourcing agent; being understood the value of "own help, mutual help, and public help", the participant can drastically minimize costs (personnel, budget, and time), which should have otherwise been totally covered by each researcher, and can directly jump into advanced research. Key Performance Indicators of such benefits are as follows: over 7.5 billion yens for installation cost of building and equipment, over 260 million yens for yearly operating cost, and reduction of over 20 years' leading time to acquire know-hows in advanced fabrications. These benefits have attracted many research groups. Since ten years, the number of research groups who sent us the letter of consensus exceeded 420. Over 750 members are yearly subscribed (including renewal and new subscription). In year 2020, over 500 persons have used cleanroom and their total access count exceeds 15,000.

Operation principle is also "own help, public help, and mutual help". Budgetwise, each term of the principle corresponds to: (1) User's payment to participate budget acquisition (charged according to the officially-approved d.lab's internal rule), and (2) national budget allocated to d.lab platform research division, MEXT Nanotechnology Platform project, and (3) major laboratories (who rent space in Takeda Building for their research work) as well as research projects with d.lab operation laboratories (such as Mita Lab). Of course, each budget category is righteously dispensed in perfectly following its own rule defined by corresponding laws and ordinances. The yearly operation cost of 260 million yens are composed of equipment installation, electricity and water fees, maintenance, and personnel. National Universities have acquired budget flexibility since the date of private agency statuses. It helps a lot to ensure staff employment as well as small to middle sized equipment acquisition.

Platform Device Research Division staffs acquire implicit information for future fabrication technologies, due to daily help to massively parallel research projects. The team develops technologies with high demand and universality and make them accessible by publishing papers. As the most recent example of successful application to multiple research domains, we have developed a platform technology of nano pores (a couple of hundreds of microns) on an alumina(γ-Al^2O^3)membrane. The technology was initially developed for "bio measurement device" through d.lab PDRD's collaborative research project with

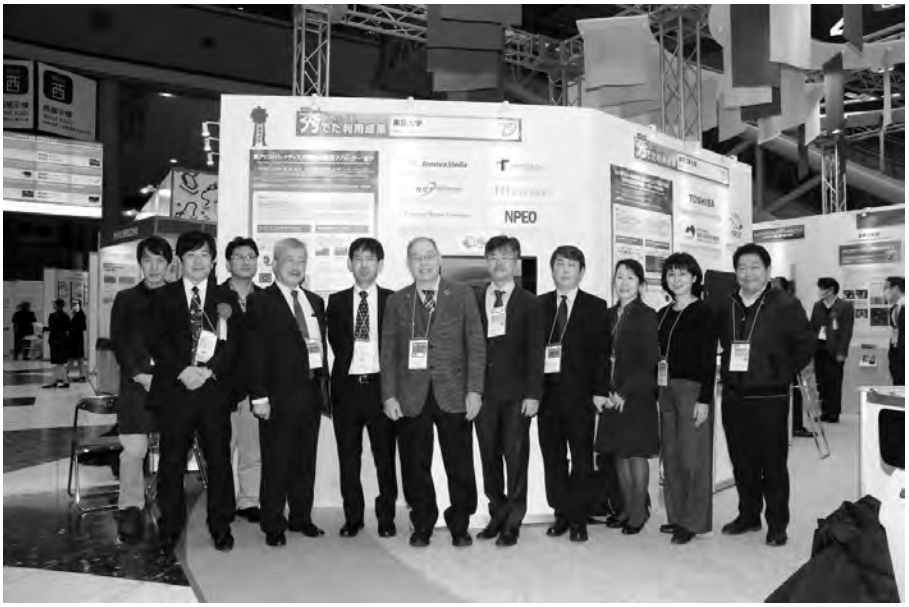


Fig.2.4.3 Group photo after award ceremony

a company; then through conversation at Takeda's cloth changing room, the same fabrication process was found to be best for a completely different device application: circular-polarized deep ultraviolet light generating membrane [1].

[1] K. Konishi et al., Optica, 7, No. 8, pp. 855-863 (2020) DOI:10.1364/OPTICA.393816

Moreover, taking full advantage that PDRD is a division of d.lab, the team has been developed for over 10 year, a reliable research scheme for integration of LSI and MEMS devices, known as "Integrated MEMS research domain". As summarized in a peer-reviewed journal [2], through VDEC function of d.lab "LSI foundry", a specific LSI circuit silicon wafers are fabricated through company (such as Phenitec Semiconductor). Then the wafer is "post"-processed in an open nanofabrication platform including Takeda Sentanchi Supercleanroom. The critical advantage of such scheme is that researchers can "easily" obtain silicon wafers with transistor circuits, which has been really difficult for university cleanrooms to acquire reliability, and can fabricate by themselves specific MEMS that no foundry company can provide. Namely, researchers can produce "World's first functionality" with "World's highest quality". Such a flexible scheme is unique in the world. Yearly one multi-chip fabrication is performed (pre-fixed participants upon request), including collaborative research works with industries.

[2] Y. Mita et al., Japanese Journal of Applied Physics, 56, p. 06GA03, 2017 (2017) DOI: 10.7567/JJAP.56.06GA03

2.4.3 Activity Report 2020 of Platform Device Research Division

【Prize】The MEXT Nanotechnology Platform Project gives prizes for good usage of platform. Every year, several projects are selected by specialists' award committee, among solicited candidates selected from over 3000 research project reports. Among the projects that PDRD have solicited, we won the 1st prize "Best use award" on "Nanoheater® device for thermally-assisted hard drive" (Fig.3). Note that our division has been awarded consecutively for two years. The awarded group are Nanophotonics Engineering Organization (NPEO), Innovastella corporation, three universities (Toyohashi Institute of Technology, Fukuoka Institute of Technology, and Carnegie-Mellon University), and a national research institute (NIST). The research topic was ring LASER and integrated nanoscale needle in order to drastically reduce power for hard drive by using near-field optics.

【Function authorization】The MEXT Nanotechnology platform project also authorizes Function for highly-skilled engineers. In year 2020, d.lab PDRD recommended Mr. Makoto Fujiwara and Mrs. Etsuko Ota. They were acknowledged as "Expert". Accordingly, all the PDRD forward engineers (Sawamura, Mizushima, Lebrasseur, Fujiwara, and Ota) are acknowledged as "Expert". The engineer with such grade is known to be capable of not only helping users but also are capable of developing new technologies. Such highly-skilled engineers are rare in Japan: During years Heisei 27 to 30, only 28 out of 166 acknowledged (three levels) engineers has got "Expert". Thereby, the PDR division is externally acknowledged as skillful nanotechnology expert laboratory.

【Impartial anti-Pandemic measure】Due to the COVID-19 pandemic, cleanroom has been under shut-down sequence since 7/Apr/2020, and completely locked down since 16/Apr, which was the day of "State of emergency for entire Japan". During three month's lock down period, the team has intentionally considered how to prevent mutual infection despite massive use of cleanroom. The resulted procedure has been accepted by the Faculty's task force. After reopening, the team strictly follow the UTokyo's alert level and perform corresponding measure. The principle is in two levels: those who are allowed by responsible to come for operation are one-by-one checked and granted for use. Those who cannot come due to the reasons such as prohibition of their origin entity have also helped by PDRD's engineers and professors' proxy use.

【No infection case & no decrease in platform uses】As a result, zero infection case as well as zero mutual infection has been obtained. The users' participation (fee) summed up to around 80 million yens, which has been smaller than the year 2019 (around 100M) but was equivalent to the year 2018. Taking three month's lockdown, the use has

was proven to be increased. Also, the number of "Nanotechnology platform use report" for 2020 was 164, which was even more than that of the year 2019 (158 reports). As the dean of Faculty of Engineering Prof. Takao Someya stated, we continuously try to "asymptote the risk down to zero%, and asymptote the research activity up to 100%". Towards that goal, every division of the faculty has been asked to try whatever popssible measures. D.lab PDRD is proud of the achievement of satisfactory results. The achievement is due to the system that has been carefully considered both users' expediency and safety; above all, the division chief would like to express his sincere thanks to each division staffs who worked enormously as an "Essential Worker".

【Granted to Supplemental Government Budge】 While wishing the pandemic end as early as possible, the PDRD was aware of importance of turning the cleanroom into "Cyber Physical" one, for the continuous use of cleanroom in case of future disasters. In year 2020, Japanese government has opened a call for supplemental budget to make research laboratories automatic and remote operation; d.lab PDRD proposed a project of "Cybe Physical Cleanroom". The project has been selected by UTokyo internal competition, and the direction asked d.lab PDRD to be a leading laboratory to create a proposal to MEXT in combining with Nano Measurement Centre and UTokyo museum's projects. The UTokyo project has won 4th place out of 91 universities projects. Due to the budget, all cleanroom machines that are controlled by PCs and workstations have been connected to a secure internet system. Now the engineers (as well as users) can handle all keyboard, mouse, and video functions from outside of cleanroom, while perfectly keeping information security. The machine is already in operation, and many projects take advantage for inside-outside cleanroom connection projects as well as remote troubleshooting.

【Granted to Post-Nanotech platform national project】The major part of "public" help for cleanroom has been covered by MEXT Nanotechnology platform. Nanotechnology platform project will end his period at the end of financial year Reiwa 3rd (31/Mar/2022); MEXT has started another national project, by officially stating "use heritage of nanotech platform", for digital transformation (DX) in materials including MEMS devices. The name of the new project is called "Material DX". Structurally speaking, material DX have adopted "research domain hub-and-spoke" system, in contrast with Nanoplat's "technology domain system" composed of characterization, nanofabrication, and material syntheses.

d.lab PDRD has been merged with Nano Engineering Center of Institute of Engineering Innovation and Information Technology Center to form a strong hub team, under presidency of Professor Yuichi Ikuhara. The team has been highly appreciated by the evaluation committee and was granted for 10-year project's "hub" site. Indeed, d.lab PDRD had been with Nano Engineering Center for the Nanotechnology Network project (2007-2012), which is in fact a precedent project of nanotechnology platform. Also, Nano engineering center is offering cleanroom infrastructure operation (through Cleanroom Operation Room, Room 311 of Takeda Building). Therefore we are sure for future successful cooperation of the new Material DX project. To begin with, MEXT has granted us a big (>100M yens) supplemental budget for our proposal to enhance performance of our cleanroom that will take place at mid-FY2021.

2.5 Activity Report of ADVANTEST D2T Research Department

2.5.1 Introduction of ADVANTEST D2T Research Department

2.5.1.1 Aim of establishing ADVANTEST D2T Department

ADVANTEST D2T research division was established in VDEC in October 2007. As the name suggests, it is financially supported by ADVANTEST Corporation.

The aim of establishing ADVANTEST D2T research division was to promote the research and education environment with regard to VLSI testing in all universities and colleges in Japan. “D2T” signifies that we consider not only design but also testing. Through our activities, we hope to provide expertise in design and testing for the industry. In addition, we are exchanging researchers with those of other universities and research institutes both in Japan and overseas. Moreover, D2T research division is suitable for collaborations with the industry because VLSI testing is one of the most practical research topics in the industry. On the basis of these activities, our final goal is to become a center of excellence of VLSI testing in Japan.

D2T research division has spent a total of 12 years to develop the first (Oct. 2007 – Sep. 2010), second (Oct. 2010 – Sep. 2013), third (Oct. 2013 – Sep. 2016), and

fourth (Oct. 2016 – Sep. 2019) phases. D2T activity report of 2020 presents the last financial year, i.e., Oct. 2019 – Sep. 2020, of the fifth phase. Systems Design Center, School of Engineering, the University of Tokyo has been established in Oct. 2019, and Advantest D2T research department is within the center. D2T research department primarily focuses on D2T research activities and education. The fifth project phase (Oct. 2019 onwards) of D2T project will be commenced by courtesy of ADVANTEST Corporation.

In this financial year, we invited Professor Tsung-Hsein Lin (2019/8 – 2020/1) from National Taiwan University for research and educational collaboration with d.lab-VDEC.

The details pertaining to the activities of our group are presented in the following sections.

2.5.1.2 Members of ADVANTEST D2T Division

Project Professor	Masahiro Fujita
Project Professor	Tsung-Hsein Lin (2019/8 – 2020/1)
Project Lecturer	Akio Higo
Researcher	Koji Asami (Advantest Laboratories Ltd.)
Researcher	Masahiro Ishida (Advantest Corporation)
Researcher	Takahiro Yamaguchi
Assistant Clerk	Makiko Okazaki

2.5.2 Report of the 15th D2T Symposium

The 15th D2T Symposium was held on September 17, 2020 online. This year, we invited the following overseas lecturers to introduce their research on biosystems, RF, IoT, Memory, and Hardware security: Professor Brian Floyd from North Carolina State University, Professor Alex Orailoglu from University of California, San Diego, Mr. Takeshi Iwasaki from ASAHI KASEI MICRODEVICES, Kazumi Hatayama-sensei from EVALUTO Corporation and Gunma University, Assistant Professor Michihiro Shintani from NAIST, Associate Professor Masaharu Kobayashi from d.lab, the University of Tokyo and Mr. Ryo Tamura from Advantest Corporation for their distinguished research topics.

We sincerely appreciate each participant for their contributions to the symposium. We look forward to greater participation again at the next symposium.

15th D2T Symposium Program ONLINE

9:50	**Opening Remarks** **Tadahiro Kuroda** (Director, d.lab, School of Engineering, The University of Tokyo) **Yoshiaki Yoshida** (President & CEO, ADVANTEST CORPORATION)
10:00	**Session 1** (Chairpersons: Makoto Ikeda, Tetsuya Iizuka, d.lab, The University of Tokyo) Beamforming Arrays and their Test and Calibration **Brian Floyd**, Professor (North Carolina State University, Raleigh, NC) Adaptive Test Pattern Construction for Hardware Trojan Detection **Alex Orailoglu**, Professor (University of California, San Diego) The Solution of Testing the Millimeter-Wave (76- to 81- GHz) without Expensive Instruments **Takeshi Iwasaki**, (ASAHI KASEI MICRODEVICES CORPORATION))
12:00	**Lunch**
13:00	**Session 2** (Chairperson: Masahiro Fujita, d.lab, The University of Tokyo) Recycled FPGA detection using exhaustive fingerprinting characterization **Michihiro Shintani,** Assistant Professor (Nara Institute of Science and Technology) Viewing Test Technology Trends from presentations at Recent Test Related Conferences **Kazumi Hatayama**, (EVALUTO Corporation and Gunma University) **Session 3** (Chairperson: Ken Takeuchi, d.lab, The University of Tokyo) STT-MRAM memory test system with an electromagnet **Ryo Tamura**, (Advantest Corporation) A Monolithic Integration of RRAM Array and Oxide Semiconductor FET for In-memory Computing in 3D Neural Network **Masaharu Kobayashi**, Associate Professor (d.lab, the University of Tokyo) Recent D2T research department progress Akio Higo, Lecturer (d.lab, The University of Tokyo)
	Closing Remarks **Masahiro Fujita** (d.lab, School of Engineering, The University of Tokyo)

2.5.3 Research Activity Reports of the ADVANTEST D2T Research Department

High-Resolution Analog-to-Digital Converter Based on Stochastic Comparators

Takahiro J. Yamaguchi, Akio Higo, Tetsuya Iizuka

This project aims to explore stochastic analog-to-digital converter (ADC) architectures. Process variations, together with many factors such as variations in voltage or temperature, lead to mismatched design parameters that produce input-referred offsets and hence cause non-linearity and missing output codes in an ADC. Instead of attempting to suppress such process variations as in conventional ADC, the stochastic ADC approach exploits the stochastic properties of many comparators such as random variation of input-referred offset and Gaussianity of the internal noise to enhance the quantization accuracy. However, the published papers only show that stochastic ADCs are noisier than the conventional flash ADCs [TCAS-I,Vol. 57, no. 11, 2010]. The central limit theorem can be applied to discrete type RVs such as a group of comparators and their sum [A. Papoulis 2000]. It shows that for this discrete RV, many more terms are required in the sum before going convergence to a Gaussian distribution [S. L. Miller 2004]. These results in the adequate number of bits (ENOB) of the stochastic ADC are represented by log44B [TCAS-I,Vol. 57, no. 11, 2010], being smaller than the ENOB of the conventional flash ADC, which is given by log22B. An approach for robustly detecting level-crossing time using stochastic median is investigated to address randomness issues and achieve accuracy.

High-Performance Analog-to-Digital Conversion Using the Wideband Spread Spectrum and Its Applications

Koji Asami, Byambadorj Zolboo, Akio Higo, Tetsuya Iizuka, Masahiro Fujita

To measure low-cost RF devices for IoT and other applications, low-cost and high-efficiency analog-to-digital conversion techniques are required. To acquire narrow-band modulation signals scattered over a wide frequency range, a compression sampling method was investigated herein.

In this financial year, we analyzed the factor of the degrade of implemented Modulated Wideband Converter performance and developed a method to improve the performance. By unique calibration signals, a degrade wave from the periodic sign function to multiply to a measured signal before A/D conversion and a frequency characteristic of analog circuits in front of an A/D converter are separated and identified. A 4-channel MWC circuit was fabricated for the verification experiments.

5G multi-channel/millimeter-wave signal measurement

Koji Asami, Ryogo Koike, Nguyen Ngoc Mai-Khanh, Akio Higo, Tetsuya Iizuka, Masahiro Fujita

To measure the millimeter-wave signals in an over-the-air environment, we study and develop fundamental research. In this financial year, we were establishing the experimental setup for millimeter-wave measurement. We were preparing the radio box with spherical scanning and planar scanning stage inside for near-field and far-field millimeter-wave measurement. In addition, we designed and fabricated the directional probe, and we develop the calibration method for probe characteristics and antenna measurement.

High-Speed and High-accuracy Multi-Pin Timing CAL for ATE

Masahiro Ishida, Tetuya Iizuka, Zule Xe, Toru Nakura, Akio Higo, Masahiro Fujita

Semiconductor test equipment (ATE) has thousands to tens of thousands of signal input and output channels. It requires timing calibration (CAL) to correspond the test signal output's timing to the device under the test (DUT) and the comparison timing of the signals output from the DUT. In this research, we focus on a high-speed and high-accuracy multi-pin timing CAL method applicable to ATE. In this financial year, we identified issues to clarify our research goals and studied the circuit scheme to realize the timing of CAL. The target accuracy of the timing CAL was set at 1 ps. It clarified that the problem to achieve the target was to minimize the change in characteristics of the CAL circuit in response to environmental changes. The fundamental method of the timing CAL was determined by discussion, and a circuit simulation analyzed the effects of environmental changes such as applied voltage and temperature on the CAL error.

Kuroda Kosuge Laboratory
(http://www.kuroda.t.u-tokyo.ac.jp/index.html)

TCI: ThruChip Interface

T. Kuroda, M. Hamada, A. Kosuge, T. Shidei, M. Okada, Wai-Yeung Yip

TCI is a 3D integration technology that employs inductive coupling between coils created with on-chip metal line patterns for data communication across stacked chips. It realizes the same or better performance as TSV (Through Silicon Via) but at a lower cost. Last year, we presented the 3D SRAM stacking using TCI and the TCI 2.5-D integration technology.

TLC: Transmission Line Coupler

T. Kuroda, M. Hamada, A. Kosuge, T. Shidei, M. Okada, Wai-Yeung Yip, Y. Hayashi

TLC is a data communication technique between circuit boards by utilizing electromagnetic coupling between transmission lines on them. It solves the issues in conventional connectors such as wearing, reliability against vibration, and impedance mismatch, realizing wireless connectors. Last year, we presented new coupler technologies enabling long communication distance for direct board-to-board communication systems, and the compact SerDes circuit for transmitting multiple signals.

Takeuchi Laboratory
(https://co-design.t.u-tokyo.ac.jp/)

High Speed Semiconductor Storage

Chihiro Matsui and Ken Takeuchi

We have developed semiconductor storage system that uses different types of storage class memories (SCM) such as S-SCM and M-SCM which are slower than DRAM but has larger capacity and lower cost. Non-volatile memories store different types of data in order to resolve trade-offs in speed, energy consumption, cost, and reliability of storage-type SCM (S-SCM) and memory-type SCM (M-SCM). In addition, data management algorithm and ECC are developed for the storage system. Finally, a high-speed storage system is developed to autonomously adjust SCM capacity according to the application characteristics.

Approximate Memory

Chihiro Matsui and Ken Takeuchi

We have proposed approximate non-volatile memory system for 5G network. Performance and power evaluation platform is developed for the edge/cloud servers. Approximate memory that tolerates memory cell errors for machine learning applications is proposed to improve both performance and energy of the memory system. By efficiently using approximate memory, the bottleneck of 5G network system and the edge/cloud servers is resolved.

Long-term Semiconductor Memory

Ken Takeuchi

We have proposed long-term memory semiconductor memory system with ReRAM. The data lifetime is significantly improved by introducing the "Finalize" programming that increase the write voltage before the data-retention. In addition, by optimizing the program stress based on the endurance, both long-term data storage and high endurance are achieved.

Nakamura Laboratory
(http://www.hal.ipc.i.u-tokyo.ac.jp/index-e.html)

IoT/Cyber-Physical System

We investigated Reinforcement Learning (RL) optimization methods for Energy Harvesting Wireless Sensor Nodes (EHWSNs) by balancing the device energy consumption with the unpredictable energy supply. RL generally requires long time for learning because of large computing cost. For this problem, we proposed a distributed learning solution that coordinates the many sensor nodes of a network to ef-

ficiently explore the large state space concurrently. Our method significantly minimizes learning risks and accelerates the learning process.

Low-Power Computing

We conducted a research on power reduction of local 5G small cell base stations. Specifically, The proposed method co-optimizes the control of two power-performance knobs: the power of ampliers and the number of active antennas. For the co-optimization, the relationship between transmission ability and power consumption is modeled. The proposed method is applied to the case in which multiple nodes exist at different distances and have dynamic traffic. The experimental results reveal the proposed method reduces the power consumption effectively.

Network Security

Zigbee is a short-range wireless communication protocol and needs low power and low bandwidth at the sacrifice of its short transfer range and slow speed. Due to this nature, it is widely used in small inexpensive sensors and IoTs that run on batteries, As Zigbee uses indirect communication to achieve low power consumption, it incurs a vulnerability to LDoS attacks. To solve this problem, we proposed a countermeasure against it and confirmed its effectiveness through experimental simulation.

Fujita Laboratory

(http://www.cad.t.u-tokyo.ac.jp/)

Partial logic synthesis via training a topologically similar binarized neural network

Masahiro FUJITA, Chaoyi JIN

We present an experimental technique for solving partial logic synthesis problems through training a topologically similar binarized neural network. Partial logic synthesis means that most parts of the logic circuit are known whereas the missing portions must be logic synthesized from specification. By replacing 2-input logic gates with perceptron model and inheriting the topological structure of the logic circuit, we are able to recover the missing parts with back propagation and discrete training.

Quantization Techniques for Small Number of Bits in Transformer based Natural Language Processing

Masahiro FUJITA, Shin-ichi O'UCHI, Ding YI,

After decades of development, natural language processing is widely used in life and research. In recent years, the Transformer-based NLP model has achieved good results on many tasks, in which a model called BERT is a major progress in recent years. However, the BERT model is really large, which requires a lot of storage and computing resources. In order to implement the BERT model on hardware, Intel has built a project named Q8BERT to quantize the model parameters to save memory space and computing resources. This research implements the Q8BERT, and makes some improvements by proposing clipping, which is to limit the range of weights, and piece-wise quantization, which is to divide the range of weights into several pieces to get higher resolutions. We show experimentally that the clipping can get higher accuracy while inference, which is better than the Q8BERT. And we get some intermedium results of non-linear experiments. Experiments for piece-wise quantization are in progress.

Efficient Attention Mechanism by Softmax Function with Trained Coefficient

Masahiro FUJITA, Shin-ichi O'UCHI, Kaito HIROTA

BERT is a neural network model which has accomplished state-of-the-art performance on eleven natural language processing tasks such as inference and paraphrasing. So it is desired to make BERT based computations available on edge devices. We propose an efficient hardware implementation method for the part of this model by modifying Softmax function. Softmax function is a part of the most significant calculation in BERT in terms of computation cost, and its hardware implementation on FPGA or ASIC has not been explored. We have succeeded in reducing the number of additions and exponential functions to 1%, while retaining 95% of the BERT's accuracy through experiments.

Scheduling Sparse Matrix-Vector Multiplication onto Parallel Communication Architecture

Masahiro FUJITA, Ruitao GAO, Mingfei YU

There is an obvious trend to make use of hardware including many-core CPU, GPU and FPGA, to conduct computationally intensive tasks of deep learning implementations, while a large proportion of which can be formulated into the format of sparse matrix-vector multiplication(SpMV). In this research, the minimum scheduling problem of 4*4 SpMV on ring-connected architecture is first studied. We have put forward a decomposition-based algorithm for larger matrices. With the proposed algorithm, search space of the minimum schedule is considerably reduced. Through comparison with an exhaustive search method and a brute force-based parallel scheduling method, the proposed algorithm is proved to be able to offer scheduling solutions of high-equality: averagely utilize 65.27% of the sparseness of the involved matrices and achieve 91.39% of the performance of the solutions generated by exhaustive search, with a remarkable saving of compilation time cost (250 times less) and the best scalability among the above mentioned approaches.

Efficient Reachability Analysis Based on Inductive Invariant Using X-value Based Flipflop Selection

Masahiro FUJITA, Ryogo KOIKE

For sequetial circuits, it is well known that the sets of reachable states may be much smaller than the entire state space, and computing the supersets of reachable states is practically useful due to the less computational complexity than the exact set of the reachable states. Inductive invariant is the one of the methods to compute such supersets. For inductive invariants, it is important to select the subset of flipflops in order to find a small and/or useful superset of reachable state. Unknown value X based analysis is used to find the subset of flipflops. In some HWMCC2017 benchmark circuits, the proposed method can find the subset of flipflops to prove the correctness of the property. The calculation of inductive invariants is formulated with Quantified Boolean Formula. The QBF problem can be solved by repeatedly applying SAT solvers. We also show a way to reduce the number of variables in QBF problems. In the method, we start with smaller inputs LUT and gradually increase the number of inputs in order to reduce variables. This method has reduced calculation time by up to around 80% when solving large QBF problem.

SAT-Based Data-Flow Mapping Onto Array Processor

Masahiro FUJITA, Yukio MIYASAKA

Recently, it has been common to perform parallel processing in machine learning. Reconfigurable array processor is drawing attention in terms of easy custom adjustment and high

performance. We propose a method to map a data-flow onto an array processor using a SAT solver. The proposed method is combined with an automatic transformation method, which changes the order of calculations, to generate a more efficient computation scheme. We have solved mapping problems of matrix-vector multiplication. In our experiment, a SAT solver was more scalable than an ILP solver. Our method handled a dataflow of more than a hundred nodes using MAC operation. We have also mapped sparse matrix multiplication with varying latency and throughput and generated faster schedules utilizing the sparsity.

Evaluation on Approximate Multiplier for CNN Calculation

Masahiro FUJITA, Takashi MATSUMOTO, Yuechuan ZHANG

Improving the accuracy of a convolutional neural network (CNN) typically requires larger hardware with more energy consumption. On the other hand, the error tolerance of CNNs allows approximate computing to cut down the implementation costs. Given that multiplication is the most resource-intensive and power-hungry operation in CNNs, approximate multipliers (AMs) can be used to reduce hardware cost. There are various existing approximate multiplier generation methods. However, it remains unknown whether a specific AM is suitable for CNN calculation and its effect on inference accuracy. In this paper, we implement an 8-bit quantized Alex-

net into hardware. The relationship between error caused by AMs and the accuracy of CNN inference is established. Mainly two AMs are considered: 1) Cartesian Genetic Programming (CGP)-based AMs 2) flexible Error-estimating based AMs. Besides, we propose two techniques, input zoom and error compensation to improve the performance of AMs in CNN calculation.

Ikeda Laboratory

(http://www.mos.t.u-tokyo.ac.jp)

Design Optimization of High-Performance Cryptographic Engine

M. Ikeda, K. Ikeda, F. Arakawa

With the development of IoT technology, high-performance cryptographic engines, such as searchable cryptography and ID and attribute-based cryptography, are required to meet increasingly diverse requirement specifications. We improved the performance of the elliptic curve cryptography engine by using scheduling and an optimal modular multiplication algorithm, and obtained a latency of 18.14us including the coordinate transformation part. For the elliptic curve pairing, we optimized a large-scale scheduling problem and investigated a design method to automatically describe the sub-sequences in HDL using the results. This method is expected to improve the design cost, which is an issue in hardware cryptographic design.

Functional Encryption Engine Design

M. Ikeda, R. Nakayama, A. Opasatian, T. Shimada

High-functional cryptography exemplified by searchable encryption and ID and attribute-based encryption is the basis of privacy guard, that is the biggest concern in cloud services. Functional cryptography has a disadvantage that the cryptographic algorithms used for its implementation has high computational cost. In this study, we implemented and optimized two main algorithms, optimal Ate pairing on elliptic curve and fully homomorphic encryption (FHE). In both cases, we employed operations on quotient ring as the unit of arithmetic, and constructed pipeline by unrolling loop that is small but repeated many times in the algorithms. We introduced micro-sequencer on-chip to accelerate pairing engine on BN254 curve free from IO bottle neck, also we implemented multiple core architecture for further acceleration of the pairing engine. For FHE by RingLWE design, we have investigated optimum design of numeric theory translation (NTT). We also studied attribute-based encryption as a possible application hardware acceleration by the pairing engine.

Attack Resilience Evaluation of Cryptographic Circuits

M. Ikeda, K. Abe

Security of cryptographic circuits is threatened by side-channel attacks. In this work, we have evaluated the feasibility of lattice attacks that can break the digital signature algorithm. In lattice attacks, there is a trade-off between the amount of information obtained by side-channel attacks and the amount of computation required to recover the secret key. We have investigated conditions regarding the amount of information to recover the secret key within a realistic amount of time through experiments using various key lengths as targets of the attack, and some of the results showed the attack could recover the secret key with less information than reported in previous attacks. We have been investigating whether side-channel attacks can acquire enough information for lattice attacks, utilizing an ASIC chip in which ECDSA is implemented as an attack target and template attack as an attack method.

A study on hardware implementation of reservoir computing system

M. Ikeda, B. Amartuvshin

The hardware realization of artificial neural networks (ANNs) is a challenging task due to large resource requirements of the involved operations. Reservoir computing (RC), based on a random recurrent neural network (RNN), is a simple yet powerful model that is well suited for time-series data processing. It consists of a reservoir for mapping inputs into a high-dimensional space and a readout for pattern analysis from the high-dimensional states in the res-

ervoir. The reservoir is fixed and only the readout is trained with a simple method such as linear regression and classification. Thus, the major advantage of reservoir computing compared to other recurrent neural networks is fast learning, resulting in low training cost. We are trying to propose digital hardware implementations of echo state network (ESN) designed for brain-computer interface based on EEG time-series data with online learning capability.

Advanced 3-D Measurement System by Smart Image Sensors and Secure Sensing

M. Ikeda, Y. Liu, D. Jiang, and N. Watanabe

We have been working toward the advanced 3-D measurement system with secure sensing scheme by integrating smart signal processing functionality onto the smart image sensors. We have studied ToF image sensor with current mode background suppression capability for modulated light projection. We added phase shifting circuits for expanding the measurement ranges, and evaluated measurement accuracy according to parameter variations. We have also studied ToF image sensor with light to pulse frequency modulation pixel for both background suppression and digital signal selection capabilities.

Design and Measurement of Weak-Signal-Readout Integrated Circuit for Terahertz-Video-Imaging

M. Ikeda, and T. Kikkawa

We designed a readout integrated circuit (ROIC) for Terahertz-Video-Imaging which converts a weak signal detected by InAs MOS-HEMT to digital signal. The ROICs are integrated as 8x7 array on 180nm CMOS and utilized with the detectors stacked on them. Each ROIC contains transimpedance amplifier, lock-in amplifier and $\Delta\Sigma$ analog-to-digital converter as well as digital-to-analog converter (DAC) to calibrate the detectors. In our previous work, we cost a lot of time to optimize some control parameters. Therefore, we modified the architecture of the amplifier to realize higher gain and easier controllability. Moreover, as a DAC architecture, we employed a resistor string instead of capacitor bank to solve the problem of leakage current.

The fabricated chip is stacked with array of antennas and InAs MOS-HEMT detectors integrated on a glass substrate by stud bumps. By measurement with a THz signal generator, we realized synchronous-detection of the signal.

Iizuka Laboratory

(http://www.mos.t.u-tokyo.ac.jp/iizuka)

Waveform Reconstruction Technique for Wideband Signal

Tetsuya Iizuka, Byambadorj Zolboo

The Modulated Wideband Converter (MWC) is one of the promising Sub-Nyquist sampling architectures for sparse wideband signal sensing, cognitive radio applications and so on. Since resources within Automatic Test Equipment (ATE) are limited on sampling rate, the MWC can be useful for testing devices with various frequency band.

In this research, we are investigating a feasibility of MWC to reconstruct a waveform of sparse wideband signals for measurement equipment.

The reconstruction performance based on the ideal sensing matrix was not acceptable due to the non-ideal hardware components. The conventional way of the calibration is to stimulate the MWC with sequential single-tone signals then estimates the actual sensing matric components. This method is quite time-consuming and inaccurate. Thus, we proposed novel calibration method for the MWC using multi-tone signal to estimate the actual sensing matrix from a single measurement to reduce the calibration time and the timing noise. In terms of NMSE performance, the proposed calibration method has reasonably good performance compared to the conventional one.

In terms of noise performance, we proposed an average noise figure (ANF) theoretical notation to expect the noise figure of MWC. The accuracy of the analytical formula is ensured with MATLAB simulation results. We have also verified the analytical formula in the practical implementations.

We proposed a new method for constructing a digital compensation filter to equalize a non-ideal frequency characteristic of an analog filter. Without the compensation filter, the reconstruction perfor-

mance of the MWC is not satisfactory. Thus, the digital compensation filter is necessary for practical realizations to maximize the performances. The previous works by other researchers were impossible to estimate the LPF without disconnecting the LPF circuit from the MWC circuit, which makes the method infeasible in some practical implementations. The other issue was that the compensation filter building method could not be used in the advanced MWC case. The proposed method can be directly used in the advanced MWC circuit without disconnecting any component.

We demonstrated the measurement results of the MWC taken from the practical implementation. The measurement result of the noise figure in MWC validates the correctness of the theoretical noise analysis. The proposed calibration technique for the MWC estimated the actual sensing matrix coefficients with single measurements. In contrast, conventional calibration needs many measurements. The calibration performance has been demonstrated in NMSE and IRR compared to the uncalibrated performance; more than 50 dB and 42 dB improvements have been achieved on NMSE and IRR, respectively.

Phase-Locked Loop Circuit Techniques for Low Phase Noise

Tetsuya Iizuka, Zule Xu, Masaru Osada, Ryoga Iwashita, Ryoya Shibata

We implemented a fractional-N PLL that achieves low-noise in a compact manner by employing a HM (Harmonic-Mixer) and a dual-feedback architecture to avoid noise amplification, then demonstrated its benefits through measurements. Furthermore, we performed an analysis of tones that can arise in all S/H (Sample-and-Hold) circuit-based HMs, and established a design methodology for LPFs (Low-Pass-Filters) to suppress these tones. Finally, we proposed a new PLL architecture where an auxiliary PLL is placed in the feedback path of the dual-feedback PLL to further suppress the DSM quantization noise, and demonstrated its benefits through simulation. This architecture can allow low-noise, ring oscillator based PLLs to be realized without complex calibration schemes such as LMS, and is expected to be of great use in applications such as communications and sensing.

We proposed a digital PLL architecture that achieves low phase noise by introducing noise shaping ADC to phase detector. First, the quantization noise of TDC(Time-to-Digital Converter)-PLL can be reduced by replacing conventional nyquist TDC with ΔΣ TDC that consists of phase detector and voltage-controlled delay line. ΔΣ TDC was proposed in previous research. Second, in order to reduce the quantization noise of FDC(Frequency-to-Digital Converter)-PLL which controls the output frequency by feedback to divider, the design of high order ΔΣ FDC was achieved by cascade connection of ΔΣ ADC and quantizer in FDC. The noise performance of these two PLLs was demonstrated through simulations. It is proved that FDC noise is lower than TDC noise because of quantization bit rate, and that ΔΣ FDC-PLL is more practical than ΔΣ TDC-PLL because the cost of ΔΣ FDC-PLL is fewer.

We demonstrated LPF is necessary before and behind in frequency conversion in main PLL of Triple-loop PLL by Matlab Simulink. This LPF decreases the spurious which may occur because of convolution of RF signal from VCO and LO signal from Integer-N PLL in frequency region. Furthermore, we improved frequency conversion part in TL-PLL and demonstrated TL-PLL can be used in 28GHz for 5G NR communication by schematic design and simulation. In this design, we used Subharmonic mixer instead of Sample & Hold circuit used in previous research and Ring Oscillator for LO input to convert high frequency using the merit of TL-PLL which can avoid increasing noise in loop.

High-Precision Analog-to-Digital Conversion Circuit Techniques

Tetsuya Iizuka, Zule Xu, Shuowei Li, Akira Matsuoka

With the increasing demand for high-speed communication and high-speed analog-to-digital converter, the design demand for high-speed and low-power comparators is increasing. The Strong-ARM comparator can meet the demand well.

A conventional Strong-ARM comparator usually has a large offset. In previous research, an auxiliary

circuit was proposed to reduce the offset of the comparator by current compensation. In this research, we build the mathematical model to describe the operating principle of such Strong-ARM comparator and the influence of the introduction of an auxiliary circuit with different parameter settings on the performance of the comparator. The simulation results show that the model can describe the behavior of the comparator and predict the influence of the auxiliary circuit on the main circuit well. The designer can effectively set the parameters of the auxiliary circuit and globally optimize the comparator based on this model.

High-resolution analog-to-digital converters (ADC) are essential for audio and sensor applications, and oversampling ADCs are used due to the noise-shaping and oversampling. Discrete-time delta-sigma ADCs (DT DS ADC) is one of the oversampling ADCs and has an advantage in its robustness to clock jitter and PVT variations. To reduce power consumption in DT DS ADC, dynamic amplifier is used, which has no static current. We presented a second-order delta-sigma ADC with closed-loop dynamic floating inverter amplifier (FIA).

FIA has a stable output common-mode voltage and unsensitive to input common-mode voltage. To get high SNR, high gain FIA + Cascode FIA was proposed. Simulation results showed that FIA + Cascode FIA had high gain and input common-mode voltage robustness. Proposed ADC achieved a 85.5 dB SNDR while consuming 45.5 μW in simulation.

Millimeter-Wave Circuit Design for Communication through Dielectric Waveguide

Tetsuya Iizuka, Mai-Khanh Nguyen Ngoc, Takamichi Horikawa

Recently, a high-speed communication technique with millimeter-wave (mm-wave) band has been actively studied for its wide bandwidth. A power amplifier (PA) with high output power is always demanded for these purposes to further improve the system performance such as communication distance, data rate and signal-to-noise ratio. In this research we proposed a PA architecture that realizes high output power in D-band by using a balun-based power combiner. With a simple combining structure, however, there is a challenge in achieving the optimum impedance matching in > 100 GHz mm-wave due to its layout asymmetry. In this paper we propose a symmetric layout structure in the balun-based power combiner in D-band to have equal input impedance at all the primary input ports so that the former-stage amplifiers can look into balanced impedance. A 2-parallel power-combined amplifier is fabricated in a 65-nm bulk CMOS process, which achieves 6.0 dBm OP1dB and 11.4 dBm saturated output power. A 4-parallel prototype with the symmetric-balun-based power combiner is designed and verified with post-layout simulation with the same process technology, which achieves 9.4 dBm OP1dB and 14 dBm saturated output power.

Implementation of Neuron Device based on CMOS Analog Circuits

Tetsuya Iizuka, Xiangyu Chen

Neuromorphic computing is a technique that simulates the biological mechanisms of neurons and synapses in the human brain and is being actively studied and applied in various fields. The spiking neural network (SNN) is called the third-generation artificial neural network, which more realistically imitates biological neural networks. Among the many models, due to the simplicity of the leaky integrate-and-fire (LIF) neuron model, it has received widespread attention.

In most cases, neurons need a very large time constant to process signals. However, large on-chip capacitors and resistors are not conducive to system integration. Based on the LIF model, we designed an analog neuron element with a small area and an adjustable time constant. Proposed circuit consists of a capacitor and two pseudo resistors (PRs). By adjusting the bias voltage of PR, the time constant of the circuit can be changed. The capacitance is a constant value of 2pF, and the maximum time constant can reach 0.15ms with TSMC 65nm process fabrication.

We also constructed a synapse circuit based on a ring oscillator. This circuit uses leakage current to drive the oscillator to work, hence it consumes very little energy. The synapse integrates the impulse

from the neuron and outputs a frequency signal corresponding to the value of the integral, which is transmitted to the next neuron. We taped out the proposed circuit using TSMC 65nm process.

Hiramoto & Kobayashi Laboratory

(http://nano-lsi.iis.u-tokyo.ac.jp/)

Variability in Nano-Scale CMOS Devices

Toshiro Hiramoto and Masaharu Kobayashi

As the size of MOS transistors is miniaturized, the effect of random variability of device characteristics is becoming too large to be overlooked. Although the main reason in conventional bulk transistors is the fluctuation of the number of dopants, the variability causes of nanowire transistors, which is one of the next-generation device candidates, remain unknown. In this study, we have clarified that the quantum confinement fluctuation caused by line width roughness is the new origin of random threshold voltage variability. We are also investigating the effect on the drain current variability.

Low Temperature Characteristics of Nano-Scale CMOS Devices

Toshiro Hiramoto and Masaharu Kobayashi

The quantum computing has attractive much attention for a future computing technology that is fundamentally different from classical computing by CMOS circuits. In the quantum computing systems, conventional CMOS circuits are utilized to control quantum bits. Therefore, it is essential to clarify and model CMOS transistor characteristics at low temperature. In this study, we are studying the subthreshold swing of bulk and nanowire transistors. We are also evaluating the characteristics variability at low temperature.

Silicon Power Devices

Toshiro Hiramoto

Although new materials such as SiC or GaN are widely studied for power devices, silicon IGBT (Insulated Gate Bipolar Transistor) is still a mainstream device for power electronics in very wide range of rated voltages. In this study, we are pursuing the potential of silicon IGBT based on new concepts of IGBT scaling and double-gate IGBT.

Device Physics of Negative Capacitance Field-Effect-Transistor

Masaharu Kobayashi and Toshiro Hiramoto

Negative capacitance FET (NCFET) is a promising next generation transistor technology which can break the physical limit of 60mV/dec in subthreshold swing. However, the comprehensive understanding on the physics of such steep subthreshold slope and unique phenomena has not been done yet. In this work, based on the transient negative capacitance by the dynamics of ferroelectric polarization switching, we made a more comprehensive NCFET model including fixed charge and charge trap in the insulator and at the interface, which contributes to further physical understanding of the device physics of NCFET.

3D neural network by co-integration of IGZO transistor and RRAM

Masaharu Kobayashi and Toshiro Hiramoto

AI algorithm such as machine learning requires massive data for learning and inference. Thus conventional computing using CPU and main memory has severe challenges on the bottleneck of data transfer. In-memory computing is getting more attentions to tackle this challenge by the fusion of computation and memory function. However, in order to increase the accuracy of the neural network, memory array size needs to be increased, which causes long latency and energy consumption in the interconnects. In this study, we developed monolithic integration of IGZO FET and RRAM on the interconnect layers. We demonstrated no performance degradation through this co-integration process. We also demonstrated XNOR operation by using IGZO FET and RRAM as a basic element of binary neural network.

Physical mechanism of the emergence of ferroelectricity in HfO2

Masaharu Kobayashi and Toshiro Hiramoto

Ferroelectric HfO2 is getting much attentions

as an emerging memory material which is CMOS compatible showing ferroelectricity even at less than 10nm thickness. It is known that doped HfO2 induces asymmetric orthorhombic phase in a thermal process, which leads to ferroelectricity. However, the physical mechanism of the emergence of ferroelectricity in HfO2 through the whole thermal process has not been fully understood yet. In this study, by using ab-initio calculation, we revealed two step phase transition process: (1) amorphous phase to tetragonal phase at high temperature due to dopant effect and interface energy, and (2) tetragonal phase to ferroelectric phase due to the kinetics of selective transition by thermal activation barrier. The latter was confirmed by ab-initio molecular dynamics simulation.

Takagi Laboratory

(https://sites.google.com/g.ecc.u-tokyo.ac.jp/mosfet/)

III-V Metal-Oxide-Semiconductor (MOS) FETs and the 3 dimensional integration

S. Takagi, Kei Sumita, Jun Takeyasu, Ryohei Yoshizu, Kasidit Toprasertpong, M. Takenaka

3D-integrated CMOS, in which transistors are vertically stacked, is expected to be a key device for future logic LSIs. In order to realize such stacked MOSFETs, channels such as III-V compound semiconductors and Ge are promising because they can be fabricated at low temperatures and are expected to have high mobility and injection speed. In our laboratory, we are investigating the realization of ultra-thin III-V-On-Insulator (III-V-OI) structures on Si substrates, and the performance improvement of III-V nMOSFETs using these structures aiming at application to 3D stacked CMOS. In this fiscal year, we have proposed a novel subband engineering using (111) surface ultra-thin InAs-OI channels with high electron mobility, and have demonstrated InAs nMOSFETs on Si using the smart-cut method. Furthermore, we have also proposed a method to evaluate the contact resistance with InAs metal alloys and have demonstrated that it has extremely low contact resistance.

Ge Metal-Oxide-Semiconductor (MOS) FETs and the 3 dimensional integration

S. Takagi, Cheol-Min Lim, Tsung-En Lee, Chia Tsong Chen, Xueyang Han, Makoto Kutaragi, Kasidit Toprasertpong, M. Takenaka

We are investigating the technology to realize ultra-thin Ge-On-Insulator (GOI) structures on Si substrates, the performance improvement of high-performance GOI CMOS using these structures, and the device physics that determines the electrical characteristics, with the aim of applying them to 3D integrated CMOS. In this fiscal year, we have demonstrated the operation of (111)-surface GOI nMOSFETs using the substrate bonding method, for the first time, and the higher mobility than that on (100)-surface ones. We also investigated a gate stack formation technique on SiGe channels with improved MOS interface characteristics, and have found that a low interface defect density can be achieved by using a TiN/Y2O3 gate stack with a TMA surface treatment.

HfO2-based Ferroelectric devices

S. Takagi, Kasidit Toprasertpong, Xuan Luo, Kento Tahara, M. Takenaka

MOSFETs (FeFETs) using ferroelectrics with polarization reversal as gate dielectrics and FeRAMs using metal sandwich structures (MFM structures) as memory cells are expected to be future devices for ultra-low power memory and logic. In particular, devices based on ferroelectric and anti-ferroelectric materials such as Hf1-xZrxO2 and ZrO2, which have been discovered recently, are of great interest because of their extremely high compatibility with current Si CMOS technology. We are studying the properties of these ferroelectric thin films deposited by atomic layer deposition (ALD) method, the device operation principle of FeFETs and the optimum device structures to realize excellent device characteristics. In this year's research, we have demonstrated an MFM memory cells with significantly reduced operating voltage by reducing the crystallization temperature of Hf0.5Zr0.5O2 and thinning the films to take advantage of the wake-up effect of the ferroelectric properties.

Reservoir computing based on ferroelectric devices

S. Takagi, Kasidit Toprasertpong, Eishin Nako, Zeyu Wang, R. Nakane, M. Takenaka

Reservoir computing has recently attracted attention as a AI computation method with computational load for learning. We have recently proposed that FeFETs and FeRAMs with memory-in-logic and nonlinear analog computing functions are promising hardware for physical implementation of reservoir computing. Also, we have demonstrated its reservoir computing operation for the first time in the world. Aiming to realize new AI hardware on Si platforms that can perform inference and learning with extremely low power consumption, we are conducting research on improving AI performance by optimizing operation ways and device structures.

Understanding of Si CMOS operation under ultra-low temperature for quantum computing application

S. Takagi, Minsoo Kang, Kasidit Toprasertpong, M. Takenaka

In quantum computing systems, in addition to devices that manipulate qubits, CMOS integrated circuits that control signals are also indispensable. To scaling up the quantum computing system, it is necessary to place Si CMOS circuits that can operate at cryogenic temperatures such as 4K near the devices for qubit operation. For this purpose, it is mandatory to quantitatively clarify the behavior of MOS transistors at cryogenic temperatures with deep understanding of their physical mechanism. We are conducting experimental and theoretical studies to clarify the electrical characteristics and reliability of Si MOSFETs at cryogenic temperatures and to quantify the physical parameters.

Takenaka Laboratory

(https://sites.google.com/g.ecc.u-tokyo.ac.jp/takenaka-lab/)

On-chip/Off-chip optical interconnect

Mitsuru Takenaka, Naoki Sekine, Hanzhi Tang, Qianfeng Chen, Dongrui Wu, Yuto Miyatake, Takaya Ochiai

We have been conducting research on optical interconnection and I/O of LSIs using silicon photonics and other technologies. We have succeeded in demonstrating the operation of a hybrid MOS optical modulator consisting of an ultra-thin InGaAsP membrane bonded to a silicon ring resonator. We have also proposed a waveguide-type hybrid phototransistor, in which an ultrathin InGaAs membrane is bonded onto a silicon waveguide. By using the silicon waveguide as the gate electrode, we succeeded in demonstrating extremely high sensitivity. In addition, the operation of a hybrid optical modulator combining a slot optical waveguide with an InP membrane and an EO polymer was analyzed, and it was shown that optical modulation at a rate of over 100 Gb/s was possible.

Si photonic integrated circuit for AI

Mitsuru Takenaka, Hanzhi Tang, Shuhei Ohno, Yuto Miyatake, Kohei Watanabe, Kazuma Taki

We have been conducting research on deep learning for AI using programmable photonic circuits such as universal optical circuits. We have demonstrated that the programmable silicon photonic circuits with the prototype ring resonator crossbar array can perform MAC operations and inferential operations are possible. We also proposed on-chip backpropagation using silicon photonic circuits, and successfully demonstrated its basic operation.

Ge mid-infrared photonic integrated circuit

M. Takenaka, Ziqiang Zhao, Yuto Miyatake, Chao Zhang

We have been studying mid-infrared photonic integrated circuits based on Ge waveguides formed on Ge-on-insulator (GeOI) wafer. We have successfully fabricated phototransistors by forming PNP- or NPN-type junctions in Ge waveguides for the first

time. We have also developed a mid-infrared optical phase shifter using phase-change materials. We demonstrated that a low-loss optical phase shifter can be realized by using GST at the mid-infrared wavelength.

2D material devices

Mitsuru Takenaka, Roda Nur, Xiaoxuan Zhang, Tipat Piyapatarakul

We have been studying semiconductor devices using graphene and molybdenum disulfide. Schottky junctions fabricated by transferring molybdenum disulfide onto Si substrates using the scotch tape method were formed and we quantitatively evaluated the carrier concentration of molybdenum disulfide from capacitance measurements. By combining the carrier concentration obtained with the Schottky junctions and capacitance measurement results of molybdenum disulfide MOS capacitors fabricated by the same method, we succeeded in quantitatively evaluating the energy distribution of the interface trap density using the Terman method.

Uchida Laboratory

(http://www.ssn.t.u-tokyo.ac.jp/publications/awards/)

Nanoscale Molecular Sensors for Volatile Organic Compounds (VOC)

Ken Uchida

Human breath contains various kinds of volatile organic compounds (VOCs), in which metabolites related with diseases or health condition should be included. Therefore, we can expect that the very early diagnosis of the disease could be achieved, if VOCs related with human diseases can be selectively detected. We have experimentally demonstrated successful operations of low-power metal-nanosheet-based molecular sensors. However, atomistic-level simulation methodologies which can reproduce the response of molecular sensors have not been established. We have developed a new atomistic simulation method for molecular sensors by combining the molecular dynamics simulation and the nonequilibrium Green's function method. In future, the developed technique will be applied to various types of molecular sensors and the accuracy will be intensively checked to further improve the calculation technique and to find materials for new types of molecular sensors.

Thermal-aware Design of Nanodevices

Ken Uchida

LSI has drastically improved the performance by reducing the size of MOS transistors. Recently, the introduction of new three-dimensional device structure; nanosheet transistor, is expected, and the Joule-heating-induced temperature rise in device channel is suggested as one of the most serious problems. We have developed a technique to minimize the operating temperature of the CMOS channel by thermal-aware design. Moreover, detailed evaluations of the electron-phonon transport properties have been conducted in our group. The molecular dynamic simulation and the nonequilibrium Green's function method were simultaneously performed, and it is suggested that there are vibrational modes peculiar to the Si/SiO2 interface, and that the vibrational mode enhances the electron-phonon scattering near the interface.

Someya Laboratory

(http://www.ntech.t.u-tokyo.ac.jp/)

Breathable mechanoacoustic sensor that listens to your heart

Md Osman Goni Nayeem and Takao Someya

We developed a multilayered nanofiber structured ultralight weight (5 mg) mechanoacoustic sensor with world's highest acoustic sensitivity. In addition, our sensor allows the skin to breathe when attached on chest wall of a human subject. In future, it is expected that our sensor may replace the bulky stethoscope that requires highly skilled clinicians to identify abnormal heart sounds, and even current state-of-art wearable patch type sensor that lacks breathability for continuous inflammation-free heart monitoring.

Mita Laboratory

(http://www.if.t.u-tokyo.ac.jp)

TopoMEMS: Development of Ideal Variable MEMS in view of Future Topological Quantum Computing

Y. Mita, K.Tsuji, A.Higo, T.Iizuka, Z.Xu, M.Ezawa (Dept. Applied Physics)

Recently, new computation methods that use Topological nature are drawing much attentions in view of future Quantum computing. Calculation takes advantages Topological natures existing in several different fields expressed as Hamiltonian matrices. Our team, granted by JST CREST project, tries to explore electrical expression of Hamiltonian matrices used for computation. Team Mita will develop ideal variable electrical devices as well as ideal MEMS devices. We named such devices and systems "TopoMEMS". As an initiating study, we have taken Su-Schriffer-Heeger model. We have developed a MEMS state-variable capacitor integrated SSH electrical circuit and have been successful in Topological / Trivial state switching due to MEMS device. Through the experiences, an ideal MEMS device design has been identified and fabrication process was developed.

Programmable Matter - Study on LSI-MEMS energy-autonomous distributed microsystems for realization of deformable matter

Y. Mita, K.Misumi, N.Usami (Dept. of Aeronautics and Astronautics),

E. Lebrasseur, G. Hwang (LIMMS, CNRS-UTokyo IIS / CNRS C2N),

G. Ulliac, (LIMMS, CNRS-UTokyo IIS, FEMTO-ST),

J.Bourgeois, B.Piranda (FEMTO-ST, France), S. Delalande (Groupe PSA, France)

As one example of future integrated MEMS that is expected to open new research and industrial application fields, the authors are trying to show a top-down application of energy-autonomous distributed microrobots. A number of identical tiny robots, sized below 1cm, will be released in an environment. Individual robot can communicate with their neighbor, stick each other, and share energy, to realize cooperative function. The PI is receiving a French National Research Center (ANR) grant on behalf of host professor of CNRS laboratory in the Institute of Industrial Science (LIMMS, CNRS-IIS, UMI 2820), together with FEMTO-ST Laboratory and PSA-Peugeot Laboratory for such "micro robots that can realize deformable substance by cooperative action, named Programmable Matter". In year 2020, an electrostatic chucking actuator system that attaches and detaches the external skeleton of the Matter has been presented in an international conference. Based on the actuation force electromagnetically analyzed, the ideal structure of the flexible electrode (named Flexiboard) has been identified, and fabrication technology of flexible electrode has been investigated.

Integration of electrode devices on MEMS fluidic devices

Y. Mita,A. Higo, T.Ezawa, E.Ota, Y.Okamoto (AIST), N.Washizu (Advantest), A.Takada (Advantest), M. Fujiwara, T.Sawamura

Towards the goal of production of brand-new sensor devices with higher sensitivity and functionality, the team is working on small-gap electrode fabrication process. This year we have integrated depletion type FET with microelectrode. Because channel of depletion FET is open at the gate-source voltage as low as 0V, the sensor can get rid of parasitic current and thereby leading to higher precision measurement. A special ASIC with threshold tuned depletion transistor was integrated with electrode, and coulter measurement has been successful.

Fine Large-Area Electron Beam Lithography Exposure Methods

A. Higo, Y. Ochiai, M. Fujiwara, T.Sawamura, Y. Mita

The team explores newly-acquired (in 2013) rapid electron beam writer F7000S-VD02. The capability of high electron dose and sharp edge due to cell (character) projection machine configuration is being examined. The breakthrough in question is to extend the large-area EB lithography, whose pattern approximation have been limited to rectangular shapes, into expressing free-form smooth shapes and

a number of periodical small patterns. This year, pattern and process design has been successful to obtain gap structure less than 16-nm wide.

Universities-Industries collaborative research on highly-functional system by MEMS post-process of CMOS-VLSI

Y. Mita, T. Yamaguchi, T. Lévi(IMS-CNRS,Bordeaux), G. Larrieu (LAAS-CNRS,Toulouse), Y.Ikeuchi (IIS), K. Saito (Nihon Univ.), Y.Sato (Nanox Japan)

The research targets are new sensor devices, made by post-process at clearnrooms such as d.lab Takeda Supercleanroom and others, of VLSI wafer made through VDEC. The important finding has been that VLSI wafer acquired just after transistor fabrication could sustain processes even with heat treatment, such as deposition, ion implantation, and drive-in. In 2016, a VLSI device made on Silicon-on-Insulator (SOI) wafer was successfully Deep-RIE processed. The industrial interest is its versatility – many different types of application devices, which differ one from another according to request of market, can be fabricated by using the same technology. More and more companies are interested in the scheme and are working on the technology on the collaborative research projects, including international cooperative research projects.

High-sensitive ultrasonic probe by integrated MEMS technology

Y. Mita, A.Higo, T.Yoshimura (Osaka Prefectural University), T.Mizuno (Konika Minolta), K.Suzuki (Konika Minolta), Y.Nakayama (Konika Minolta), T.Endo (Nagoya Medical Center)

Using the same scheme as above mentioned CMOS-MEMS post process R&D scheme, this project aims at integrating piezoelectric material and MEMS post-processing to obtain a brand-new ultrasonic inspection probe, whose sensitivity is as 100 times as cutting-edge technology. In year 2020, the team investigated LSI test circuit of high-voltage electronic circuit, fabricated by support from a public funding from Japan Agency of MEdical Research and Development (AMED). Based on the results obtained, an application LSI circuit was designed for small-scale image acquisition system.

Project PARIS: PARallel Integrated microSystem for High Frequency Action-Based Non-Invasive Multi-Modal Cell Analyses

Y.Mita, T.Tsuchiya, K.Misumi, Y.Okamoto (AIST), A.Mizushima, E.Lebrasseur, T.Bauvent (ENS Paris-Saclay, exchange student), C.Moslonka (ENS Paris-Saclay, VDEC internship student), B. le Pioufle C.Moslonka (ENS Paris-Saclay), Tixier Mita Agnès (UTokyo RCAST), Olivier Français (ESIEE, Univ. Paris Est), F.Marty (ESIEE, Univ. Paris Est)

Having granted again JSPS-CNRS bilateral project 2018, the team is developing a large-scale multi-modal cell analyses system (project name: PARIS). The electrorotation method, which is known to measure a mechanical rotational response to the incident rotational electrical field frequency is used. The method is non-invasive so the evaluated cells are possible to be used in further biological experiments. In year 2020, massively parallel device has been investigated. Device topology that can infinitely expand the working area and corresponding fabrication process of sandwitched electrode array have been successfully developed.

Colloidal integrated Infrared Detector

A.Higo, N.Miyazawa, N. Usami, M. Kobayashi (Dept. EEIS),

W. Haibin, N. Kubo, K. Segawa (RCAST), Y. Mita

Electron devices using colloidal quantum dots are believed to open new application fields such as light emitting devices and or photovoltaics. Up to date, very few research activities have been done in sensors applications; if we can realize integrated photodiodes that have extended sensitive wavelength as long as 1.35μm-1.4μm wavelength, such devices can be used by many new applications such as security cameras and / or Laser Radar (Lidar) under sunlight. The aim of this research is to find an integration method for beyond Si-LSI device. We try to integrate colloidal quantum dots of which absorption spectra can be designed through molecular design. By integration, Silicon device will be able not only to capture infrared wavelength lights, which is impossi-

ble by its original characteristics, but also my include information reading and computation circuits. For the first year's exploratory study, partly financed by the LIMMS internal project grant, spin coating integration method has been investigated. Root cause that prevented Electrical Quantum Efficiency has been identified to an unexpected reverse Schottky junction. The existence of unexpected junction was first confirmed by using new test structure (Coaxial Circular TLM) and was doubly confirmed by Angle-Resolved Photo-Emission Spectroscopy (ARPES). Based on the result, device parameter optimization has been made and resulted in better External Quantum Efficiency (EQE).

Development of zero power multiple-threshold maximum acceleration sensor for cyber physical system

Y. Mita, R Ranga Reddy

D.lab is awarded a Japanese JST – Indian DST joint grant (SICORP) for cyber physical systems research, in cooperation with IIT Bombay campus. The team is participating the project through a Shock Resonant Spectrum (SRS) sensor, which has been a research theme of 2012-2014. A new Ph.D student from India is assigned and fabrication process was recovered. This year we have analyzed complete system to record 10-levels of maximum acceleration in MEMS device. Based on the result, we have started collaboration with India. We have distantly followed research internship student from IITH who stayed three months. Also, the design heritage of latching mechanism has been employed for development of ideal MEMS research in view of future quantum computing.

Appendix

A.1 VDEC CAD Tools

Since 1996, VDEC has provided CAD software licenses to the registered researchers in universities and colleges in Japan. The CAD tools we provided in 2021 through the activities of VDEC in Systems Design Lab (d.lab) are shown in Table A.1.1. The researchers can use those CAD tools when their local machines, whose IP addresses are registered in advance, are authorized by one of VDEC license server located in the ten VDEC subcenters shown in Figure A.1.1. For each CAD tool, VDEC provides 10-100 floating licenses. Those CAD tools can be utilized only for research and education activities in national universities, other public universities, private universities, and colleges.

When one is going to use VDEC CAD tools and chip fabrication service (the details are described in Section 1-3), some faculty member of his/her research group in a university or a collage needs to do user registration. Figure A.1.2 shows (a) the number of registrants, (b) the number of distinguished universities/colleges of the registrants, and (c) the number of registrants who applied VDEC CAD tools, (d) the number of applied licenses of all CAD tools.

Table A.1.1 VDEC CAD tools

Name	Function	Vendor
Cadence tool set	Verilog-HDL/VHDL entry, Simlation, Logic synthesis, Test pattern generation, Cell-based (including macros) place, route, and back-annotation, Interactive schematic and layout editor, Analog circuit simulation, Logic verification, Circuit extraction	Cadence Design Systems, Inc.
Synopsys tool set	Verilog-HDL/VHDK simula-tion, Logic synthesis, Test pattern generation, Cell-based (including mac-ros) place, route, and back-annotation, Circuit simulation, Device simula-tion	Synopsys, Inc.
Mentor tool set	Layout verification, Design rule check	Mentor Graphics Co. Ltd.
Silvaco tool set	Fast circuit simulation	Silvaco
ADS/Golden Gate	Design and verification of high-frequency cir-cuits	Keysight Technologies
Bach system	BachC-based design, synthesis, and verification	Sharp
LAVIS	Layout visualization platform	TOOL

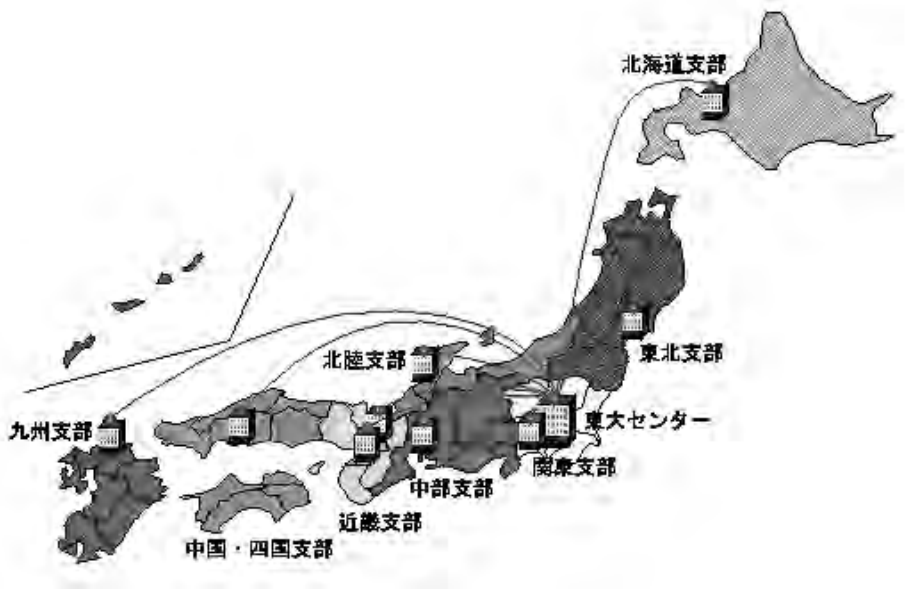
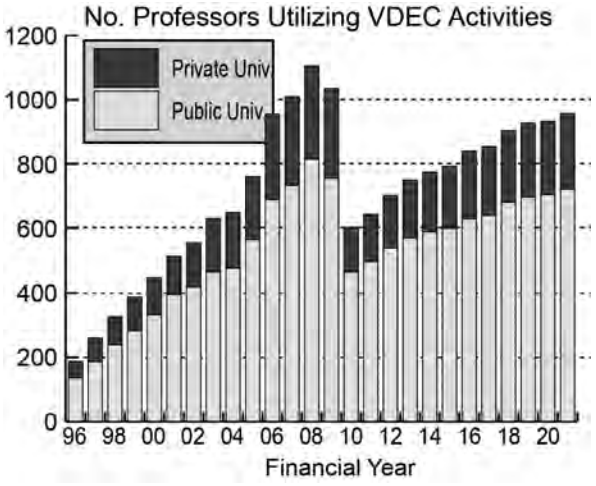
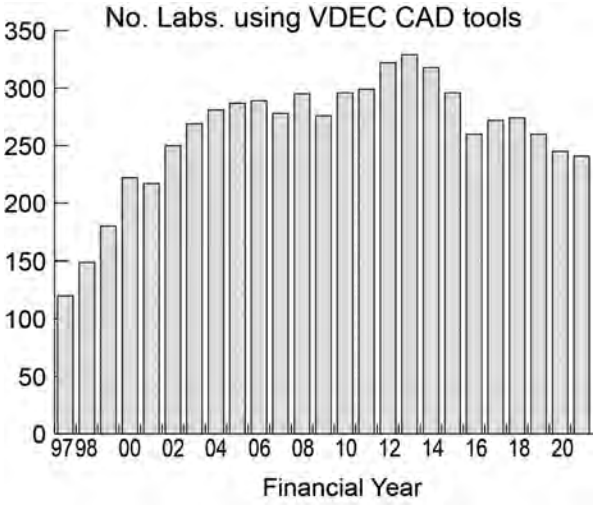


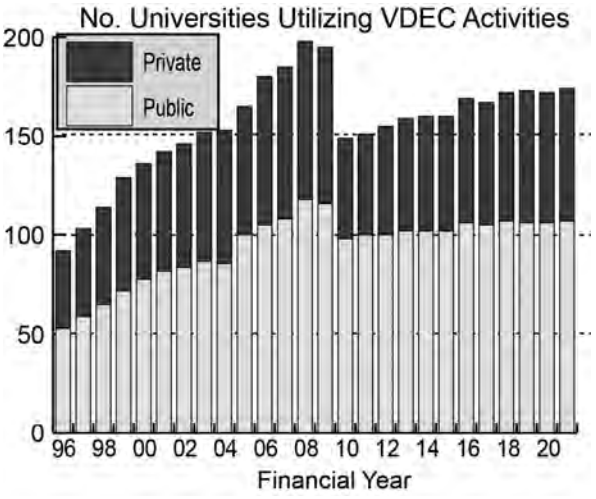
Fig. A.1.1 VDEC Subcenters



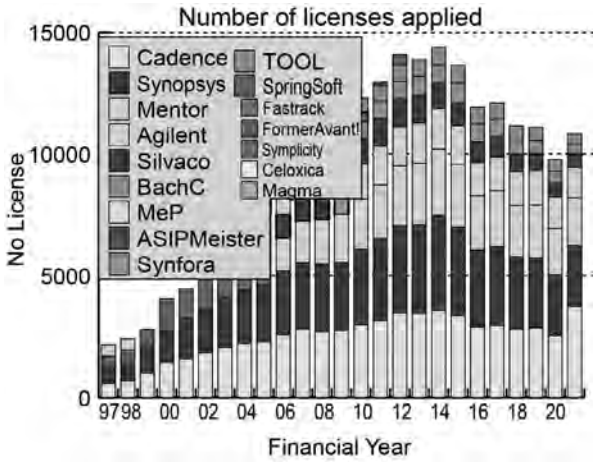
Fig(a)



Fig(c)



Fig(b)

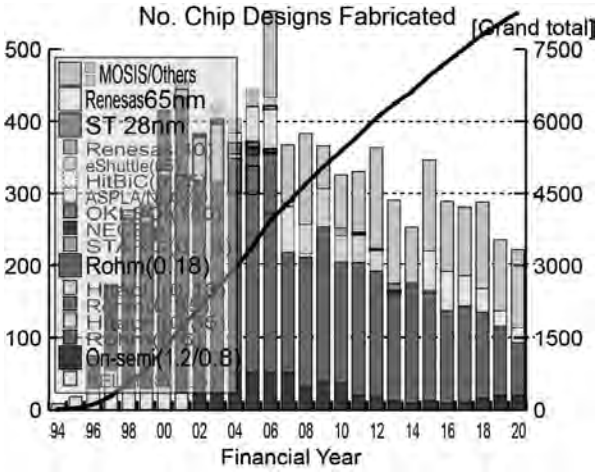


Fig(d)

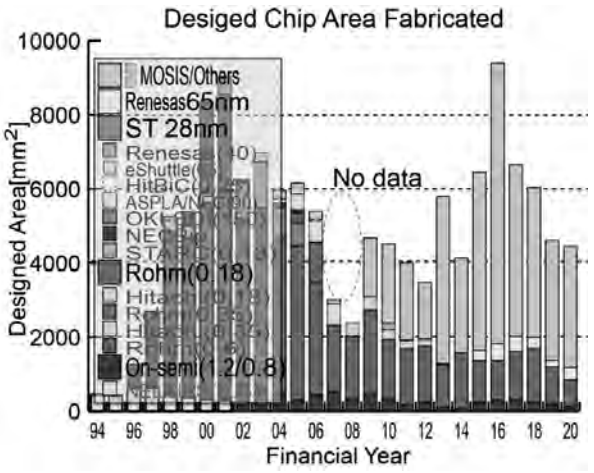
Fig.A.1.2

A.2 Status of Chip Fabrication Support at Platform Design Research Division

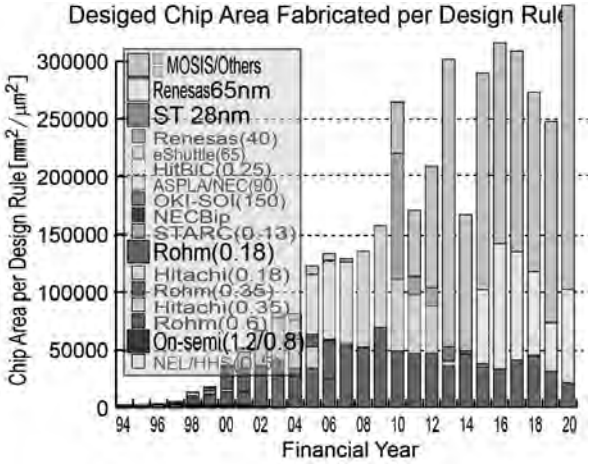
As for the support for VLSI chip prototyping, in the pilot project in FY 1994 and 1995, there was only one foundry, NEL's CMOS 0.5μm (the process was later continued by Hitachi Hokkai Semiconductor). After the inauguration of VDEC in 1996, the 1.2-μm CMOS process of Motorola Japan (which was continued by ON Semiconductor in 1999) started cooperation, and the 0.6-μm CMOS process of ROHM was added in 1997. In 1997, CMOS 0.6μm from ROHM was added, followed by 0.35μm from Hitachi, Ltd. in 1998, and 0.35μm from ROHM in 1999. In addition, as part of the IP development project, a prototype of STARC 0.13μm was developed. Since FY 2001, we have been providing services of CMOS 0.18μm from Hitachi, Ltd. In 2002, under the leadership of Dr. Iwata of Hiroshima University, we conducted a trial trial fabrication service in cooperation with VDEC and MOSIS. This service provides overseas fabs such as TSMC and IBM at low cost through MOSIS. Furthermore, under the leadership of Dr. Shibata of the University of Tokyo, NEC Compound Device, Inc. provided a prototype service for bipolar LSI. In 2004, we started prototyping Oki Electric CMOS SOI 0.15μm process and ASPLA 90nm process as test prototypes, and the 90nm prototype was operated as a regular prototype from 2005 in the form of public solicitation. In FY2006, we started trial production of 0.18μm process by ROHM and test production of 0.25μm SiGeBiCMOS by Hitachi, Ltd. In FY 2007, we started to study an advanced process to succeed 90nm CMOS, which was terminated in FY 2007, and in FY 2008, we started trial production of eShuttle's 65nm CMOS. In addition, as part of the METI-STARC project "Next Generation Semiconductor Circuit Architecture Commercialization Support Project," prototype production using Renesas Electronics' 40nm CMOS was also started. On the other hand, CMOS1.2μm was terminated in September 2011, Renesas Electronics' 40nm CMOS prototyping was terminated in 2012, and eShuttle's 65nm CMOS prototyping was terminated in August 2013. As a successor to CMOS 1.2μm, a test prototype of CMOS 0.8μm was conducted in October 2012 with the cooperation of Onsemi-Sanyo Semiconductor Manufacturing Co. As for the leading-edge prototyping, STMicroelectronics started FD-SOI 28nm CMOS



(a)Trend of number of designs fabricated.



(b)Trend of designed area



(c)Trend of designed area normalized by design rule.

Figure A.2.1 Trend of number of designs and designed chip area.b

prototyping through CMP of France in FY 2013. In addition, we started SOTB 65nm CMOS prototyping by Renesas Electronics as a regular prototyping in FY2015. In FY2020, we started to study BiCMOS 0.18um prototypes under an agreement with IHP of Germany.

Fig. A.2.1(a) shows trends of number of chip designed for VDEC chip fabrication. For the first 6 years until 2001, the number of designed chips shows steady increase, which means drastic improve of the effectiveness researches and education of LSI design, and we assume drastic increase of number of students related to LSI chip design and education. During few years of stable number around 400 chip designs per year, we can see transition of designs toward finer process. In 2007, we saw a large drop, which was caused by sudden process transition from 0.35μm CMOS to 0.1μm CMOS, and in 2008, we also saw another drop by process transition from 90nm CMOS to 65nm CMOS.

Fig. A.2.1(b) shows trends of designed chip area, which shows much clear trends of drop by process migration. On the other hand, Fig. A.2.1(c) shows trends of designed chip area normalized by design rule, which assume to be strong relation with design efforts. Coming from the fact that the normalized chip area is still growing, we assume the major reason for decrease of number of chips and designed area is increase of design effort per chip and per unit area due to process scaling.

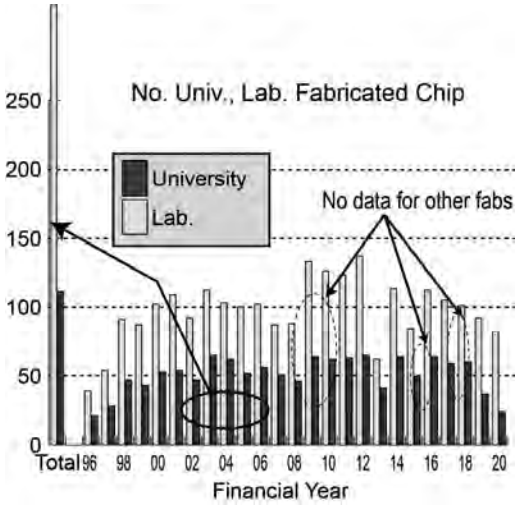


Figure A.2.2 Trend of number of processors and universities fabricated chip.

Table A.2.1 Chip fabrication schedule in 2020

○0.8μm CMOS (On-Semiconductor - Sanyo)

	Chip application deadline	Design deadline	Chip delivery
2020 #1	2020/7/6	2020/9/28	2020/12/17
2020 #2	2021/1/12	2021/3/29	2021/6/28

○0.18μm CMOS (Rohm)

	Chip application deadline	Design deadline	Chip delivery
2020 #1	2020/3/16	2020/6/8	2020/10/6
2020 #2	2020/6/15	2020/9/7	2020/12/8
2020 #3	2020/8/3	2020/10/26	2021/2/2
2020 #4	2020/11/30	2021/2/22	2021/6/4

○SOTB 65nm CMOS

	Chip application deadline	Design deadline	Chip delivery
2020 #1	2020/8/3	2020/8/24	2021/2/16
2020 #2	2021/1/25	2021/3/8	2021/9(est.)

A.3 Seminar

Seminars are always needed as the advancement of LSI design technology. In 2020, VDEC has held CAD Seminar, Refresh Seminar, and Designer's Forum, for academic and industrial circuit designers. In this fiscal year, all the seminars were held online due to the pandemic of COVID-19.

A.3.1 CAD Seminar for VDEC users

Along with advancement of circuit design CAD tools, tutorials on these tools are highly demanded. VDEC offers the CAD Seminar twice per year. In the CAD Seminar, VDEC invites lecturers from venders including Cadence, Synopsys and Keysight to give tutorials on their CAD tools. The seminar is held in VDEC, The University of Tokyo and VDEC sub-centers simultaneously in several universities nationally, August, September, and March of one fiscal year. Each tutorial takes one or two days.

Table A.3.1 CAD technical seminar in 2019 fiscal year

CAD Seminar I

Date	Tutorial	Venue	Attendees
8/11	Keysight Empro	Online	14
8/19, 19	Synopsys IC Compiler-II	Online	27
8/25	Synopsys IC Validator	Online	19
8/27, 28	Cadence Virtuoso Schematic, Layout	Online	74
9/1	Synopsys Custom Designer	Online	18
9/4	Cadence Innovus	Online	24
8/11	Keysight Empro	Online	14
8/19, 19	Synopsys IC Compiler-II	Online	27
8/25	Synopsys IC Validator	Online	19

CAD Seminar II

Date	Tutorial	Venue	Attendees
3/18	Cadence Innovus	Online	35
3/19	Synopsys SiliconSmart	Online	16
3/24	Cadence SpectreRF	Online	50
3/25	Cadence Quantus	Online	34
3/26	Synopsys Q&A Meeting	Online	14
Until 3/31	Synopsys Formality	On-demand	95
Until 3/31	Synopsys Design Compiler	On-demand	113
Until 3/31	Synopsys IC Compiler-II	On-demand	114

A.3.2 Refresh Seminar for industry and academia

The fundamental and advanced knowledges are both imperative to integrated circuit design. VDEC offers the Refresh Seminar for industrial and academic people. University professors and highly experienced engineers are invited to give lectures on circuit design, covering the topics on analog, digital, RF, MEMs, and basic design flow. The seminar was originally launched in 1998, with the support of Ministry of Education Technical Education Division. It is now being supported by several industrial/ academic societies.

Fig. A.3.1Refresh Seminar at VDEC seminar room at the University of Tokyo, VDEC.

Fig. A.3.2 Screen shot of Refresh Seminar online.

Table A.3.2 Refresh Seminar

Date	Course	Contents	Lecture	Attendees
6/23, 24	VDEC Digital Circuit Design Flow	Digital circuit design flow using VDEC-collaborated CAD environment and process	Kazutoshi Kobayashi (Kyoto Institute of Technology)	36
7/6, 7, 8	Analog Circuit Design	Analog Circuit Design and simulation Integrated Circuits Verifica-tion (LVS, DRC)	Masahiro Sugimoto (Chuo Univ.) Hidetoshi Onodera (Kyoto Univ.) Koji Kotani (Tohoku Univ.)	48
7/20, 21	CMOS-RF Circuit Design	Modulation/Demodulation Cascaded connection Basic Performance Transceiver Architecture Circuit Element Design Flow	Hiroyuki Ito (Tokyo Inst. of Tech.)	12
8/20, 21	Transistor-Level Circuit Design Flow	Custom circuit design flow using VDEC-collaborated CAD environment and process	Toru Nakura (Fukuoka Univ.)	27
9/7, 8	MEMS Design VDEC	Custom circuit design flow using VDEC-collaborated CAD environment and pro-cess MEMS Basic 1: Fabri-cat-ion Process MEMS Basic 2: Operation Principle Structural Design Layout Design	Yoshio Mita (The Univ. of Tokyo)	2
9/14, 15, 16	MEMS Fabrication	CAD Design and Analysis Lithography, Etching, Release Vibration measurement and analysis	Yoshio Mita (The Univ. of Tokyo)	1

A.3.3 Matlab Seminar for industry and academia

Collaborating with Mathworks Inc., we successfully held a seminar named "Improving development efficiency for FPGA/ASIC using Matlab/Simulink". The attendee number is 27. Using fruitful documents and design resources provided by Mathworks Inc, we were being tutored about translating Simulink block diagram to HDL automatically during the 4-hour seminar.

A.3.4 Designer's Forum for academia

VDEC LSI designer forum intended for students and young teachers were held. The VDEC LSI designer forum has aimed to sharing the information that generally hard to be obtained common technical reports or academical papers, such as the failure an LSI designer had been through and the solution, and the construction method in the design milieu in the laboratory.

Table A.3.3 Program of Designers Forum in 2020

Table B.3.5 Program of Designers Forum in 2020	
9/25	
12:00-12:45	Reception
12:45	Opening
13:00-14:00	Keynote Speech
14:00-14:10	Break
14:10-15:50	VDEC Design Award Presentation I
9/26	
13:00-13:50	Idea Contest Presentation
13:50-14:00	Break
14:00-14:50	Idea Contest Presentation
14:50-15:00	Voting
15:30-	Awarding Ceremony and Closing

A.4 Venture companies related to VDEC

Some professors related to VDEC started venture companies. The following is a list of the venture companies related to VDEC.

[1] AIL Co.,Ltd. (http://www.ailabo.co.jp/)

Related professor : Professor Kazuo Taki, Kobe Univ. (Representative Director)

Description of business : (1) LSI design service
(2) Engineer dispatching service

[2] Synthesis Corporation

(Merged with Soliton Systems on July 1st in 2017, http://www.synthesis.co.jp/)

Related professor : Professor Emeritus Isao Shirakawa, Osaka Univ. (Director)

Description of business : (1) System LSI development and design service
(2) IP development and sales
(3) Development and sales of IPs
(4) Development of EDA tools

[3] ASIP Solutions (http://www.asip-solutions.com/)

Related professor : Professor Masaharu Imai (Representative Director, CTO)

Description of business : (1) R&D, education and consulting of IoT application system
(2) Sales of ASIP design tool and consulting of ASIP development

[4] Nanodesign Corporation (http://www.nanodesign.co.jp/)

Related professor : Professor Kazuyuki Nakamura, Kyushu Institute of Technology. (Rep-resentative Director)

Description of business : (1) LSI design and development
(2) Design consulting, etc.

[5] A-R-Tec Corp. (http://www.a-r-tec.jp/)

Related professor : Professor Emeritus Atsushi Iwata, Hiroshima Univ. (Representative Director)

Description of business : (1) Design and measurement of IC and evaluation board
(2) Crosstalk noise analysis
(3) Develop human resources for new employees and beginners

[6] Ishijima Electronics (http://ishi.main.jp/)

Description of business : (1) Electronic circuit and board development
(2) Software development
(3) Consulting

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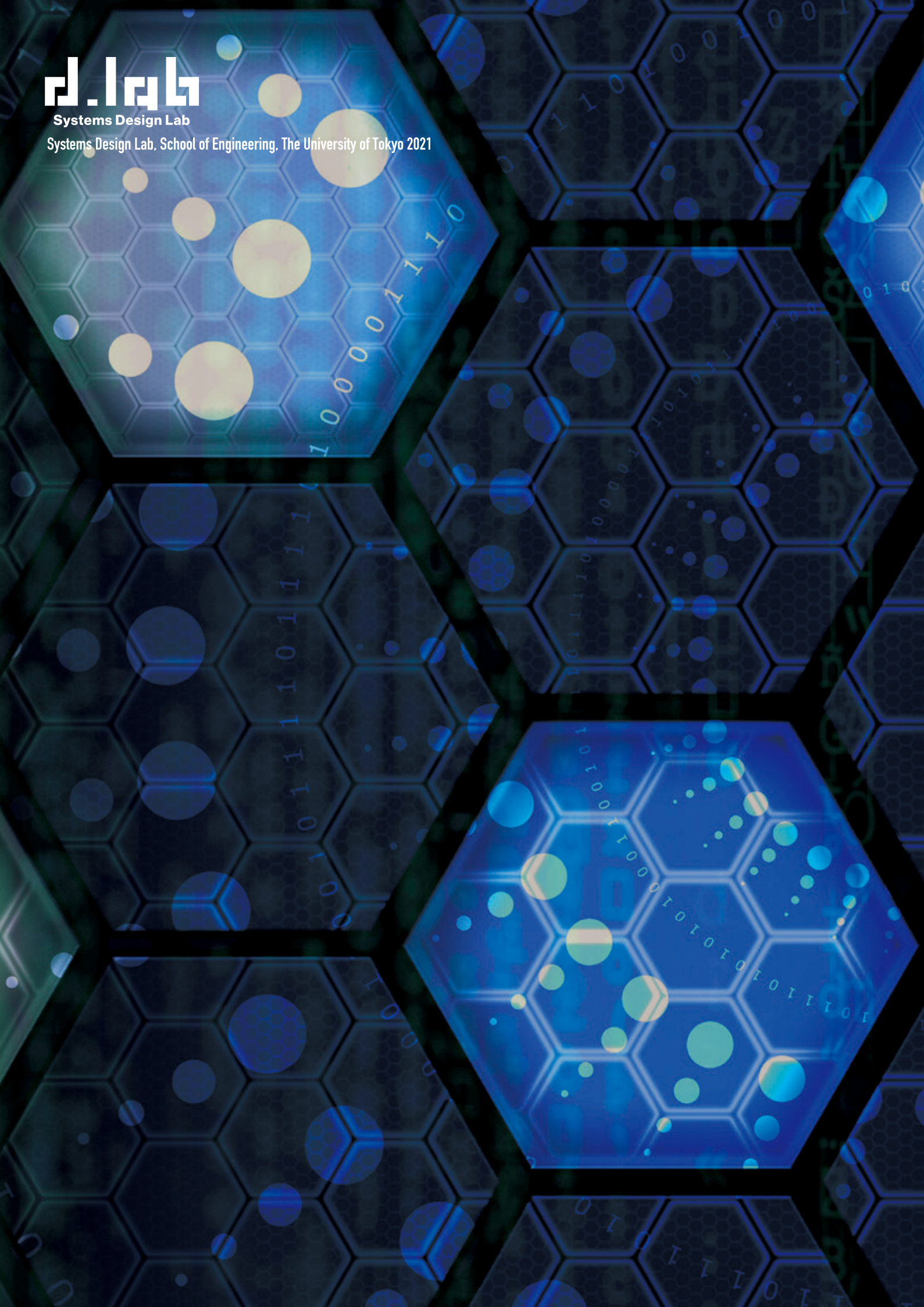

Systems Design Lab, School of Engineering, The University of Tokyo 2021