Systems Design Lab

東京大学大学院工学系研究科
附属システムデザイン研究センター
先端設計研究部門・先端デバイス研究部門
(旧VDEC)基盤設計研究部門・基盤デバイス研究部門

年　報

令和４年度

2022

Systems Design Lab, School of Engineering, (VLSI Design and Education Center), The University of Tokyo

Annual Report

Systems Design Lab, School of Engineering
The University of Tokyo 2022

Message from the Director of d.lab

Tadahiro Kuroda

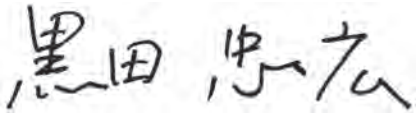
Director
Systems Design Lab (d.lab)
School of Engineering, The University of Tokyo

In February of this year, the Ministry of Education, Culture, Sports, Science and Technology (MEXT) issued a call for proposals under their「次 世 代X-nics半 導 体 創 成 拠 点 形 成 事 業」(Translation: Initiative to Establish Innovation Centers for Next-Generation X-nics Semiconductors). Their ultimate goal is the creation of groundbreaking, neXt-generation, novel semiconductors through multi-disciplinary synergy (multiplication "X"), much like the creation of various functional devices from spintronics and photonics, novel computing technologies from neurophysiology and quantum mechanics, and integrated devices from novel materials based on topotronics.

Regardless of the specific form of the novel semiconductor, a key requirement is the improvement of energy efficiency. In the last decade, while the amount of AI processing skyrocketed by 4 orders of magnitude, the energy efficiency of general-purpose processors increased by only an order of magnitude. This has driven platform providers such as GAFAM to develop their in-house specialized chips to achieve high energy efficiency. However, the development of specialized chips requires increasingly more time and higher cost. Given the rapid advance in AI technology, if it takes a year to develop a specialized chip, it is already obsolete by the time the development is complete. The strategy for growth in the DX age requires rapid iteration (being agile) of the development-improvement cycle. This can be achieved if LSI chips are designed the way software is written and prototyped the way a program is compiled to make them updatable like software.

A related question is how to accelerate technology innovation. The answer can be found in the idea of a collective brain expounded by Joseph Henrich, Professor of Human Evolutionary Biology at Harvard University. The bigger the collective brain is, the easier it is to accelerate technology innovation. For instance, through research conducted on various Pacific islands, the paper "Population Size Predicts Technological Complexity in Oceania" found a correlation between the size of variation in fishing tools and the population of the island. The reason that, even with a smaller brain than Neanderthals, Homo sapiens were able to invent and utilize various tools is also thought to be due to their integration into large groups. The internet has enabled a giant collective brain of 7.7 billion people. A platform that attracts many people will turn into a center for accelerated technology innovation.

We at d.lab proposed an "Agile-X Center for Democratization of Innovative Semiconductor Technology." Our target is a 10-fold increase in the population of chip designers. To that end, we will create an agile development platform to reduce both the time and cost for chip development and prototyping by an order of magnitude. During the application process, we were asked by the X-nics review committee what X stands for. We answered that it is the unknown of "what" innovation will change the world. Nevertheless, we know "where" the innovation will come from. That is the platform where a large population of people congregate. I am pleased to say that our proposal has been accepted. I believe that, in addition to More Moore and More than Moore, More People will accelerate the creation of intellectual value.



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2022
Systems Design Lab, School of Engineering,
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The University of Tokyo
Annual Report

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Chapter1 Introduction to d.lab

The VLSI Design and Education Center (VDEC) was established at the University of Tokyo in 1996. At the time of its founding, Japan's semiconductor industry held a 50% share of the USD 50-billion global market, and engineers who could hit the ground running were in high demand. VDEC has since provided unparalleled, outstanding education to develop many high-caliber engineers for the semiconductor industry.

However, have these graduates of VDEC been able to fully realize their potential? In the last quarter century, even though the global semiconductor market enjoyed a rapid 7% annual growth rate, Japan's share continued to shrink, falling to the current level of about 10% of a market that is now approaching USD 500 billion.

The current semiconductor business is one of mass production of high volume, low margin general purpose chips. General purpose chips have been able to achieve large volumes because of the wide adoption of the von Neumann computer architecture constructed with the combination of memory and processor chips. While Japan led the world in memory device innovation, it lost the business competition on capital investment.

The mass production, mass consumption model has its limits. Because of the excessive burdens it places on the environment, the world is now facing an energy crisis. The recent trend of applying AI to big data analysis is fueling further growth in energy consumption.

In the middle of this development, a game changer has emerged. Recognizing that it is hard to compete by using general purpose chips procured from semiconductor makers, technology giants including GAFA have started to develop their own specialized logic chips in-house.

In response to this paradigm shift, the University of Tokyo established the Systems Design Lab (d.lab) in October of 2019 and formed a strategic alliance with TSMC a month later. d.lab was formed by establishing the Advanced Design Research Division and the Advanced Device Research Division and adding them to the existing Platform Design Research Division and Platform Device Research Division which had been operating VDEC and the Takeda Clean Room. Subsequently in October of 2020, d.lab started an industrial partnership program which has grown to include more than 40 corporate members.

Furthermore, the Research Association for Advanced Systems (RaaS) was founded in August of 2020 to lay out the framework for the university to collaborate with both the industry and the government. Using d.lab and RaaS to realize a two-pronged strategy of open and closed collaboration respectively, the university is actively promoting cooperation between academia and society as well as collaborative creation with industry. Our research aims to boost the time-performance of semiconductors, with target goals of 10x increase in both energy and development efficiencies.

Japan is aiming to transition from the current industrial/information society to Society 5.0, a human-centric society where knowledge is value. In this knowledge-based society, semiconductors will evolve from being a necessity of industry to the brain cell of society.

What strategy should the semiconductor industry pursue to address this evolution? It is d.lab's mission to find the answer.

Chapter2 Activity Report of d.lab

2.1 Advanced Design Research Division

2.1.1 Division Overview

The Advanced Design Research Division faculty consists of four professors, one associate professor, one lecturer, one project professor, and one senior fellow (joint appointment included). Its goal is to enable the design of integrated circuits with both high energy efficiency and high design efficiency.

In July 2021, NEC Corporation and the University of Tokyo were selected to lead the research and development of a new computing mechanism to accelerate data structure processing, as part of a pilot study to identify R&D challenges for the Project for Innovative AI Chip and Next-Generation Computing Technology Development of the New Energy and Industrial Technology Development Organization (NEDO). The research is scheduled to complete by the end of June 2022.

In addition to its research effort, the Advanced Design Research Division has two organizational responsibilities. First, it operates the d.lab Partnership Program with help from other d.lab divisions. Second, it founded and operates the Research Association for Advanced Systems. The following section is the FY2021 report on these two operations.

2.1.2. d.lab Partnership Program Activities

The d.lab Partnership Program was launched in FY2020 to establish an international center of knowledge-value where system designers and members of the semiconductor industry meet to exchange information and ideas and to engage in open discussion of collaboration between academia and society. The Program aims to create a hub that brings together ideas from system designers in industries including IoT, AI, 5G, automated driving, and healthcare, advanced semiconductor technologies such as advanced CMOS processes and 3D integration technologies, as well as enablers of such technologies including materials and manufacturing equipment. For FY2021, a total of 43 corporations joined the Program. Table 2.1.1 contains the list of FY2021 corporate members. We would like to thank these members again for their participation.

As noted in our last annual report, our original vision was to not only create a platform for the dissemination of the research accomplishment of d.lab, but also to turn our Mejirodai campus into a new venue for interaction and learning. We were planning to host various events to enable program members to interact with renowned professors and students at the University of Tokyo, with universities and research organizations from around the world, and with other industrial executives and leaders, as well as events to share information and knowledge from international conferences and introduce and assess the most advanced technologies from the likes of TSMC. Unfortunately, same as in FY2020, because of COVID-19, we were forced to once again center our activities in FY2021 around seminars held in the form of webinars. Our activities spanned almost the entire year from May 2021 to March 2022. Table 2.1.2 summarizes the seminars we held in FY2021.

We held our program kickoff meeting on May 19, 2021 which also featured a keynote presentation. With 5G service having been rolled out in Japan as well, the focus of R&D in the country has been shifting to Post/Beyond 5G. Professor Akihiro Nakao of the School of Engineering, University of Tokyo, who has led Japan's 5G technology development, discussed what lies ahead beyond 5G and the role semiconductor will play in a talk entitled "The Direction of Beyond 5G/Post 5G R&D and What We Can Expect from Semiconductor Development." He was followed by Professor Tadahiro Kuroda, Director of d.lab, who provided an overview of d.lab and introduced the d.lab Partnership Program activities in FY2021 together with their schedule.

On Jun 29, we held a seminar to report on the 2021 VLSI Technology/Circuit Symposia which took place from Jun 13 to 19 earlier in the year. We reported on the circuit, system, process, and device technologies presented at the Symposia. We also invited the Small and Medium Enterprise Agency to the seminar to introduce the support program aimed at promoting the semiconductor industry.

On Jul 21, we hosted another seminar to report on the

2021 IEEE 71st Electronic Components and Technology Conference (ECTC 2021). The conference is organized by the IEEE Electronics Packaging Society to provide a forum for wide ranging discussion of the science and technology of packages, components, and microelectronic systems. It is one of the world's long-established and leading international conferences, held for the 71st time last year. The technology program covered the latest achievement in development across the full spectrum of packaging technology. Its main topics included advanced packaging, modeling and simulation, photonics, interconnection, material and process, reliability, manufacturing technology, components and RF, as well as emerging technologies. In our report, we focused on the latest trends and topics in advanced packaging, which is a mainstream technology for our current activities, and hybrid bonding, which is a next-generation core technology. The seminar was preceded by an announcement of the "VDEC Refresh Seminar for Engineers, Course M" by Associate Professor Yoshio Mita.

On Aug 18, we held our first technology exchange meeting for our corporate partners, where some of our partners presented on their differentiating technologies and expectation for future technology exchange. Presentation was made by six of our partners - Ushio Inc., Analog Devices, Inc., Showa Denko Materials Co., Ltd., KIOXIA Corporation, Semiconductor Energy Laboratory Co., Ltd., and Toppan Inc. The goal of the technology exchange meeting is to promote collaboration between our corporate partners and with d.lab faculty members and students.

On Sep 22, the second installment of the technology exchange meeting was held. The six presenting corporate partners were Dai Nippon Printing Co., Ltd., Alchip Technologies, Limited, Gigaphoton Inc, Nikon Corporation, DISCO Corporation, and Organo Corporation.

On Nov 17, we held a special seminar "Gastronomy, Robotics, and Semiconductor" in conjunction with the third installment of the technology exchange meeting. For the keynote presentation, Mr. Masahiro Fujita of Sony Group Corporation described the future that could be realized with the advance in semiconductor, AI, and robotics. From a novel perspective of gastronomy, he discussed his research on using AI and robots to expand human creativity. The keynote was followed by the presentations of TOKYO OHKA KOGYO CO., LTD. and Renesas Electronics Corporation in the third installment of our technology exchange meeting.

On Dec 17, we organized an imec Day event where we heard directly from executives in charge of R&D at imec, which leads the world in the research and development of ever advancing, ultra-high performance silicon systems. The speakers introduced their efforts in extending CMOS device scaling and development of the most advanced 3D system integration process and device technologies. It was an excellent opportunity for the audience to receive firsthand information on the most advanced silicon system technologies. Dr. Naoto Horiguchi, imec Program Director of Logic CMOS Device, discussed "CMOS device scaling options toward N1 and beyond," while Dr. Eric Beyne, imec Senior Fellow, VP R&D, and Program Director of 3D System Integration, presented on "A 3D Integration Future: enabling continued system-level electronic scaling."

The theme of our seminar on Dec 22 was TSMC Day. TSMC (Taiwan Semiconductor Manufacturing Company, Ltd.), headquartered in Hsinchu City of Taiwan, is the world's largest and most advanced semiconductor foundry. The company established the TSMC Japan 3DIC R&D Center in Japan in 2021. It is without question that, in addition to semiconductor scaling to achieve More Moore technology innovation, 3DIC technology, which realizes More Than Moore technology innovation, is key to the future of the semiconductor industry. Center Director Emoto and Technical Director Ichikawa presented the mission of the R&D center in "Overview and initiatives of TSMC Japan 3DIC R&D Center." They also provided an update on the latest technology development in the company.

At the beginning of the year on Jan 19, 2022, we held a seminar to report on IEDM2021. IEDM (International Electron Devices Meeting) is the world's top international conference on device technology organized by IEEE. The conference was held in a hybrid format – allowing both in-person and on-demand attendance – from Dec 11 to 15. In our meeting, faculty members from d.lab provided a summary of the conference and discussed the latest trends in device technology, focusing on advanced CMOS device technology and material, non-volatile memory technology, computing technology, and 3D integration technology.

On Mar 2, we organized a d.lab Day event which provided a forum for the first time in the d.lab Partnership Program for d.lab faculty members to introduce their research activities. The event was held in response to interest expressed by our partners in learning about the research of our faculty members, a year and a half after the program started. It is hoped that the seminar will stimulate new activities such as collaborative research.

As the last event of our FY2021 seminar series, we held a meeting on Mar 23 to report on the 2022 International Solid-State Circuits Conference (ISSCC2021). ISSCC is the top international conference on IC technology held in February. Starting with Professor Makoto Ikeda who has been for years the chair of ISSCC's technology program, faculty members from d.lab discussed the latest trends seen in the conference in the thriving area of machine learning processors, ICs enabling emerging computing technologies exemplified by quantum computing, as well as 5G, AI, and game console ICs which are expected to drive the future of the semiconductor market.

For FY2022, we are considering organizing a mix of remote seminars and in-person events, while carefully monitoring the development of COVID-19. In addition to incorporating first-time events in our plan, we would like to continue to promote intellectual exchange between our partners and the university, and among our partners themselves.

2.1.3 Research Association for Advanced Systems Activities

With preparation that started in FY2019, the Research Association for Advanced Systems (RaaS) was established on Aug 17, 2020. The founding members are the University of Tokyo, Toppan Inc., Panasonic Corporation, Hitachi, Ltd., and MIRISE Technologies. The goal of RaaS is to increase 10-fold the development efficiency of specialized chips, which are indispensable in a data-driven society, by constructing a design platform for such chips and by adopting an open architecture for hardware design. In addition, RaaS aims to increase 10-fold energy efficiency by researching and developing 3D integration technology and by stacking multiple chips manufactured in the latest 7nm CMOS technology in a single package.

At RaaS, we believe that the driver of the semiconductor industry is once again swinging back from general purpose to specialized chips, against the backdrop of the unique energy crisis of the data society. The crisis is being spurred by the exponential growth in data and the increasing sophistication of AI processing. On the current trajectory, IT equipment alone is expected to consume close to twice the total available power of today by 2030, and about 200 time the total available power of today by 2050. It will be impossible to realize a sustainable future if digital transformation will consume so much energy as to destroy the earth's environment.

Under such a condition, only those who can improve energy efficiency 10-fold can afford to increase computer performance 10-fold, or extend smartphone use 10-fold. Compared to general purpose chips which are required to handle all tasks, specialized chips achieve orders-of-magnitude improvement in energy efficiency by eliminating unneeded circuits. That is why specialized chips are in demand. In addition, since AI processing utilizes neural networks which process data in parallel, it is difficult for von Neumann architecture which is designed for sequential processing to deliver adequate performance. As a result, specialized chips are being developed around the world to serve as AI accelerators. Furthermore, the slowing of Moore's Law is also providing a tailwind for specialized chips.

Unfortunately, specialized chips development requires special skills and cannot be easily undertaken by everyone. The latest chips integrate more transistors than there are people in the world. Development costs have skyrocketed in recent years to approach $100 million. It will take even a team of several hundred designers several years to develop a specialized chip, which makes it difficult to keep pace with today's rapid technological advance.

In software development, bugs can be patched after the fact. But hardware cannot be shipped unless it is completely error-free. Compared to software, hardware development is indeed hard and carries more risk.

If technologies similar to compilers used in software development are available to chip development, in other words, if silicon compilers become a reality, we can expect both hardware development cost and risk to drop. In addition, more people can become hardware designer. Eventually, as the open source culture takes root in hardware development and the supporting ecosystem expands and develops into a multi-layer network, mass collaboration

will become possible. When that happens, one will be able to develop chips like writing software.

Alan Kay once said that "People who are really serious about software should make their own hardware." Indeed, system development requires both hardware and software development.

Our goal at RaaS is to democratize access to silicon technology. We aim to create a development platform to realize agile authentic prototyping where prototypes can be created rapidly by innovating silicon compiler technology to enable designing chips like writing software.

Our technology goal is a 10-fold increase in both development efficiency and energy efficiency. We plan to improve development efficiency by creating an agile design platform and adopting an open architecture. In addition, we aim to increase energy efficiency through manufacturing chips in the most advanced CMOS process and implementation of 3D integration.

We provide semiconductors as a service, rather than sell them as a product. It is the role of RaaS to develop the necessary technologies to achieve that goal.

RaaS has planned to bring researchers from member companies together at the Mejirodai International Village campus of the University of Tokyo where they can conduct research while providing stimulation to each other. Unfortunately, because of COVID-19, RaaS activities have also been limited to center around remote work.

In FY2021, RaaS applied to and was accepted by the "Project for Research and Development of Enhanced Infrastructures for Post 5G Information and Communications Systems / Development of Advanced Semiconductor Manufacturing Technology (b) Development of Advanced Semiconductor Backend Processing Technology (More than Moore)" of the New Energy and Industrial Technology Development Organization (NEDO). The development theme is "(b2) Implementation Technology for Edge Computing." As a result, we were joined by SCREEN Holdings Co., Ltd., DAIKIN INDUSTRIES, Ltd., FUJIFILM Corporation, and Panasonic Connect Co., Ltd. as new members of RaaS, adding technology R&D to the system R&D which we have been pursuing from the beginning.

In the system R&D, RaaS completed the design of and taped out our first chip in the 7nm process in FY2021. It is our biggest accomplishment of the year where we were able to complete the design and prototyping of a chip using the latest CMOS technology with complicated design rules in less than a year since our inception.

In the technology R&D, based on the NEDO project mentioned above, our efforts have been focused on the establishment and implementation of technology for WoW (wafer-on-wafer) and CoW (chip-on-wafer) integration using Cu-Cu low temperature bonding as part of our direct bonding 3D integration technology development (equipment and process development for WoW and CoW).

Table 2.1.1 List of FY2021 d.lab Partner Members (in Japanese phonetic order)

Advantest Corporation
Analog Devices, Inc.
Alchip Technologies, Limited
Ushio Inc.
Organo Corporation
KIOXIA Corporation
Gigaphoton Inc
Samsung R&D Institute Japan
Siemens EDA Japan
JSR Corporation
Showa Denko Materials Co., Ltd.
Shin-Etsu Chemical Co., Ltd.
SCREEN Holdings Co., Ltd.
Sumitomo Corporation
Socionext Inc.
Sony Group Corporation
DAIKIN INDUSTRIES, Ltd.
Dai Nippon Printing Co., Ltd.
TDK Corporation
DISCO Corporation
Tokyo Electron Limited
TOKYO OHKA KOGYO CO., LTD.
Toppan Inc.
Nikon Corporation
IBM Japan, Ltd.
Cadence Design Systems, Japan
Nihon Synopsys G.K.
JEOL Ltd.
Panasonic Corporation
Panasonic Smart Factory Solutions Co., Ltd.
Semiconductor Energy Laboratory Co., Ltd.
Hitachi, Ltd.
Fujitsu Limited
FUJIFILM Corporation
Micron Memory Japan, K.K.
Mitsubishi Chemical Corporation
Mitsubishi Electric Corporation
MIRISE Technologies
Miraxia Edge Technology Corporation
Murata Manufacturing Co., Ltd.
Renesas Electronics Corporation
ROHM Co., Ltd.

Table 2.1.2 List of FY2021 d.lab Partnership Program Seminars

Date	Title	Presenter(s)
5/19/2021	FY2021 d.lab Partnership Program Kick-off & Special Keynote	Prof. Akihiro Nakao, School of Engineering Prof. Tadahiro Kuroda, d.lab
6/29/2021	Business Restructuring Grant Program 2021 VLSI Symposia Report	Mr. Kento Tsuda, Deputy Director, Small and Medium Enterprise Agency, METI Prof. Ken Takeuchi, d.lab Prof. Makoto Ikeda, d.lab Mototsugu Hamada, Project Prof., d.lab Prof. Toshiro Hiramoto, d.lab Prof. Shinichi Takagi, d.lab Masaaki Niwa, Senior Fellow, d.lab
7/21/2021	Seminar Announcement ECTC 2021 Report	Yoshio Mita, Associate Prof., d.lab Toru Ogawa, RaaS Advisor Takeshi Takagi, Principal Researcher, d.lab Tadatomo Suga, RaaS Advisor Masaaki Niwa, Senior Fellow, d.lab
8/18/2021	d.lab Partners Technology Exchange (1)	Mr. Takafumi Mizojiri, Ushio Inc. Mr. Shogo Arita, Analog Devices, Inc. Mr. Takahiro Tanabe, Showa Denko Materials Co., Ltd. Mr. Takaya Ogawa, KIOXIA Corporation Mr. Haruyuki Baba, Semiconductor Energy Laboratory Co., Ltd. Mr. Tatsuo Noguchi & Mr. Keiichiro Uchida, Toppan Inc.
9/22/2021	d.lab Partners Technology Exchange (2)	Mr. Koji Ichimura, Dai Nippon Printing Co., Ltd. Mr. Hiroyuki Furuzono & Mr. Eijiro Sasa, Alchip Technologies, Limited Mr. Kenji Oishi, Gigaphoton Inc Mr. Yuta Komatsu, Nikon Corporation Mr. Shunsuke Teranishi, DISCO Corporation Mr. Hiroshi Sugawara, Organo Corporation
11/17/2021	Special Technology Seminar “Gastronomy, Robotics, and Semiconductor” d.lab Partners Technology Exchange (3)	Mr. Masahiro Fujita, Sony Group Corporation Mr. Satoshi Fujimura, TOKYO OHKA KOGYO CO., LTD. Mr. Hirotaka Hara, Renesas Electronics Corporation

12/17/2021	imec Day	Dr. Naoto Horiguchi, imec Dr. Eric Beyne, imec
12/22/2021	TSMC Day	Mr. Yutaka Emoto, TSMC Japan Mr. Kinya Ichikawa, TSMC Japan
1/19/2022	IEDM2021 Report	Prof. Toshiro Hiramoto, d.lab Prof. Shinichi Takagi, d.lab Masaharu Kobayashi, Associate Prof., d.lab Prof. Ken Takeuchi, d.lab Takeshi Takagi, Principal Researcher, d.lab
3/2/2022	d.lab Day	Prof. Shinichi Takagi, d.lab Prof. Makoto Ikeda, d.lab Prof. Ken Takeuchi, d.lab Yoshio Mita, Associate Prof., d.lab Masaharu Kobayashi, Associate Prof., d.lab
3/23/2022	ISSCC2022 Report	Prof. Makoto Ikeda, d.lab Prof. Ken Takeuchi, d.lab Tetsuya Iizuka, Associate Prof., d.lab Mototsugu Hamada, Project Prof., d.lab Atsutake Kosuge, Lecturer, d.lab

2.2 Advanced Device Research Division

Advanced Device Research Division is working for the development of three-dimensional (3D) integration technology and advanced device technology aiming at ten times higher energy efficiency of semiconductor systems in the data-driven systems.

In 2021, we launched a new project of the next-generation 3D integration technology.

Recently, the computing technology for processing large amount of data is becoming more important and the energy consumption by frequent data transfer between memories and processors is a severe problem. To solve this problem, the direct bonding 3D stack technology, where the data transfer distance is shortened by direct bonding of chips or wafers, has attracted much attention.

This year, in the NEDO project "Post 5G Information and Communication Technology Infrastructure Reinforcement Research and Development Project / Development of Advanced Semiconductor Manufacturing Technology (Subsidy)", the Research Association for Advanced Systems (RaaS) which d.lab is the headquarters of technology research association on 3D integrated technology, proposed "Direct 3D Stacking Technology Development (Development of Equipment and Processes for WoW (Wafer on Wafer) and CoW (Chip on Wafer))", and this proposal was adopted. Currently, we are working with RaaS member companies to develop and implement chokepoint technologies related to WoW and CoW bonding technologies using low-temperature hybrid bonding of Cu-Cu.

2.3 Platform Design Research Division

2.3.1 Overview of Platform Design Research Division

Since its establishment in 1996, the VLSI Design and Education Center (VDEC) at the University of Tokyo has been developing projects that contribute to integrated circuit design education at universities and technical colleges in Japan, based on the three major roles: ”spreading the latest information on VLSI design and education,” ”providing licenses of CAD tools,” and ”supporting on VLSI chip fabrications for academic use.” On October 1, 2019, VDEC has been re-organized into Systems Design Lab (d.lab), Graduate School of Engineering, the University of Tokyo as part of an organizational restructuring aimed at strengthening integrated circuit related activities in the University of Tokyo's semiconductor integrated circuit-related activities. The Platform Design Research Division of d.lab continues to carry out the functions of the VDEC and continues “VDEC activities” seamlessly. Here, the outline of “VDEC activities” of the FY2021 is reported below.

The missions of VDEC are for advancement of researches and education on LSI design in public and private universities and colleges in Japan and send many distinguished VLSI designers into industry. After 25 years of VDEC establishment, educations on CAD software, LSI design and design flow in universities have been well established. On the other hand, advancement on nano-meter CMOS technologies forces design flow and CAD software complicated. We have been continuing CAD tool seminar by the lecturers from EDA vendors for twice a year. We hold the seminar in VDEC and provide distance learning through video streaming. We expect spread of the up-to-date LSI design methodology by using CAD tools.

In order to make it more convenient for the participants, the seminars have been held only in Tokyo since 2009, and at the same time, the seminars have been broadcasted to individual participating lab. The VDEC expects that the latest CAD use-case will be shared among labs through the seminar organized by VDEC, and will be a trigger to spread the technology nationwide. In FY2020, all seminars will be conducted online. Some items were conducted in the form of on-demand plus live Q&A sessions to improve the convenience of participation. In addition, in view of the current situation where the tool-chains of various companies are becoming more complex and it is difficult to fully use the introduced tools, lectures on the tool-chains recommended by each tool vendor were also held in conjunction with the individual tool seminars. From the end of FY2019, we received permission from each EDA vendor to use EDA tools from home, to avoid delay&slowdown in integrated circuit design research and education in Japan.

2.3.2 Status of Education at Platform Design Research Division

The LSI Design Flow Seminar is designed to educate the basic concepts of LSI design and to provide hands-on experience of practical design examples using multiple CAD tools. For this purpose, VDEC has been organizing LSI design education seminars as well as “Refresh Seminar” for re-education programs for engineers. “Analog Design Course”, and “RF Design Course,” were held from June to September. All of these courses are experiential education courses with exercises, and experienced instructors from major universities are invited as lecturers. In addition, “Transistor Level Design in VDEC Environment (Course VT)” and “Digital Design Methodology in VDEC EDA Environment (Course VD Course VT)” and “VDEC Digital Design Methodology Course (Course VD)” are conducted for designers in universities. The “Refresh Seminar” are all held online in FY2021, and as a result, the number of participants has increased compared to previous years.

In addition to these seminars, VDEC holds the “VDEC Designers’ Forum” once a year, mainly for young faculty members and students. This is a workshop-style meeting, where participants bring their design cases and exchange their successes and failures, in addition to invited lectures from companies and universities. In FY2021, the VDEC Designer Forum had been held online. Since FY2011, the “IEEE SSCS Japan Chapter VDEC Design Award” has been presented as an award for VDEC activities. The final judging and awarding of the “IEEE SSCS Japan Chapter VDEC Design Award” has been held at VDEC Designers’

Forum since 2011, and in 2021, the IEEE SSCS Japan Chapter VDEC Design Award will be presented to Mr. R. Okada of Nara Institute of Science and Technology. Three VDEC Design Award Excellence Awards, (Mr. R. Okada (Nara Institute of Science and Technology), Mr. A. Matsuoka(The University of Tokyo), and Mr. H. Sakai(Tokyo University of Science)), and three VDEC Design Award Encouragement Prizes (Mr. T. Tsujimura(Nagoya University), Mr. K. Sahara(Tokyo University of Science), and Y. Mori(Nara Institute of Science and Technology)), and three VDEC Design Award Commendation Prizes for Idea Contest (K. Kawahara(Tokyo University of Science), S. Mitsuno(the University of Tokyo), and T. Fukushima(Tokyo Denki University)).

Although the educational system through such seminars and forums has enabled students to learn the basics of LSI design, they still face various difficulties in actual LSI design situations. For beginners, setting up the CAD software is the biggest problem. Even after setting up the software, they are often baffled by the "difficult error messages" issued by the CAD software. VDEC users can register for the "CAD mail group" and the "Prototyping Technology User Group" on the VDEC website, where they can post their questions and ask for help. The registered users of the mail groups are not obligated to respond, but in most cases they can get help from experienced users within a few hours or days. We hope that you will take advantage of this system to help solve your problems.

2.3.3 Publications related to Platform Design Research Division

Figure 2.4 shows the use of the VDEC facility in the published literature related to VDEC. It can be confirmed that CAD software is widely used in writing papers. Since CAD software is often used not only in chip design but also in the preparation stage of chip prototyping, its contribution as a tool to demonstrate the basic idea of the research is also significant.

2.3.4 Report on AI Chip Design Center

VDEC and the AIST have been jointly commissioned by NEDO to develop a common platform technology for accelerating AI chip development under the "Innovation Promotion Project for Accelerating AI Chip Development / R&D Item 2: Development of Common Platform Technology for Accelerating AI Chip Development" since 2018. In this project, we have established an EDA utilization and design environment for venture companies and small and medium-sized enterprises(SMEs) in Japan, and are working as an "AI chip design center(AIDC)". In this activity, in addition to the introduction of EDA tool licenses that allow venture companies and small and medium-sized companies to prototype up to engineering samples, we have introduced IP for 40nm and 28nm, and are also providing a large-scale, high-speed design and verification environment using a hardware emulator, which was introduced with a subsidy from the Ministry of Economy, Trade and Industry at the start of this project. In FY2020, we have designed a SoC platform with NoC, PCIe, DDR4, etc., and multiple functional IP cores, and taped out the platform as a SoC with multiple AI IP cores designed by multiple users, and after almost 1-year delay, we have received assembled chip in the beginning of Jan. 2022, and after one week we could evaluate most of SoC functionalities and by the end of March 2022, almost all of Ips got fully verified. In order to further strengthen this activity, we are accelerating our research by establishing the "AIST-The University of Tokyo AI Chip Design Open Innovation Laboratory" (AIDL) in the Takeda Building, Asano Campus, The University of Tokyo on September 1, 2019.

Table 2.3.1 Chip fabrication schedule

【CMOS 1.2μm 2P2M】 On-Semiconductor(Former Motorola Japan)

	Chip application deadline	Design deadline	Chip delivery
2022#1	2022/7/4	2022/9/26	2022/12/19
2022#2	2023/1/10	2023/3/27	2023/6/26

【CMOS 0.18μm 1P5M(+MiM)】 Rohm

	Chip application deadline	Design deadline	Chip delivery
2022 #1	2022/4/4	2022/6/27	2022/10/14
2022 #2	2022/6/13	2022/9/5	2022/12/23
2022 #3	2022/8/1	2022/10/24	2023/2/11
2022 #4	2022/12/5	2023/2/27	2023/6/16

【SOTB CMOS 65nm】

	Chip application deadline	Design deadline	Chip delivery
2022 #1	2022/6/13	2022/7/25	2023/1/21
2022 #2	2023/1/23	2023/3/6	2023/8/26

2.3.5 Plan for FY 2022 "VDEC Activities" of Platform Design Research Division

In FY2021, we will continue the VDEC Activities for academics as before.

【Design related information dispatching/Seminar】

We will continue holding the following seminars: (1) CAD tools seminars which have been continued since 1997, (2) "Refresh seminar" since 1998, (3) "Designer' Forum" since 1997. We will also continue seminars for LSI tester usage at VDEC and sub-centers, workshops on LSI testing technologies initiated by D2T.

【CAD tool support】

We will continue Cadence tools, Synopsys tools and Mentor tools as the main stream design tools. We will continue analog RF design environment, GoldenGate and ADS by Agilent, C-based design environment, BachC by Sharp. In addition, we continue trial of several CAD tools, such as layout platform, Lavis by TOOL. Design debugging platform from SpringSoft has merged into Cadence tools and will be continued.

【Chip fabrication services】

We will continue chip fabrication services for 0.18 μ m CMOS by Rohm, 0.8 μ m CMOS by On-semiconductor-Sanyo, SOTB 65nm CMOS by Renesas Electronics, and IHP SiGeBiCMOS 0.18um as the regular services.

In addition to the above. We will continue to develop an "AIDC" activities, in collaboration with AIST. We will introduce a logic emulator for large-scale AI digital chip design verification, and maintain and operate EDA licenses for industrial applications. The main objective of this project is to provide small and medium-sized venture companies with a development environment for AI chip design, evaluation, and verification in order to accelerate the development of AI chips, but we also plan to improve the environment for use by universities in order to promote university-originated companies in the field of AI-related integrated circuits.

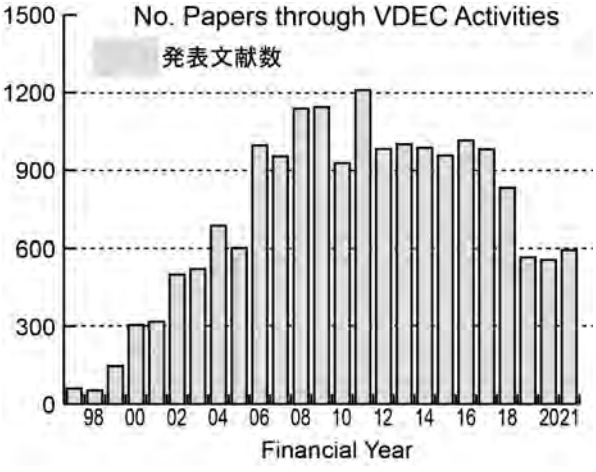

Fig. 2.3.1 Trends of number of papers through VDEC activities.

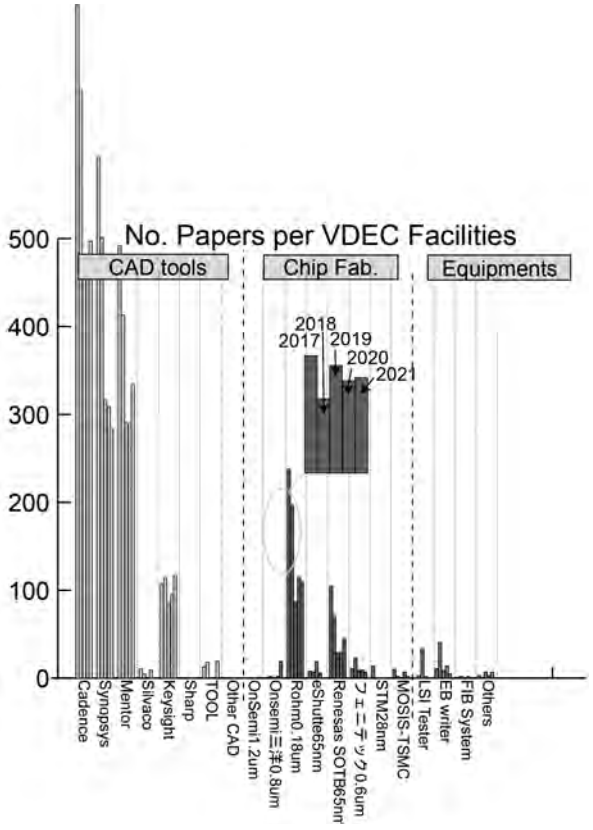

Fig. 2.3.2 Number of papers related to VDEC facilities.

2.4 Platform Device Research Division

2.4.1 Mission

D.lab platform device research division aims at providing every researcher with three essential elements for research on new devices. The division is with around 30 staffs, powered by Dr. Yoshio Mita, the playing division director who himself actively performs experiments in the Cleanroom as a leading researcher, and operated in collaboration with related departments (such as Institute of Engineering Innovation, Electrical Engineering and Information Systems, and Mechanical Engineering) in terms of human and budget resources. Especially in the year 2021, thanks to the invaluable help of Prof. Yuji Suzuki, vice dean for education, we could launch new subcontracting system to the Ph.D student as "excellent Ph.D", in order that they help the team by mentoring all junior members on behalf of experienced senior member in TakedaSCR. Research in emerging fields of semiconductor electronics devices (such as integrated circuits), sensors and microsystems requires three essential elements: (1) fabrication machines with stupendous amount of budget, (2) rich accumulation of fabrication technology knowledges, and (3) research capability to develop new technologies required for new devices. In Japan, these three elements had been prepared and kept in an individual research group until the end of 20th century. However, due to the technology trends towards advanced fabrication over larger-scale wafers, it has become almost impossible for a research group to purchase and maintain the cutting-edge fabrication machine line, in the 21st century. Originally, it was impossible for every research group in universities, companies, research institutes, and NPOs, to exclusively "own" such large-scale facility and necessary budget by themselves; If researchers wish to "cooperate" with the other researchers in a platform, which is equally open to everybody, they can "effectively own" the most advanced "open platform", and thereby the cutting-edge research activities can be held anywhere in Japan. This is the principle of d.lab's open device platform, which is in fact a lateral expansion of "shared economy model in VLSI design and fabrication" to micro-nano fabrication and measurement research field, originally established by VDEC for Japan in 1996.

Towards that end, d.lab Platform Device Research Division takes full advantages of spaces (of its own and of open rental) in Takeda Sentanchi Building. The building was inaugurated in December 2003, thanks to the enormous donation in 2001 from Mr. Ikuo Takeda (founder of Advantest) to the faculty of engineering (Dean was Professor

Fig2.4.1 Development of Takeda Sentanchi Supercleanroom

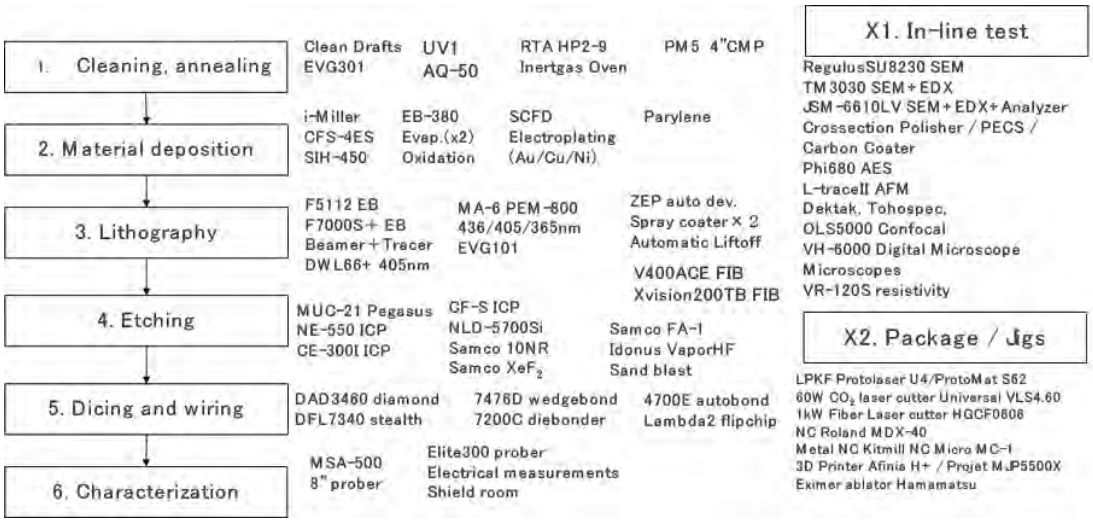

Fig.2.4.2 List of equipment under d.lab Platform Device Research Division

Hiroshi Komiyama) as well as VDEC (director was Professor Kunihiro Asada). In the building, a 600m^2-square supercleanroom including "official ISO3 (a.k.a. federal class 1. Once measured as ISO1)" area (Fig.1). The cleanroom and affiliated experimental rooms are equipped with cutting-edge nanofabrication and measurement machines, total valued over 3.9 billion yens (33M euros). The users can openly use such nice machines really inexpensively.

Over 70 apparatuses are openly accessible (Fig.2), including, "world's fastest" large-area direct electron beam (EB) writing machine Advantest F5112+VD01, which has been donated according to the wise decision of Mr Ooura, a chairman of Advantest, fine EB writer Advantest F7000S-VD02 and Silicon Deep Reactive Ion Etching machine SPTS MUC-21 ASE-Pegasus, both purchased by Japanese government's supplemental budget (known as Abenomics, the first arrow), and the scanning electron microscope (SEM) Hitachi Regulus SU8230 that provides highest-class resolution among those obtainable by research laboratory. The machines can cover most of the research steps in nanotechnology, which are cleaning, film deposition, lithography, etching, packaging and characterization. Not all apparatuses are yet installed in Takeda Building, however due to nationwide platform network, researchers can access in another equivalent nanofabrication platform center(s).

2.4.2 "Takeda Sentanchi Supercleanroom" cooperation platform

The platform is called "Nanotechnology Platform UTokyo Nanofabrication site" according to the MEXT's national project, or simply "Takeda Sentanchi Cleanroom" (in short, Takeda CR). The platform is widely open to those who share the "value of cooperation". The most important understanding for every user is the platform must not be considered as a simple outsourcing agent; being understood the value of "own help, mutual help, and public help", the participant can drastically minimize costs (personnel, budget, and time), which should have otherwise been totally covered by each researcher, and can directly jump into advanced research. Key Performance Indicators of such benefits are as follows: over 7.7 billion yens for installation cost of building and equipment, over 300 million yens for yearly operating cost, and reduction of over 20 years' leading time to acquire know-hows in advanced fabrications. These benefits have attracted many research groups. Since ten years, the number of research groups who sent us the letter of consensus exceeded 456. Over 900 members are yearly subscribed (including renewal and new subscription). In year 2020, over 550 persons have used cleanroom and their total access count exceeds 16,000.

Operation principle is also "own help, public help, and mutual help". Budgetwise, each term of the principle corresponds to: (1) User's payment to participate budget acquisition (charged according to the officially-approved d.lab's internal rule), and (2) national budget allocated to d.lab platform research division, MEXT Nanotechnology Platform project, and (3) major laboratories (who rent space in Takeda Building for their research work) as well as research projects with d.lab operation laboratories (such as Mita Lab). Of course, each budget category is righteously dispensed in perfectly following its own rule defined by corresponding laws and ordinances. The yearly operation cost of 300 million yens are composed of equipment installation, electricity and water fees, maintenance, and personnel. National Universities have acquired budget flexibility since the date of private agency statuses. It helps a lot to ensure staff employment as well as small to middle sized equipment acquisition.

Platform Device Research Division staffs acquire implicit information for future fabrication technologies, due to daily help to massively parallel research projects. The team develops technologies with high demand and universality and make them accessible by publishing papers.

Moreover, taking full advantage that PDRD is a division of d.lab, the team has been developed for over 10 year, a reliable research scheme for integration of LSI and MEMS devices, known as "Integrated MEMS research domain". As summarized in a peer-reviewed journal [1], through VDEC function of d.lab "LSI foundry", a specific LSI circuit silicon wafers are fabricated through company (such as Phenitec Semiconductor). Then the wafer is "post"-processed in an open nanofabrication platform including Takeda Sentanchi Supercleanroom. The critical advantage of such scheme is that researchers can "easily" obtain silicon wafers with transistor circuits, which has been really difficult for university cleanrooms to acquire reliability, and can fabricate by themselves specific MEMS that no foundry company can provide. Namely, researchers can produce "World's first functionality" with "World's highest quality". Such a flexible scheme is unique in the world. Yearly one multi-chip fabrication is performed (pre-fixed participants upon request), including collaborative research works with industries.

[2] Y. Mita et al., Japanese Journal of Applied Physics, 56, p. 06GA03, 2017 (2017) DOI: 10.7567/JJAP.56.06GA03

2.4.3 Activity Report 2021 of Platform Device Research Division

【Prize】The MEXT Nanotechnology Platform Project gives prizes for good usage of platform. Every year, several projects are selected by specialists' award committee, among solicited candidates selected from over 3000 research project reports. Among the projects that PDRD have solicited, we won again the 1st prize "Best use award" on "Silicon MEMS monolithic SPR spectroscopy sensor by using plasmonic structure" (Fig.3). Note that our division has been awarded consecutively for three years, including two last years as the best use award. The awarded group are UEC Tetsuo Kan's group. It is about MEMS devices that can make selective spectroscopy enhanced by nanostructure.

【No infection case & no decrease in platform uses】In the year 2021, we also continued strict but acceptable anti-pandemic protocol. Due to the influence of Omicron variant, which is less toxic but much more contagious, we identified three positive cases (of maintenance company as well as user), but zero transfection has been obtained.

【Post-Nanotech platform national project】The major part of "public" help for cleanroom has been covered by MEXT Nanotechnology platform. Nanotechnology platform project will end his period at the end of financial year Reiwa 3rd (31/Mar/2022); MEXT has started another national project, by officially stating "use heritage of nanotech platform", for digital transformation (DX) in materials including MEMS devices. The name of the new project is called "Material DX". Structurally speaking, material DX have adopted "research domain hub-and-spoke" system, in contrast with Nanoplat's "technology domain system" composed of characterization, nanofabrication, and material syntheses.

d.lab PDRD has been merged with Nano Engineering Center of Institute of Engineering Innovation and Information Technology Center to form a strong hub team, under presidency of Professor Yuichi Ikuhara. The team has been highly appreciated by the evaluation committee and was granted for 10-year project's "hub" site. Following the year 2020, MEXT has granted us a big supplemental budget for our proposal to enhance performance of our cleanroom that will take place at mid-FY2022. Also, d.lab was awarded by MEXT's "Next generation X-nics research site" and also supplemental budget has been granted. In total, we have identified 4500 millions of yens to complete competitive Cleanroom; yielding 300M yens per year if we renew everything at every 15 years.

Fig.2.4.3 Group photo after award ceremony

2.5 ADVANTEST D2T Research Department

2.5.1 Introduction of ADVANTEST D2T Research Department

2.5.1.1 Aim of establishing ADVANTEST D2T Department (former D2T research division)

ADVANTEST D2T research division was established in VDEC in October 2007. As the name suggests, it is financially supported by ADVANTEST Corporation.

The aim of establishing ADVANTEST D2T research division was to promote the research and education environment with regard to VLSI testing in all universities and colleges in Japan. "D2T" signifies that we consider not only design but also testing. Through our activities, we hope to provide expertise in design and testing for the industry. In addition, we are exchanging researchers with those of other universities and research institutes both in Japan and overseas. Moreover, D2T research division is suitable for collaborations with the industry because VLSI testing is one of the most practical research topics in the industry. On the basis of these activities, our final goal is to become a center of excellence of VLSI testing in Japan.

D2T research division has spent a total of 12 years to develop the first (Oct. 2007 – Sep. 2010), second (Oct. 2010 – Sep. 2013), third (Oct. 2013 – Sep. 2016), and fourth (Oct. 2016 – Sep. 2019) phases. D2T activity report of 2021 presents the last financial year, i.e., Oct. 2020 – Sep. 2021, of the fifth phase. Systems Design Center, School of Engineering, the University of Tokyo has been established in Oct. 2019, and Advantest D2T research department is within the center. D2T research department primarily focuses on D2T research activities and education. The fifth project phase (Oct. 2019 onwards) of D2T project was commenced by courtesy of ADVANTEST Corporation. The details pertaining to the activities of our group are presented in the following sections.

2.5.1.2 Members of ADVANTEST D2T Division

Project Professor	Masahiro Fujita
Postdoctoral research fellow	Zolboo Byambadorj
Project Lecturer	Akio Higo
Researcher	Koji Asami (Advantest Laboratories Ltd.)
Researcher	Masahiro Ishida (Advantest Corporation)
Researcher	Takahiro Yamaguchi
Assistant Clerk	Makiko Okazaki

2.5.2. Report of the 16th D2T Symposium

The 16th D2T Symposium was held on September 15, 2021, online (a part of the talk is hybrid). This year, we invited the following overseas lecturers to introduce their research on biosystems, BioMEMS, Memory, 3D integration, and Design Optimization, AI chips: President of the University of Tokyo, Professor Teruo Fujii, director of d.lab, Professor Tadahiro Kuroda, Professor Wayne Luk from Imperial College London, Professor Alex Orailoglu from University of California, San Diego, Fellow of the University of Tokyo and Professor Tim Cheng from Hong Kong University of Science and Technology, Professor Mehdi Tahoori from Karlsruhe Institute of Technology, Dr. Shin-ich Ouchi from AIST for their distinguished research topics. Dr. Zolboo presented the recent D2T research activities.

We sincerely appreciate each participant for their contributions to the symposium. We look forward to greater participation again at the next symposium.

16th D2T Symposium Program ONLINE　September 15, 2021

10:00	**Opening Remarks** **Tadahiro Kuroda** (Director, d.lab, School of Engineering, the University of Tokyo) **Yoshiaki Yoshida** (President & CEO, ADVANTEST CORPORATION)
10:15	**Session 1** (Chairpersons: Yoshio Mita, Masahiro Fujita, d.lab, the University of Tokyo) *Microfluidics for Cellular and Molecular Systems* **Teruo Fujii**, President (the University of Tokyo) *Meta-programming Strategies for Multi-Target Design Optimisation* **Wayne Luk**, Professor (Imperial College London)
12:00	**Lunch**
13:00	**Session 2** (Chairperson: Tetsuya Iizuka, d.lab, the University of Tokyo) *Time Performance Improvement by Agile Design and 3D Integration* **Tadahiro Kuroda**, Professor (d.lab, the University of Tokyo) *Design of Reliable and Efficient Deep Learning Processing Systems* **Alex Orailoglu**, Professor (University of California, San Diego)
14:45	**Session 3** (Chairperson: Makoto Ikeda, d.lab, The University of Tokyo) *Ratio based Resistive Memory Cells for Low Error Rate and High Energy Efficiency* **K.-T. Tim Cheng**, Professor (Hong Kong University of Science and Technology and Fellow, the University of Tokyo) *AI-Accelerator Proof of Concept by a Multi-IP Chip Project* **Shin-ichi O'uchi (S. O'uchi)** Laboratory Team Leader, AIST-UTokyo AI Chip Design Open Innovation Laboratory (AIDL) National Institute of Advanced Industrial Science and Technology (AIST)
16:30	**Session 4** (Chairperson: Masahiro Fujita, d.lab, The University of Tokyo) *Recent D2T research department progress* **Akio Higo**, Lecturer (d.lab, The University of Tokyo) *Analysis and Calibration Techniques of Modulated Wideband Converter for High-Precision Sub-Nyquist Sampling System* **Zolboo Byambadorj**, Doctoral research fellow (d.lab, The University of Tokyo) *Computing Paradigms based on Flexible Inorganic Printed Electronics* **Mehdi Tahoori**, Professor (Dependable Nano-Computing at Karlsruhe Institute of Technology)
18:00	**Closing Remarks** **Masahiro Fujita** (d.lab, School of Engineering, The University of Tokyo)

2.5.3 Research Activity Reports of the ADVANTEST D2T Research Department

High-Resolution Analog-to-Digital Converter Based on Stochastic Comparators

Takahiro J. Yamaguchi, Akio Higo, Tetsuya Iizuka

This project aims to explore stochastic analog-to-digital converter (ADC) architectures. Process variations, together with many factors such as variations in voltage or temperature, lead to mismatched design parameters that produce input-referred offsets and hence cause non-linearity and missing output codes in an ADC. Instead of attempting to suppress such process variations as in conventional ADC, the stochastic ADC approach exploits the stochastic properties of many comparators such as random variation of input-referred offset and Gaussianity of the internal noise to enhance the quantization accuracy. However, the published papers only show that stochastic ADCs are noisier than the conventional flash ADCs [*TCAS-I*, Vol. 57, no. 11, 2010]. The central limit theorem can be applied to discrete type RVs such as a group of comparators and their sum [A. Papoulis 2000]. It shows that for this discrete RV, many more terms are required in the sum before going convergence to a Gaussian distribution [S. L. Miller 2004]. These results in the adequate number of bits (ENOB) of the stochastic ADC are represented by log44*B* [*TCAS-I*, Vol. 57, no. 11, 2010], being smaller than the ENOB of the conventional flash ADC, which is given by log22*B*. An approach for robustly detecting level-crossing time using stochastic median is investigated to address randomness issues and achieve accuracy.

High-Performance Analog-to-Digital Conversion Using the Wideband Spread Spectrum and Its Applications

Koji Asami, Zolboo Byambadorj, Akio Higo, Tetsuya Iizuka, Masahiro Fujita

We investigate the compression sampling method to measure low-cost RF devices for IoT and other applications. A 4-channel MWC circuit was fabricated, and we verified our proposed methods to improve the characteristics. We measured and verified characteristics by the Bluetooth and LTE waveforms that used the device under test for RF communication, and this project was closed by the end of March 2021.

5G multi-channel/millimeter-wave signal measurement

Koji Asami, Zolboo Byambadorj, Ryogo Koike, Sheng Guo, Nguyen Ngoc Mai-Khanh, Akio Higo, Tetsuya Iizuka, Masahiro Fujita

We study and develop fundamental research to measure the millimeter-wave signals in an over-the-air environment. In this financial year, we designed and fabricated the planar monopole probe antenna with a high spatial resolution for the near field measurement of the millimeter-wave antenna. We developed algorithms for the near-to-far-field transformation and the identification of probe characteristics. We have established the experimental setup for millimeter-wave measurement and are currently proceeding the verification and the performance improvement by using actual antennas for 5G.

High-Speed and High-accuracy Multi-Pin Timing CAL for ATE

Masahiro Ishida, Hidaka Otsuka, Tetsuya Iizuka, Toru Nakura, Zule Xe, Akio Higo, Masahiro Fujita

Automatic test equipment (ATE) for Semiconductors has thousands to tens of thousands of signal input and output channels. It requires timing calibration (CAL) to correspond the test signal output's timing to the device under the test (DUT) and the comparison timing of the signals output from the DUT. This research focuses on a high-speed and high-accuracy multi-pin timing CAL method applicable to ATE. In this financial year, we discussed and determined the circuit scheme to realize our research goal that the target accuracy of the timing CAL is at 1 ps. Then, we designed the test element group (TEG) chip for LSI shuttle services in VDEC

function at d.lab design platform research division. We discussed the challenges for developing the timing CAL devices, and we decided to fabricate TEG for evaluating the CAL accuracy degradation by the power variation and thermal environment. We designed the TEG layout and LSI circuit using the TSMC 65 nm CMOS process, and we confirmed the target accuracy of 1 ps by simulations. Then, we taped out the design.

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2.5.4 Publication

Journal

[1] Zolboo Byambadorj, Koji Asami, Takahiro J. Yamaguchi, Akio Higo, Masahiro Fujita and Tetsuya Iizuka, "A Calibration Technique for Simultaneous Estimation of Actual Sensing Matrix Coefficients on Modulated Wideband Converters," IEEE Transactions on Circuits and Systems-I: Regular Papers, vol. 67, no. 12, pp. 5561 - 5573, Dec. 2020.

Chapter3 Research in d.lab

Kuroda and Kosuge Laboratory
(http://www.kuroda.t.u-tokyo.ac.jp/index.html)

TCI: ThruChip Interface

T. Kuroda, M. Hamada, A. Kosuge, T. Shidei, M. Okada, Wai-Yeung Yip, K. Shiba, T. Omori

TCI is a 3D integration technology that employs inductive coupling between coils created with on chip metal line patterns for data communication across stacked chips. It realizes the same or better performance as TSV (Through Silicon Via) but at a lower cost. This year, we presented research papers on TCI-based 3D SRAM stacking technologies including (a) circuit technology for low-power computation, (b) area efficient coil-design, and (c) computing architecture and AI processing algorithms to use 3D stacked SRAMs efficiently. We presented our achievements at ESSCIRC'21 and EDAPS'21.

TLC: Transmission Line Coupler

T. Kuroda, M. Hamada, A. Kosuge, Y. Hayashi, Ximing Wang

TLC is a data communication technique between circuit boards by utilizing electromagnetic coupling between transmission lines on them. It solves the issues in conventional connectors such as wearing, reliability against vibration, and impedance mismatch, realizing wireless connectors. This year, through joint research with a company, we conducted research and development of compact and high-density TLC mounting technology for connecting packaged boards and PCBs, and research on fully sealed non-contact connector technology for simultaneous communication of non-contact power supply and TLC in close proximity to each other. GND shielding technology is studied to prevent mutual interference between wireless power transmission and contactless communication.

RFID Tag Chip Design

T. Kuroda, M. Hamada, A. Kosuge, R. Miura, S. Shibata

We are developing a wireless tag that integrates an antenna and wireless circuits on a tiny chip less than 1 mm square and combine it with an intelligent reader to pursue an extremely low-cost IoE (Internet of Everything) system. This year, we developed a new collision avoidance function that deterministically avoids collisions based on received signals by utilizing adiabatic circuits. We developed a low-power RFID tag circuit using TSMC 0.18m CMOS process by using our proposed the adiabatic logic circuit and presented our experimental results at A-SSCC'21. We have also developed a new bonding-less mounting technology in which the coil mounted on the RFID tag is coupled to the coil on the PCB. A test chip was developed and evaluated using TSMC 0.18um CMOS process, and papers were presented at SSDM'21, ASP-DAC'21, and JJAP'22.

Wired-logic AI Processor

T. Kuroda, M. Hamada, A. Kosuge, K. Shiba, Yao-Chung Hsu, R. Sumikawa, F. Hondo

We are studying non-von Neumann AI processors focusing on wired-logic to reduce power consumption. The area efficiency is a bottleneck of the wired-logic processor and it is significantly degraded due to the need to implement a huge number of elements on a chip. Therefore, we have developed two new technologies: (1) a technology to optimize the network by removing unnecessary neurons and synapses, called pruning in the human brain, and (2) a nonlinear neural network technology that incorporates the property of human neurons to use a wide variety of nonlinear functions in the right places to increase the representation capability of the network in order to prune more drastically than before and save the number of elements. In addition, we are developing convolutional wired-logic architecture circuits that reuse circuits in accordance with the processing of convolutional algorithms. Research works regarding MNIST and CIFAR-10 using FPGA were published on IEEE JETCAS and OJCAS respectively.

mmWave Imaging Radar based Object Recognition

T. Kuroda, M. Hamada, A. Kosuge, Wai-Yeung Yip, S. Suehiro

In harsh environments (bad weather, night, dirt on cameras), conventional human/object detectors utilizing conventional cameras have low accuracy. Since millimeter wave radar technology has high environmental resistance, the radar is promising solution for the harsh environment. However, unlike image recognition, it has a problem in detection algorithm due to low-resolution blur data. In this research, we are developing a new deep learning AI technology that handles millimeter wave images based on a new semi-automatic training data generation technology and develop a highly accurate AI technology for human/object identification. This year, we mainly studied the characteristics of millimeter-wave radar data and the network structure that matches them and developed a camera-radar cooperative semi-automatic learning data generation technique and developed a millimeter-wave radar AI system that can detect the type and location of six types of objects with the same accuracy as image recognition.

Takeuchi Laboratory
(https://co-design.t.u-tokyo.ac.jp/)

Computation in memory (CiM)

Ken Takeuchi and Chihiro Matsui

We have developed a comprehensive Computation-in-Memory (CiM) simulation platform. The simulation platform has capability to emulate multi-level cell (MLC) and various memory device non-idealities such as uniform/non-uniform conductance variation and shift. The simulation results address that the conductance shift has much more critical impact than conductance variation on inference accuracy in CiM.

Simulated Annealing

Ken Takeuchi, Chihiro Matsui and Naoko Misawa

Memory error tolerant ReRAM-based Computation-in-Memory (CiM) to solve the knapsack problem, one of the combinatorial optimization problems, is proposed. Proposed log-encoding simulated annealing (SA) on ReRAM CiM reduces the array area of ReRAM CiM by 97.6%. To co-design ReRAM device and SA, error injection is applied. As a result, the asymmetric ReRAM error increases the acceptable bit-error rate (BER) by 10 times and the acceptable bit precision to 5-bit.

In-sensor Computing

Ken Takeuchi and Chihiro Matsui

We have proposes an integration of event-based vision sensor (EVS) and processor (e.g., computation-in-memory, CiM) for low-power processing. By using newly defined characterization method of frame and EVS camera, an event-driven SRAM CiM with partitioned word-line (WL) activation method is proposed for 3D-integration of EVS. The multiple-bit synaptic weights are stored in a set of SRAMs. The proposed CiM for EVS achieves 10-6 times energy efficiency compared with CiM for frame camera.

Nakamura Laboratory
(http://www.hal.ipc.i.u-tokyo.ac.jp/)

IoT Network Security

Hiroshi Nakmaura

Zigbee is a short-range wireless communication protocol and needs low power and low bandwidth at the sacrifice of its short transfer range and slow speed. Due to this nature, it is widely used in small inexpensive sensors and IoTs that run on batteries, As Zigbee adopts indirect communication to achieve low power consumption, it incurs a vulnerability to LDoS attacks. To solve this problem, we proposed a countermeasure method and attacker detection algo-

rithm without consuming large computing resources or power to satisfy the constraints of IoT devices. Through experimental simulation, we confirmed its effectiveness.

Coarse-Grain Reconfigurable Architecture

Takuya Kojima, Hiroshi Nakamura

Coarse-grained reconfigurable architectures (CGRAs) are expected as a promising architecture for wide variety of computing including embedded systems and high-performance computing due to its benefit of high-energy efficiency and programmability. CGRA consists of an array of numerous processing element and its efficiency heavily depends on the quality of compiler which maps applications onto these PEs. So far, we have proposed a novel algorithm called GenMap (A Genetic Algorithmic Approach for Optimizing Spatial Mapping), which is a mappaing framework based on a genetic algorithm. We extend GenMap to handle not only spatial but also temporal reconfiguration and confirmed its effectiveness.

Lightweight Runtime Environment of ROS2 nodes for Embedded Devices

Hideki Takase, Hiroshi Nakamura

The Robot Operating System (ROS) and ROS2, the latest version of ROS, have attracted attention as a design platform for distributed robot software development. One of the drawbacks of ROS2 is that it is necessary to employ high-performance and power-hunger devices since it requires a Linux environment for operation. This drawback prevents ROS2 from being applied to embedded devices because they must be quick in response and consumes less power. Thus, we have proposed a novel solution called mROS2, which is a lightweight runtime environment of ROS2 nodes. One of the advantages of mROS2 is that it provides efficient communication mechanisms with less memory consumption. Currently, we are designing software architecture for this communication flow. This work is expected to contribute to the power saving and real-time performance enhancement of mobile robot systems.

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Logic Synthesis for Generalization and Learning Addition

Masahiro FUJITA, Xinpei ZHANG, Mingfei YU, Qingyang YI, Yukio MIYASAKA

Logic synthesis generates a logic circuit of a given Boolean function, where the size and depth of the circuit are optimized for small area and low delay. On the other hand, machine learning has been extensively studied and used for many applications these days. Its general approach of training a model from a set of input-output samples is similar to logic synthesis with external don't-cares, except that in the case of machine learning the goal is to come up with a general understanding from the given samples. Seeing this resemblance from another perspective, we can think of logic synthesis targeting a generalization of the care-set. In this research, we try such logic synthesis that generates a logic circuit where the given incomplete relation between input and output is generalized. We compared popular logic synthesis methods and machine learning models and analyzed their characteristics. We found that there were some arithmetic functions that these conventional models cannot effectively learn. Out of them, we further experimented on addition operations using tree models and found a heuristic minimization method of BDD achieves the highest accuracy.

FPGA Based Accelerator for Neural Networks Computation with Flexible Pipelining

Masahiro FUJITA, Heming SUN, Qingyang YI

FPGA is appropriate for fix-point neural networks computing due to high power efficiency and configurability. However, its design must be intensively

refined to achieve high performance using limited hardware resources. We present an FPGA-based neural networks accelerator and its optimization framework, which can achieve optimal efficiency for various CNN models and FPGA resources. Targeting high throughput, we adopt layer-wise pipeline architecture for higher DSP utilization. To get the optimal performance, a flexible algorithm to allocate balanced hardware resources to each layer is also proposed, supported by activation buffer design. Through our well-balanced implementation of four CNN models on ZC706, the DSP utilization and efficiency are over 90%. For VGG16 on ZC706, the proposed accelerator achieves the performance of 2.58x, 1.53x and 1.35x better than the referenced non-pipeline architecture, A, pipeline architecture B and C, respectively.

FPGA Based Accelerator for Neural Networks Computation with Flexible Pipelining

Masahiro FUJITA, Ryogo KOIKE

Due to the large scale integration of VLSI in recent years, formal verification technique becomes much important. One of them is inductive invariant that is used to compute sets of reachable state in a sequential circuit. For inductive invariants, it is important to select the subset of flipflops in order to find a small and/or useful superset of reachable states. It is difficult to compute inductive invariants with all flipflops, so it may be useful to use the subsets of flipflops. In this research, the calculation of inductive invariants is formulated with Quantified Boolean Formula (QBF). The QBF problem can be solved incrementally by using MUX for choosing flipflops. We confirmed the validity of our method with ISCAS89 benchmark circuits.

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Implementation of Fully Homomorphic Encryption

M. Ikeda, T. Shimada, Y. Zhao, and M. Fujita

Fully homomorphic encryption (FHE) is a public-key cryptography scheme that allows any operation to be performed in ciphertext without a secret key. While this technology is expected to be a solution to the privacy problem, which is the biggest concern of current cloud-based services, it has the problem of large computational resources. This research aims to speed up the fully homomorphic encryption, such as TFHE and BGV, by implementing ASIC. The chip prototyped this year has achieved a 4-fold speedup compared to CPU, and further speedups are expected in the future.

We are also focusing on improving algorithms and security parameters to achieve higher speeds when implemented in hardware. Specifically, we have proposed a method to increase the number of operations types that can be performed in a single step by modifying the TFHE algorithm. We also studied methods to optimize the security parameters for the shortest execution time under the constraints of hardware architecture and security level, etc.

Design optimization of high-performance cryptography

M. Ikeda, K. Ikeda, A. Opasatian, K. Masada, and F. Arakawa

The development of more advanced technology such as IoT and Functional encryption, such as attribute-based encryption, drives the need for higher and broader specification of high-performance cryptographic computation. To achieve those needs, the performance of elliptic curve cryptography computations are improved in various ways. Using the scheduling and optimal modular multiplication algorithm, we extend the acceleration of pairing cal-

culation to the scalar multiplication and the hash to point calculation as well. The pairing engine is also designed to support the computation in many curves setting. Moreover, the automated design of accelerator architecture for different curve are also being researched to help reduce the design time, which is an issue in hardware cryptographic design. The demonstration of practical use case is showcased by integrating the pairing engine to accelerate the software implementation of the file encryption system based on attribute-based encryption.

Implementations of Post-Quantum Cryptography (PQC) Algorithms

M. Ikeda, H. Bui, and T. Shimada

Post-quantum cryptography is a type of public-key cryptography that is resistant to attacks by both classical and quantum computers yet can be performed by a conventional computer. It aims to replace modern-day cryptography standards such as classic Diffie-Hellman, RSA, and elliptic curve which all can be cracked in polynomial time with a sufficient quantum computer. Examples of some PQC algorithms include lattice-based cryptography (NTRU), codes-based cryptography (Classsic McEliece) and, super-singular-isogeny-based cryptography (SIKE).

Among these PQC algorithms, we are currently focusing on an improved SIKE implementation as it provides multiple benefits over the others chief of which is that it is an extension of elliptic curve cryptography. Its main problem lies in its speed, which is an order of magnitude slower to run than the other PQC candidates. Our research aims to improve the speed of the algorithm by using the inherent parallelism offered by hardware acceleration and by using a dataflow approach to the design applicable for ASIC implementation. Currently, we have determined the maximum speed that SIKE can achieve and are aiming to use clocking techniques to reduce the amount of hardware resources yet maintain the speed at around the same level.

Security Measures of Crypto-engine

M. Ikeda, K. Abe, and S. Kikuoka

Cryptographic circuits must be resistant to side-channel attacks. We conducted template attacks using measured current consumption on a hardware implementation of 256-bit ECDSA to leak a part of secret information and confirmed that it is possible to recover the secret key via lattice attacks. In addition, we considered the conditions under which the attack was likely to succeed and countermeasures based on the attack results.

For hardware implementations of elliptic curve pairings, it is important to select the optimal curve that achieves both sufficient security and low cost. We evaluated the security against solving DLP (discrete logarithm problem) and ECDLP(elliptic curve discrete logarithm problem) and hardware costs such as area, cycles, and latency of paring-based cryptography on major pairing-friendly elliptic curves like BN and BLS12 curve with multiple parameters.

Neural network and its security

M. Ikeda, Z. Wang, and B. Amartuvshin

The huge computing cost of neural network has become an obvious obstruction from its wide application. Specific hardware can greatly reduce the computation time and energy consumption but its designing is still a changeling task due to large resource requirements of involved operations. Recently Binary Neural Network (BNN) has attracted much attention because of its compactness and easy implementation. We designed a self-synchronous circuit for BNN to further enhance the energy efficiency and calculation speed. The simulation results showed the light-weightness while considerable throughput is kept.

On the other hand, cloud computing is another method to prevent the unaffordable computational cost on personal computers. However, it may involve severe privacy problems due to uploading original data to the cloud server. Fully Homomorphic

Encryption (FHE) is believed as a solution to the privacy concern, while it still suffers from the huge computing cost and as only addition and multiplication are supported in FHE, degradation of accuracy is unavoidable. In this research we designed ASIC hardware to highly improve the computing speed compared with the common platforms such as CPU and GPU. We chose BGV algorism, which is one of FHE schemes, for encrypting the computations in neural network and have designed a polynomial multiplier for accelerating BGV computations. Also, we adjusted the neural network structure to meet the FHE requirements. We investigated the effects of activation function, training method and layer structure of the neural network with only additions and multiplications and made the accuracy almost the same as the original network.

Smart Image Sensors / SPAD Sensors and Measurement Methods

M. Ikeda, Y. Miao, D. Jiang, N. Watanabe, H. Matsuoka, and T. Kikkawa

We have been working toward new types of image sensors with higher functionality and performance, such as smart image sensors and SPAD sensors.

Smart image sensors integrate advanced information processing into the sensor to achieve various functions. We designed a ToF image sensor with light to pulse frequency modulation and digital processing for decoding the modulated signal, for signal identification under multi-user interference. We also design a ToF image sensor with long-distance ranging capability by adding phase shifting circuits. These sensors have been fabricated, and we have evaluated the real-world performance.

SPAD sensors have extremely high sensitivity and time resolution and are thus considered to be promising for applications such as distance ranging and fluorescence lifetime imaging (FLIM). In FLIM photons' arrival time histograms are used. To achieve high-efficient histogram generating, we have proposed a method that allows adjustment of the class width so that finer measurements can be taken in the early stages of decay with limited hardware resources. In addition, intending to efficiently process temporal information of input photons in real-time, we are working to introduce event-based data processing methods for SPAD image sensors. We have designed the sensors, and evaluation of the fabricated sensors is in progress.

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Phase-Locked Loop Circuit Techniques for Low Phase Noise

Tetsuya Iizuka, Zule Xu, Zunsong Yang, Masaru Osada, Ryoga Iwashita, Yo Kumano

Switched-capacitor sampling PLLs (SC-SPLL) are competitive for both low phase noise and low power consumption. However, the conventional type-I architecture is unsuitable to fractional-N operation. A type-II PLL is a good candidate, but it conventionally demands a transconductance-based (gm-based) integrator or an extra DAC, which necessitates extra power and area. In this work, we propose a type-II hybrid architecture re-using sampling capacitor as a capacitive digital-to-analog converter (CDAC) that receives the digital integrator's output. In this way, no gm cell or extra DAC are needed. Thus, the entire architecture is compact and with high performance as well. The prototype chip in 65-nm CMOS achieves −80-dBc reference spur, 236-fs integrated RMS jitter, and 4.6-mW power consumption, translating to −246-dB FoM.

Ring voltage-controlled oscillator (VCO) is attractive for a compact footprint, multiple phases, and no magnetic coupling. However, for the low-jitter PLL higher than 5 GHz, most previous works still resort to LC VCOs where the inductors suffer from a large area and underlying magnetic coupling. We proposed an inductorless cascaded PLL with ultra-

low jitter that leverages the large performance gap between low- and high-frequency ring oscillators. A single-stage sample-and-hold subsampling phase detector is proposed for the 1st stage, where the oscillator's control voltage is updated only when the impulse sensitivity function is zero, enabling wider loop bandwidth, lower jitter, and lower spur. Fabricated in 65-nm CMOS, the prototype operating at 10GHz achieves –63-dBc reference spur, 175-fs integrated RMS jitter, and –240-dB FOM with a 125-MHz reference clock.

We proposed a low phase noise, fractional-N ring PLL that makes use of the Harmonic-Mixer (HM) based feedback architecture and a nested PLL based phase-domain filter. Compared to their LC-based counterparts, ring oscillators enjoy benefits such as small area, multi-phase outputs, and absence of magnetic coupling among others. However, their inferior phase noise requires a wide PLL loop bandwidth, making it difficult to employ in fractional-N PLLs where the Multi-Modulus-Divider (MMD) contributes large quantization noise. To overcome this issue, this work proposed an architecture that uses HM-based feedback to avoid noise amplification, and a nested-PLL-based phase-domain filter to both filter out the quantization noise and increase the shaping frequency. The effectiveness of the proposed method was shown through calculation, simulation, and measurement of an actual chip designed in 65nm CMOS process.

Based on the conventional second-order ΔΣ FDC(Frequency-to-Digital Converter)-PLL that can reduce phase noise with noise shaping, we proposed a higher-order ΔΣ FDC-PLL for a wider loop bandwidth and lower phase noise. To solve the stability issue from the higher-order ΔΣ FDC, we introduced MASH(Multi-stAge noise SHaping). We demonstrated the higher-order quantization noise shaping of the MASH 2-k FDC and the lower phase noise/jitter performance of the proposed FDC-PLL by MATLAB Simulink. The MASH FDC can be designed by using a SAR ADC for the first stage, and using a ΔΣ ADC with FIAs(Floating Inverter Amplifiers) for the next stage.

Performance indicators of voltage-controlled oscillators (VCOs) include phase noise, power consumption, circuit area, and oscillation frequency, etc. In fields such as wireless communications, LC-VCOs are generally used because of their superior phase noise characteristics. As one of the topologies, a gate bias is applied to the cross-coupling transistor, and it is always operated in the saturated region to increase the conversion efficiency from DC power to signal (RF) power. We have designed and fabricated prototypes of NMOS and CMOS Class-C VCOs that reduce power consumption while keeping the phase noise at

the same level as conventional ones. Unfortunately, we could not measure the phase noise of the NMOS VCO due to a buffer design error, but we plan to confirm the phase noise of the CMOS VCO as soon as we receive the chips TO in January. FoM is expected to be 188~190dBc/Hz based on simulation.

High-Precision Analog-to-Digital Conversion Circuits and its Design Automation Techniques

Tetsuya Iizuka, Zule Xu, Shuowei Li, Akira Matsuoka, Ryoya Shibata, Haoming Zhang

There is a strong demand for high resolution and high power efficient ADC. To improve the power efficiency of edge devices, fully-dynamic discrete-time A/D converters (DTADC) are suitable, which have the scalability of the power and the operating speed. This research proposes a fully-dynamic DTADC using floating inverter amplifiers (FIA). Correlated level shifting (CLS) is applied to FIA, which results in 50dB DC gain with one stage amplifier. A new sampling noise cancel technique with CLS-FIA was proposed. Proposed ADC achieved a 91.8 dB SNDR, while consuming 76.2 μW in simulation.

As the demand for high-speed communications and high-speed analog-to-digital converters contin-

ues to grow, the design requirements for high-speed and low-power comparators are increasing. We have established a mathematical model and simplified it. By controlling a few parameters, the degree of calibration of the strong-arm comparator can be completely predicted. The designer can easily set up the circuit for the strong-arm comparator based on our design guidelines to make a calibration. Also, to simplify the design of analog circuits, we try to design the ADC based on standard cells. For the capacitor selection of the sampling circuit, we found that we can select an appropriate channel length, float the source and drain terminals of the transistor, to obtain a MOSFET-based capacitor that is almost independent of the bias voltage, thereby replacing the commonly used MIM and MOM capacitors. It becomes possible to design sampling circuits based on standard cells.

Noise generally causes poor system performance, and various techniques are used or additional power is consumed to avoid the noise. Stochastic resonance is a phenomenon in which adding noise of a certain intensity to a nonlinear system improves the performance of the system. When this phenomenon is applied to analog-to-digital converters (ADC), it is expected to improve the detection accuracy of weak signals and reduce power consumption by allowing noise in the circuit. In our study, the proposed circuit utilizes the same architecture as a charge-redistribution successive approximation register (SAR) ADC. We have analyzed the performance under the assumption of ideal noise application. In addition, our simulations have shown that when the input signal amplitude is comparable to the input-referred noise of the comparator, the performance of the proposed circuit can be better than the SAR ADC.

The dynamic circuit is a type of circuit that differ from static circuit, it is a combinational logic that make flexible use of the storage of information in the form of charge on the capacitance. Even though it's functionally identical as the commonly used static combinational logic, it has the advantage of power-efficiency and higher speed and smaller area because of using less transistors, especially P-MOS. However, a clock signal has to be added to take control of the phase of the periodic charging and discharging while ensuring the correct logic function, thus the timing of dynamic circuit is much more complicated than the common static logic and is always a difficult task that need huge manual force to be properly arranged. In this study, we want to reduce that manual force by semi-automizing the timing arrangement. The specific method is to characterize the dynamic circuit to a standard cell with timing information, and use Synopsys tool to check the complex timing in the proper way. Since it is not a traditional circuit, the construction of the model of dynamic circuit and the utility of tool is challenging.

Millimeter-Wave Circuit Design for Wideband Communications

Tetsuya Iizuka, Takamichi Horikawa, Sota Kano

In recent years, there is growing demand for the next-generation wireless communications such as Beyond 5G and 6G, which realize ultra-high-speed communications exceeding 100 Gb/s. Millimeter wave band from 30 to 300 GHz offers a wide frequency bandwidth and is being actively studied for Beyond 5G and 6G applications.

In this study, we designed an oscillator, which is essential component in millimeter-wave integrated circuits, with operating frequency of 150 GHz. It is challenging to ensure gain for oscillation at these very high frequencies near the operating limit of transistor. Thus, we presented a novel method of increasing the oscillation frequency and output power, using the design method of power amplifiers optimizing the power gain. In the proposed method, impedance matching based on transmission lines maximizes the power extracted from transistors, and simultaneously adjusts the oscillation frequency to the target value using the phase shift caused by the

line length. We actually designed the oscillator using a SiGe BiCMOS 130nm process, and shown in simulation that the output of 147.5 GHz and -0.13 dBm can be estimated. Furthermore, for application to 300 GHz band a frequency doubler was simulated, and we demonstrated that in total design the 300 GHz oscillator can operate at -12 dBm output power.

Implementation of Neuron Device based on CMOS Analog Circuits

Tetsuya Iizuka, Xiangyu Chen, Byambadorj Zolboo

As von Neumann's bottleneck worsens and Moore's Law is about to end, researchers face unprecedented challenges. One of the solutions to these problems is a computational model architecture inspired by the human brain, which has the potential to eliminate the bottleneck of von Neumann and lead the next generation of computer engineering. Morphic computing has emerged as a hotspot for research. Deep Neural Networks (DNN), the second generation of artificial neural networks (ANN), can perform operations in multiple processor layers and are widely used in many fields such as pattern recognition, language translation, and object detection. In 2017, AlphaGo, a DNNs-based Go program developed by Google DeepMind, played against a human Go world champion and finally won. It seems that DNN's great success has defeated the human brain. This performance is really great, but can it really be said that DNN can beat the human brain? There is an important question that cannot be avoided: how much energy does this computational process require? Deep learning basically only adjusts the weights by a method called gradient descent to obtain the optimum value, and the large amount of multiplication / integration operations performed by DNN in the process consumes a large amount of power. AlphaGo uses more than 2000 CPUs and more than 300 GPUs and consumes 100-200kW of power, which is about 10 ^ 4 orders of magnitude higher than the power consumption of the human brain of about 20W. It Shows a clear advantage in terms of power consumption compared to DNN.

It is well known that billions of neurons in the brain are interconnected by trillions of synapses to form a complex, high-level computational system that can process in parallel the vast amount of information received through various sensory organs. These neurons communicate with each other and process information through action potentials or spiking signals. Spiking neural networks (SNNs) are known as the third generation of ANNs and greatly bridge the gap between ANNs and biological neural networks (BNNs). SNNs are event-based learning that do not require external storage and are considered to be the most promising neuro- morphic computing systems. Like BNNs, SNNs are composed of neurons and synapses and are considered to be the most promising neuromorphic computational systems. ANNs are usually built using a bottom-up approach, meaning that each component of BNNs needs to be simulated.Therefore, the first and most important step to implement SNNs in hardware is to design their basic building blocks, such as spiking neurons and synapses.

A number of hardware-implemented spiking neurons or synapses have been reported. However, most of these conventional spiking neurons use analog information such as voltage and current to communicate with each other, which leads to requirements on the magnitude of the voltage or current. To implement the Leaky-integration function of neurons on signals, integrators with operational amplifiers are often built and use large on-chip capacitors and resistors to achieve long time constants. Even more, to achieve the “fire” function of neurons, the inclusion of comparators is used to simulate the threshold of neurons. These approaches will undoubtedly make the neuron power consumption very high and the chip area occupied very large.

we propose a neuron-synapse structure that uses

time-domain analog signals (pulse interval, pulse width and frequency) for signaling, and the circuit structure includes a leaky integrate-and-fire (LIF) neuron, a synapse, and a weight circuit. The proposed LIF neuron does not use operational amplifiers as well as comparators and maintains a subthreshold state in the absence of signal input. In addition, since the proposed neuron-synapse structure transmits temporal signals rather than voltage and current, it is well suited for applications in reservoir computing and STDP construction.

In addition, we also build pulse-based neural networks with these proposed elements and train them with the recursive least squares method to achieve the learning function of sine waveforms.

Antenna Measurement and Testing Techniques for Wireless Communications

Tetsuya Iizuka, Mai Khanh Nguyen Ngoc, Byambadorj Zolboo, Sheng Guo

In 5G technologies, over the air (OTA) measurements are necessary for 5G antennas due to the technologies rely on millimeter-wave frequencies and small-sized terminals. The conventional OTA measurement is based on far-field measurement. However, the far-field measurement is almost infeasible in the millimeter-wave due to high path loss and low measurement accuracy. Therefore, near-field measurement takes place of OTA measurement in the millimeter-wave range. The far-field measurement data can be achieved from near-field measurement by using near-field to far-field methods.

In this research, there are plenty of challenges from hardware to software including automated near-field measurement equipment, millimeter-wave probe, and near-field to far-field transformation methods.

In the millimeter-wave probe application, we focus on an arrow-shaped monopole antenna design on a standard PCB board. The radiation pattern is proven to have an effective directivity in the simulation environment. In the measurement result after the fabrication of the arrow-shaped antenna, the target frequency is slightly changed from 28 GHz to 27.5 GHz due to some mismatch in the physical dimension of the arrow-shaped conductor.

In near-field measurement, one of the easiest ways is to measure S-parameters on the planar scanning area in front of the antenna under test (AUT). Not only it is practically uncomplicated to make the measurement, but the transformation method after the measurement is also straightforward. In this research, the near-field measurement is made on a rectangular plane within the range of near-field distance from AUT. During the scanning process on the rectangular plane, AUT and probe connections are impacted by undesirable vibration from moving sliders.

The method of near-field to far-field transformation in our research is based on plane wave spectrum (PWS). Using several differently oriented measurements of unknown patterned AUT with the unknown patterned arrow-shaped monopole probe antenna, the pattern of AUT is theoretically obtainable under several assumptions. Due to the mismatch of physical parameters, it is impossible to achieve such ideal assumptions which lead to some undesirable effect on near-field measured data.

The preliminary results show that near-field to far-field transformed data from the measured data does have some errors compared to the simulation data and the reference data of AUT due to unwanted mismatch of hardware. Under the correct measurement setup, moderate performance on the far-field pattern can be achieved.

High-Precision Inter-Pin Skew Detection Technique for Automatic VLSI Test Equipments

Tetsuya Iizuka, Hidaka Otsuka

Timing Calibration (calibration of pin-to-pin skew) is necessary for automated testing performed on semiconductor Automatic Test Equipment (ATE). Conventional CAL methods are incapable of

performing CAL of less than 10ps, but as process miniaturization and signal speeds increase, higher-precision CAL methods will be required in the future. Also, the characteristic of ATE is that it has many pins, and the CAL method must also support multiple channels. We designed and measured a pin-to-pin skew detection circuit to realize CAL with an accuracy of 1 ps.

Conventional CAL methods use the driver and comparator of the ATE itself to mutually detect the skew. In the proposed method, the skew detection circuit is implemented on a CAL board (performance board) and is designed to detect skew at a point closer to the DUT. There is a clock tree in the circuit that can distribute precisely timed signals to each channel. By passing this signal through the comparator of the ATE, the pin-to-pin skew from the DUT to the comparator is detected. There is also a skew detector on each channel in the circuit to detect skew between the channel input signals and the clock tree signals. The detected skew is dimensionally converted to the voltage domain for external readout. By passing the ATE driver signals through each channel, this feature can be used to detect pin-to-pin skew from the driver to the DUT.

The design was done in TSMC CMOS 65nm process and the chip was measured by probing. In the simulation, the process variation of the channel-to-channel skew was suppressed to σ93fs, and the variation of the channel-to-channel skew of the clock tree with respect to environmental variations was suppressed to less than 80fs. In the measurement, the channel-to-channel skew was large due to factors not modeled in the simulation. However, it was confirmed that even when the power supply voltage was varied by 1% and a current of about 20mA was applied to the heater inside the circuit, the amount of skew variation could be kept below 1ps.

Verification of Topological Quantum State based on Electrical Circuits

Tetsuya Iizuka, Yuan Haochen

Topological quantum computing(TQC) is a method of fault-tolerant quantum computing, in which a single quantum gate could be generated by the braiding of certain topological quantum objects, named "anyons", and one simplest realization of a non-Abelian anyon is a quasiparticle named Majorana fermion which obeys ordinary Fermi-Dirac statistics and owns a particular mechanism, Majorana zero mode(MZM). Therefore, we focus on the 1D circuit chain realization of Majorana zero-energy edge states to discover whether the MZM will appear at the boundaries, by measuring the nodes' eigenmode voltages and two-point impedance.

To realize the Majorana edge mode, there are several models including the 1D SSH model and 1D Kitaev model. In this research, we focus on the circuit realization of the 1D Kitaev model.

The circuit chain contains two main lines, one line consists of capacitors C in series representing electron band while another one consists of inductors L in series representing hole band, to realize the opposite hopping parameters between electron and hole bands. The interaction between the electrons and holes is simulated by bridging capacitors C_X and inductors L_X. And each electron/hole node is connected to the ground via capacitors C_0 or inductors L_0, to make the circuit chain topological.

We have constructed three topological circuit chains with different resonant frequencies by adjusting the values of capacitors and inductors, also with three trivial chains for comparison. The rapidly increasing two-point impedance is found in the topological models with the EM simulation results, implementing the existence of MZMs at both edges. We taped out using Rohm 0.18um process.

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Variability in Nano-Scale CMOS Devices

Toshiro Hiramoto and Masaharu Kobayashi

As the size of MOS transistors is miniaturized, the effect of random variability of device characteristics is becoming too large to be overlooked. Although the main reason in conventional bulk transistors is the fluctuation of the number of dopants, the variability causes of nanowire transistors, which is one of the next-generation device candidates, remain unknown. In this study, we have clarified that the quantum confinement fluctuation caused by line width roughness is the new origin of random threshold voltage variability. We are also investigating the effect on the drain current variability.

Low Temperature Characteristics of Nano-Scale CMOS Devices

Toshiro Hiramoto and Masaharu Kobayashi

The quantum computing has attractive much attention for a future computing technology that is fundamentally different from classical computing by CMOS circuits. In the quantum computing systems, conventional CMOS circuits are utilized to control quantum bits. Therefore, it is essential to clarify and model CMOS transistor characteristics at low temperature. In this study, we are studying the subthreshold swing of bulk and nanowire transistors. We are also evaluating the characteristics variability at low temperature.

Silicon Power Devices

Toshiro Hiramoto

Although new materials such as SiC or GaN are widely studied for power devices, silicon IGBT (Insulated Gate Bipolar Transistor) is still a mainstream device for power electronics in very wide range of rated voltages. In this study, we are pursuing the potential of silicon IGBT based on new concepts of IGBT scaling and double-gate IGBT.

Research on monolithic integration technology of embedded memory device using Sn-doped IGZO

Masaharu Kobayashi, Toshiro Hiramoto

Oxide semiconductor material such as IGZO has been used for flat panel display applications, and now becomes promising for integrated circuit applications because of its low temperature process, extremely low leakage current by wide bandgap, and its high voltage tolerance. Reliability characteristics can be improved by doping Sn in IGZO. In addition, mobility can be enhanced by the Sn-doped IGZO (IGZTO. In this study, we clarified the physical origin of the mobility enhancement in IGZTO. Widely distributed s-orbital wave function can flatten the potential fluctuation originated from cation disorder in IGZO. Furthermore, we demonstrated the stable endurance characteristics in IGZTO-capped ferroelectric HfO_2 capacitors. Finally, we developed co-integration process of IGZTO FETs and ferroelectric-HfO_2 capacitor at less than 400°C process, and demonstrated 1T1C memory cell operation, and predicted sub-ns operation by SPICE simulation.

Research on fundamental material properties of ferroelectric-HfO_2

Masaharu Kobayashi, Toshiro Hiramoto

Ferroelectric-HfO_2 is a promising material for next generation ferroelectric memory applications because of its high CMOS compatibility, ferroelectricity less than 10nm thickness, and high coercive voltage. In general, ferroelectric-HfO_2 appears in a poly-crystalline film, while conventional perovskite is formed in a single crystalline film. While out-of-plane polarization of ferroelectric phase grains are preferred for memory operation, however, it is not verified yet whether out-of-plane polar grains can align themselves or not in ferroelectric-HfO_2. In this study, we showed that in-plane polar (010) orientation is thermodynamically stable by ab-initio simulation. We also experimentally found that

FE-HfO_2 grains have in-plane polar (010) orientation by electron diffraction mapping method. However, by applying electric field, we found that FE-HFO_2 grains turn its orientation to (001) by the same method. We studied the kinetic pathway of the transition from in-plane to out-of-plane polar orientation by ab-initio simulation. We demonstrated that the transition can occur through the intermediate tetragonal phase only with an extra small energy. This result indicate that FE-HfO_2 can align its polar-axis to out-of-plane orientation in any 3D structure under the electric field.

Research on 3D ferroelectric/anti-ferroelectric transistor memory devices

Masaharu Kobayashi, Toshiro Hiramoto

Ferroelectric FET (FeFET) using ferroelectric-HfO_2 is a promising memory device for high density storage applications. A FeFET can work as a memory cell by itself just like NAND flash memory, FeFETs can also take 3D stack architecture for high density memory. In our previous work, we proposed oxide semiconductor-channel FET instead of conventional poly-silicon channel toward 3D stack FeFETs. We showed that short gate length and thin film thickness help to increase memory window, by simulation. In order to realize 3D FeFET, however, oxide semiconductor has to be conformally deposited in 3D trench structure. In this tudy, we developed conformal deposition process of InOx by ALD method in 3D structure. Based on the design guideline described above, we successfully fabricated a vertical channel FeFET and demonstrated its memory operation with memory window > 1V. Furthermore, we propose to use anti-ferroelectric gate insulator instead of ferroelectric, as anti-ferroelectric FET (AFeFET), and use half-loop hysteresis for efficient erase operation. We experimentally demonstrated the memory operation of the AFeFET. This work shows the feasibility of FeFET and AFeFET for 3D structure high density and low power memory.

Takagi Laboratory

(https://sites.google.com/g.ecc.u-tokyo.ac.jp/mosfet)

III-V Metal-Oxide-Semiconductor (MOS) FETs and the 3 dimensional integration

S. Takagi, Kei Sumita, Ryohei Yoshizu, Kasidit Toprasertpong, M. Takenaka

3D-integrated CMOS, in which transistors are vertically stacked, is expected to be a key device for future logic LSIs. In order to realize such stacked MOSFETs, channels such as III-V compound semiconductors and Ge are promising because they can be fabricated at low temperatures and are expected to have high mobility and injection speed. In our laboratory, we are investigating the realization of ultra-thin III-V-On-Insulator (III-V-OI) structures on Si substrates, and the performance improvement of III-V nMOSFETs using these structures aiming at application to 3D stacked CMOS. In this fiscal year, we established a novel model of thickness fluctuation (surface roughness) scattering, which is an important scattering mechanism that determines the electron mobility of thin-body channel MOSFETs, and shown that further mobility enhancement of InAs nMOSFETs is possible by improving the MOS interface roughness. Furthermore, we proposed a new method to evaluate the interface state density inside the conduction band of InAs at InAs MOS interfaces and experimentally demonstrated that the InAs MOS interfaces have excellent interfacial properties.

Ge Metal-Oxide-Semiconductor (MOS) FETs and the 3 dimensional integration

S. Takagi, Tsung-En Lee, Chia Tsong Chen, Xueyang Han, Kasidit Toprasertpong, M. Takenaka

We are investigating the technology to realize ultra-thin Ge-On-Insulator (GOI) structures on Si substrates, the performance improvement of high-performance GOI CMOS using these structures, and the device physics that determines the electrical characteristics, with the aim of applying

them to 3D integrated CMOS. In this fiscal year, we demonstrated that extremely-high hole mobility can be obtained even in ultra-thin body channels by introducing uniaxial strain through the thinning of a compressively-strained GOI structures, fabricated by the Ge condensation method. We also demonstrated that EOT can be reduced down to 1 nm with maintaining a low interfacial defect density in a TiN/Y2O3/SiGe gate stack structure with ultra-thin Y2O3 formed by atomic layer deposition (ALD).

HfO_2-based Ferroelectric devices

S. Takagi, Kasidit Toprasertpong, Xuan Luo, Makoto Kawano, Koichiro Iwashige, M. Takenaka

MOSFETs (FeFETs) using ferroelectrics with polarization reversal as gate dielectrics and FeRAM using metal sandwich structures (MFM structures) as memory cells are expected to be future devices for ultra-low power memory and logic. In particular, devices based on ferroelectric and anti-ferroelectric materials such as Hf1-x$ZrxO_2$ and ZrO_2, which have been discovered recently, are of great interest because of their extremely high compatibility with current Si CMOS technology. We are studying the properties of these ferroelectric thin films deposited by an ALD method, the device operation principle of FeFETs and the optimum device structures to realize excellent device characteristics. In this year, we demonstrated for FeRAM applications that MFM capacitors with Hf0.5Zr0.5O_2 films thinned to around 4 nm, which is expected to operate at low voltages, significantly improves dielectric reliability and enables more than 1014 write cycles at 1.2 V operation.

Reservoir computing based on ferroelectric devices

S. Takagi, Kasidit Toprasertpong, Eishin Nako, Zeyu Wang, R. Nakane, M. Takenaka

Reservoir computing has recently attracted attention as a AI computation method with computational load for learning. We have proposed that FeFETs and FeRAMs with memory-in-logic and nonlinear analog computation capabilities are promising hardware for physical implementation of reservoir computing. Thus, we are searching for methods to improve AI performance of reservoir computing based on ferroelectric devices by examining operating schemes and device characteristics. In this fiscal year, we demonstrated that AI performance can be improved by using combining original and inverted input data applied to the gate electrode. We also investigated the effect of FeFET degradation on AI performance, and found that AI performance can be maintained by updating weights even when FeFET memory characteristics significantly deteriorate.

Understanding of Si CMOS operation under ultra-low temperature for quantum computing application

S. Takagi, Minsoo Kang, Kasidit Toprasertpong, M. Takenaka

In quantum computing systems, Si CMOS circuits that can operate at cryogenic temperatures such as 4 K must be placed close to the qubit chip in order to improve the number of qubits. For this purpose, we are conducting experimental and theoretical studies to quantitatively describe the electrical characteristics of MOS transistors at cryogenic temperatures and to clarify their physical mechanisms. In this year, we experimentally evaluated the variation of sub-threshold swing from room temperature to 4 K for Si n-MOSFETs with different substrate concentrations and found that the values of sub-threshold swing can be quantitatively reproduced regardless of the substrate concentration by assuming both tail states and localized interface states existing near the band edge.

Takenaka Laboratory

(https://sites.google.com/g.ecc.u-tokyo.ac.jp/takenaka-lab/)

On-chip/Off-chip optical interconnect

Mitsuru Takenaka, Hanzhi Tang, Yuto Miyatake, Tipat Piyapatarakul, Kazuma Taki, Taketoshi Nakayama, Tomohiro Akazawa

We have been conducting research on optical interconnection and I/O of LSIs using silicon photonics and other technologies. We have successfully demonstrated a multi-bandgap III-V-on-insulator (III-V-OI) wafer using quantum well intermixing. As a result, passive waveguides, photodetectors, and optical modulators were monolilthically integrated on a III-V-OI wafer.

Si photonic integrated circuit for AI

Mitsuru Takenaka, Hanzhi Tang, Yuto Miyatake, Kohei Watanabe, Kazuma Taki, Mingzhi Huang, Akifumi Kurumatani

We have been conducting research on deep learning for AI using programmable photonic circuits such as universal optical circuits. We have demonstrated a non-volatile optical phase shifter in conjunction with a III-V/Si hybrid MOS phase shifter and ferroelectric FET.

Ge mid-infrared photonic integrated circuit

M. Takenaka, Ziqiang Zhao, Yuto Miyatake, Chao Zhang

We have been studying mid-infrared photonic integrated circuits based on Ge waveguides formed on Ge-on-insulator (GeOI) wafer. We have found that high-energy ion implantation of hydrogen into a Ge bulk wafer enables the low crystal defect density in the Ge device layer, resulting in obtaining an n-type Ge-OI wafer. As a result, a low-loss Ge waveguide was obtained using an n-type GeOI wafer.

2D material devices

Mitsuru Takenaka, Roda Nur, Tipat Piyapatarakul

We have been studying semiconductor devices using graphene and molybdenum disulfide. We have successfully demonstrated a phototransistor by bonding MoS2 on HfO_2 gate dielectric. Using hole traps in HfO_2, we achieved high responsivity through photogating effect.

Uchida Laboratory

(http://www.ssn.t.u-tokyo.ac.jp)

Nanoscale Molecular Sensors for Volatile Organic Compounds (VOC)

Ken Uchida

Human breath contains various kinds of volatile organic compounds (VOCs), in which metabolites related with diseases or health condition should be included. Therefore, we can expect that the very early diagnosis of the disease could be achieved, if VOCs related with human diseases can be selectively detected. We have experimentally demonstrated successful operations of low-power metal-nanosheet-based molecular sensors. However, atomistic-level simulation methodologies which can reproduce the response of molecular sensors have not been established. We have developed a new atomistic simulation method for molecular sensors by combining the molecular dynamics simulation and the nonequilibrium Green's function method. In future, the developed technique will be applied to various types of molecular sensors and the accuracy will be intensively checked to further improve the calculation technique and to find materials for new types of molecular sensors.

Thermal-aware Design of Nanodevices

Ken Uchida

LSI has drastically improved the performance by reducing the size of MOS transistors. Recently, the introduction of new three-dimensional device structure; nanosheet transistor, is expected, and the Joule-heating-induced temperature rise in device channel is suggested as one of the most serious prob-

lems. We have developed a technique to minimize the operating temperature of the CMOS channel by thermal-aware design. Moreover, detailed evaluations of the electron-phonon transport properties have been conducted in our group. The molecular dynamic simulation and the nonequilibrium Green's function method were simultaneously performed, and it is suggested that there are vibrational modes peculiar to the Si/SiO_2 interface, and that the vibrational mode enhances the electron-phonon scattering near the interface.

Someya-Yokota-Lee Laboratory

(http://www.ntech.t.u-tokyo.ac.jp/, https://fles.t.u-tokyo.ac.jp/)

Highly durable skin-applied electrodes for electrocardiographic measurement

Yan Wang, Sunghoon Lee, Tomoyuki Yokota and Takao Someya

We developed the world's thinnest and lightest skin attachable electrode which can measure electrocardiograms with high accuracy for one week. The skin attachable electrode was fabricated on a stretchable nanosheet that is ultra-thin, highly durable, highly adhesive, and breathable. The nanosheet can be attached to the skin without the adhesive materials. The very thin dimethylpolysiloxane was reinforced by several layers of polyurethane nanofibers to achieve excellent mechanical durability. In fact, it enables long-term measurement of health conditions in daily activities, and is expected to be applied as a wearable device for early detection of illness and poor physical condition in the medical and healthcare fields in the future.

Mita Laboratory

(http://www.if.t.u-tokyo.ac.jp)

TopoMEMS: Development of Ideal Variable MEMS in view of Future Topological Quantum Computing

Y. Mita, K.Tsuji, A.-C.Eiler,A.Higo, T.Iizuka, Z.Xu, M.Ezawa (Dept. Applied Physics)

Recently, new computation methods that use Topological nature are drawing much attentions in view of future Quantum computing. Calculation takes advantages Topological natures existing in several different fields expressed as Hamiltonian matrices. Our team, granted by JST CREST project, tries to explore electrical expression of Hamiltonian matrices used for computation. Team Mita will develop ideal variable electrical devices as well as ideal MEMS devices. We named such devices and systems “TopoMEMS”. As an initiating study, we have taken Su-Schriffer-Heeger model. We have developed a MEMS state-variable capacitor integrated SSH electrical circuit and have been successful in Topological / Trivial state switching due to MEMS device. The result has been presented in the top MEMS conference. Then, we have identified another interesting compu-tation scheme by directly using dynamics of MEMS. Towards that end, a bistable MEMS actuator has been developed and presetnted in an international conference.

Programmable Matter - Study on LSI-MEMS energy-autonomous distributed microsystems for realization of deformable matter

Y. Mita, K.Misumi, N.Usami (Dept. of Aeronautics and Astronautics),

E. Lebrasseur, G. Hwang (LIMMS, CNRS-UTokyo IIS / CNRS C2N),

G. Ulliac, (LIMMS, CNRS-UTokyo IIS, FEMTO-ST),

J.Bourgeois, B.Piranda (FEMTO-ST, France), S. Delalande (Groupe PSA, France)

As one example of future integrated MEMS that is expected to open new research and industrial appli-

cation fields, the authors are trying to show a top-down application of energy-autonomous dis-tributed microrobots. A number of identical tiny robots, sized below 1cm, will be released in an en-vironment. Individual robot can communicate with their neighbor, stick each other, and share ener-gy, to realize cooperative function. The PI is receiving a French National Research Center (ANR) grant on behalf of host professor of CNRS laboratory in the Institute of Industrial Science (LIMMS, CNRS-IIS, UMI 2820), together with FEMTO-ST Laboratory and PSA-Peugeot Laboratory for such "micro robots that can realize deformable substance by cooperative action, named Programmable Matter". In year 2020, an electrostatic chucking actuator system that attaches and detaches the external skeleton of the Matter has been presented in an international conference. Based on the actuation force electromagnetically ana-lyzed, the ideal structure of the flexible electrode (named Flexiboard) has been identified, and a reliable integration process with thinned high-voltage photovoltaic cells have been developed.

Integration of electrode devices on MEMS fluidic devices

Y. Mita, A.-C. Eiler, A. Higo, T.Ezawa, E.Ota, Y.Okamoto (AIST), N.Washizu (Advantest), A.Takada (Advantest), M. Fujiwara, T.Sawamura

Towards the goal of production of brand-new sensor devices with higher sensitivity and func-tionality, the team is working on small-gap electrode fabrication process. This year, we have newly acquired a Fully-Depleted SOI VLSI device for massively parallel measurement and its post-process have been developed.

Fine Large-Area Electron Beam Lithography Exposure Methods

A. Higo, Y. Ochiai, M. Fujiwara, T.Sawamura, Y. Mita

The team explores newly-acquired (in 2013) rapid electron beam writer F7000S-VD02. The capability of high electron dose and sharp edge due to cell (character) projection machine configura-tion is being examined. The breakthrough in question is to extend the large-area EB lithography, whose pattern approximation have been limited to rectangular shapes, into expressing free-form smooth shapes and a number of periodical small patterns. This year, pattern and process design has been successful to obtain gap structure less than 16-nm wide. The result has been presented in the top MEMS conference.

Universities-Industries collaborative research on highly-functional system by MEMS post-process of CMOS-VLSI

Y. Mita, T. Yamaguchi, T. Lévi(IMS-CNRS,Bordeaux), G. Larrieu (LAAS-CNRS,Toulouse), Y.Ikeuchi (IIS), K.Saito (Nihon Univ.)

The research targets are new sensor devices, made by post-process at clearnrooms such as d.lab Takeda Supercleanroom and others, of VLSI wafer made through VDEC. The important finding has been that VLSI wafer acquired just after transistor fabrication could sustain processes even with heat treatment, such as deposition, ion implantation, and drive-in. In 2016, a VLSI de-vice made on Silicon-on-Insulator (SOI) wafer was successfully Deep-RIE processed. The in-dustrial interest is its versatility – many different types of application devices, which differ one from another according to request of market, can be fabricated by using the same technology. More and more companies are interested in the scheme and are working on the technology on the col-laborative research projects, including international cooperative research projects. This year, a world's lowest-level (1.5V) soft microactuator with highest figure-of-merit has been developed and presented in the top MEMS conference.

High-sensitive ultrasonic probe by integrated MEMS technology

Y. Mita, A.Higo, T.Yoshimura (Osaka Prefectural Uni-

versity), T.Mizuno (Konika Minolta), K.Suzuki (Konika Minolta), Y.Nakayama (Konika Minolta), T.Endo (Nagoya Medical Center)

Using the same scheme as above mentioned CMOS-MEMS post process R&D scheme, this project aims at integrating piezoelectric material and MEMS post-processing to obtain a brand-new ultrasonic inspection probe, whose sensitivity is as 100 times as cutting-edge technology. In year 2020, the team investigated LSI test circuit of high-voltage electronic circuit, fabricated by support from a public funding from Japan Agency of MEdical Research and Development (AMED). This year, the fully-integrated system has been investigated.

Test Structure for high-density CMOS-MEMS hybrid integrated Technology

Y.Mita, Y.Ebihara, A.Mizushima, T.Yoda (TITech), K.Hirakawa (TITech), M.Iwase (TITech), M.Ogasawara (TITech), A.Higo and Y.Ochiai

Chip-level highly-dense bonding integration is drawing high attention to simply obtain high-functional system; it has been almost impossible to individually examine pad-to-pad connec-tions, whose size is in an order of several microns and whose number is order of 1 million. New test structures and methods are mandatory. We have proposed a two-pads-per-probe scheme, in which one of the pad is used for testing pad to make what we call “loop-back test”. A test LSI have been designed, fabricated, and integrated with gold bumps as well as MEMS test structures. The failure mode has been emulated and successfully verified. The result has been presented in an international conference.

Appendix

A.1 VDEC CAD Tools

Since 1996, VDEC has provided CAD software licenses to the registered researchers in universities and colleges in Japan. The CAD tools we provided in 2022 through the activities of VDEC in Systems Design Lab (d.lab) are shown in Table A.1.1. The researchers can use those CAD tools when their local machines, whose IP addresses are registered in advance, are authorized by one of VDEC license server located in the ten VDEC subcenters shown in Figure A.1.1. For each CAD tool, VDEC provides 10-100 floating licenses. Those CAD tools can be utilized only for research and education activities in national universities, other public universities, private universities, and colleges.

When one is going to use VDEC CAD tools and chip fabrication service (the details are described in Section 1-3), some faculty member of his/her research group in a university or a collage needs to do user registration. Figure 1.2.2 shows (a) the number of registrants, (b) the number of distinguished universities/colleges of the registrants, and (c) the number of registrants who applied VDEC CAD tools, (d) the number of applied licenses of all CAD tools.

Table A.1.1 VDEC CAD tools

Name	Function	Vendor
Cadence tool set	Verilog-HDL/VHDL entry, Simlation, Logic synthesis, Test pattern generation, Cell-based (including macros) place, route, and back-annotation, Interactive schematic and layout editor, Analog circuit simulation, Logic verification, Circuit extraction	Cadence Design Systems, Inc.
Synopsys tool set	Verilog-HDL/VHDL simulation, Logic synthesis, Test pattern generation, Cell-based (including macros) place, route, and back-annotation, Circuit simulation, Device simulation	Synopsys, Inc.
Mentor tool set	Layout verification, Design rule check	Mentor Graphics Co. Ltd.
Silvaco tool set	Fast circuit simulation	Silvaco
ADS/Golden Gate	Design and verification of high-frequency circuits	Keysight Technologies
Bach system	BachC-based design, synthesis, and verification	Sharp
LAVIS	Layout visualization platform	TOOL

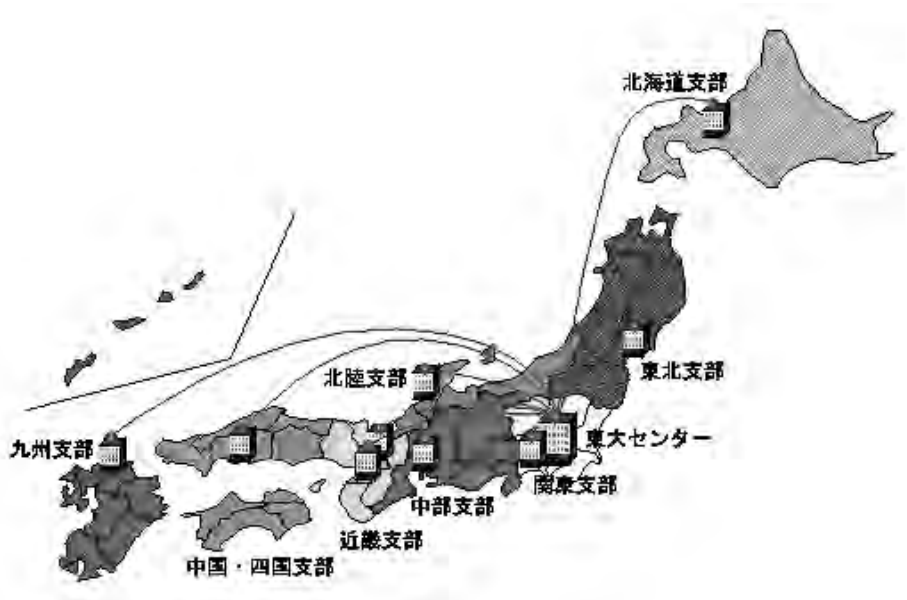


Fig. A.1.1 VDEC Subcenters

Table A.2.1 Chip fabrication schedule in 2021

0.8μm CMOS (On-Semiconductor - Sanyo)

	Chip application deadline	Design deadline	Chip delivery
2021#1	2021/7/5	2021/9/27	2022/2/1
2021#2	2022/1/11	2022/3/28	2022/6/16

0.18μm CMOS (Rohm)

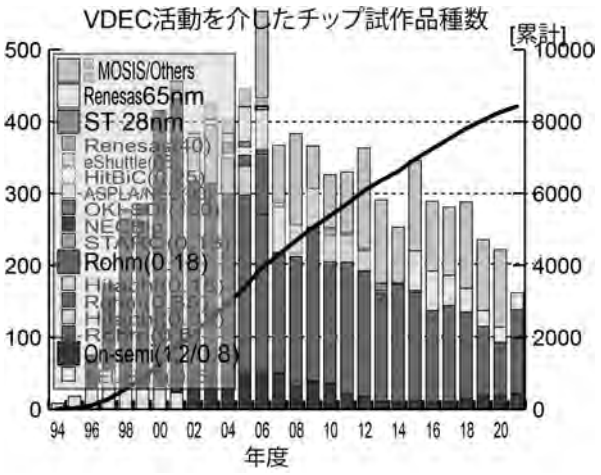
	Chip application deadline	Design deadline	Chip delivery
2021 #1	2021/4/5	2021/6/28	2021/9/21
2021 #2	2021/6/14	2021/9/6	2021/12/24
2021 #3	2021/8/4	2021/10/27	2022/2/13
2021 #4	2021/12/6	2022/2/28	2022/6/10

SOTB 65nm CMOS

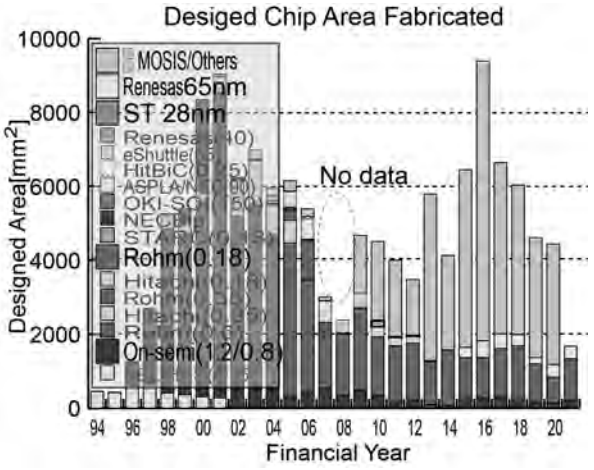
	Chip application deadline	Design deadline	Chip delivery
2021 #1	2021/6/14	2021/7/26	2022/1/28
2021 #2	2022/1/24	2022/3/7	2022/8/27(est)

A.2 Status of Chip Fabrication Support at Platform Design Research Division

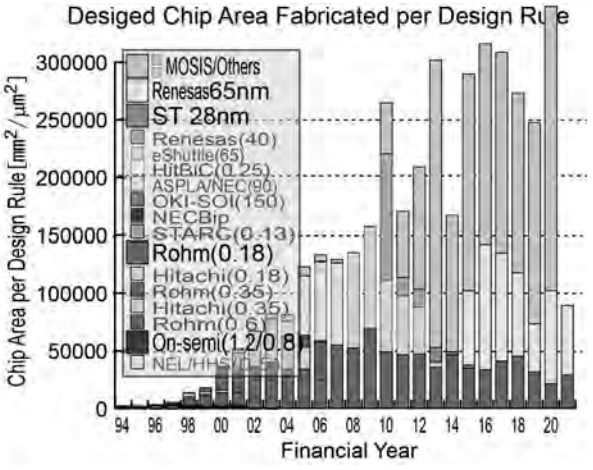
As for the support for VLSI chip prototyping, in the pilot project in FY 1994 and 1995, there was only one foundry, NEL's CMOS 0.5μm (the process was later continued by Hitachi Hokkai Semiconductor). After the inauguration of VDEC in 1996, the 1.2-μm CMOS process of Motorola Japan (which was continued by ON Semiconductor in 1999) started cooperation, and the 0.6-μm CMOS process of ROHM was added in 1997. In 1997, CMOS 0.6μm from ROHM was added, followed by 0.35μm from Hitachi, Ltd. in 1998, and 0.35μm from ROHM in 1999. In addition, as part of the IP development project, a prototype of STARC 0.13μm was developed. Since FY 2001, we have been providing services of CMOS 0.18μm from Hitachi, Ltd. In 2002, under the leadership of Dr. Iwata of Hiroshima University, we conducted a trial trial fabrication service in cooperation with VDEC and MOSIS. This service provides overseas fabs such as TSMC and IBM at low cost through MOSIS. Furthermore, under the leadership of Dr. Shibata of the University of Tokyo, NEC Compound Device, Inc. provided a prototype service for bipolar LSI. In 2004, we started prototyping Oki Electric CMOS SOI 0.15μm process and ASPLA 90nm process as test prototypes, and the 90nm prototype was operated as a regular prototype from 2005 in the form of public solicitation. In FY2006, we started trial production of 0.18μm process by ROHM and test production of 0.25μm SiGeBiCMOS by Hitachi, Ltd. In FY 2007, we started to study an advanced process to succeed 90nm CMOS, which was terminated in FY 2007, and in FY 2008, we started trial production of eShuttle's 65nm CMOS. In addition, as part of the METI-STARC project "Next Generation Semiconductor Circuit Architecture Commercialization Support Project," prototype production using Renesas Electronics' 40nm CMOS was also started. On the other hand, CMOS1.2μm was terminated in September 2011, Renesas Electronics' 40nm CMOS prototyping was terminated in 2012, and eShuttle's 65nm CMOS prototyping was terminated in August 2013. As a successor to CMOS 1.2μm, a test prototype of



(a) Trend of number of designs fabricated.



(b) Trend of designed area.



(c) Trend of designed area normalized by design rule

Figure A.2.1 Trend of number of designs and designed chip area.b

CMOS 0.8μm was conducted in October 2012 with the cooperation of Onsemi-Sanyo Semiconductor Manufacturing Co. As for the leading-edge prototyping, STMicroelectronics started FD-SOI 28nm CMOS prototyping through CMP of France in FY 2013. In addition, we started SOTB 65nm CMOS prototyping by Renesas Electronics as a regular prototyping in FY2015. In FY2021, we started BiCMOS 0.18um prototypes under an agreement with IHP of Germany.

Fig. A.2.1(a) shows trends of number of chip designed for VDEC chip fabrication. For the first 6 years until 2001, the number of designed chips shows steady increase, which means drastic improve of the effectiveness researches and education of LSI design, and we assume drastic increase of number of students related to LSI chip design and education. During few years of stable number around 400 chip designs per year, we can see transition of designs toward finer process. In 2007, we saw a large drop, which was caused by sudden process transition from 0.35 μ m CMOS to 0.18 μ m CMOS, and in 2008, we also saw another drop by process transition from 90nm CMOS to 65nm CMOS.

Fig. A.2.1(b) shows trends of designed chip area, which shows much clear trends of drop by process migration. On the other hand, Fig. A.2.1(c) shows trends of designed chip area normalized by design rule, which assume to be strong relation with design efforts. Coming from the fact that the normalized chip area is still growing, we assume the major reason for decrease of number of chips and designed area is increase of design effort per chip and per unit area due to process scaling.

Fig. A.2.2 shows trends number of professors and universities fabricated chip. Number of professors who have contracted NDA for process technologies to access design rules and design libraries are, 92, 287, and 49, respectively, for 65nm CMOS, 0.18 μ m CMOS, and 0.8 μ m CMOS.

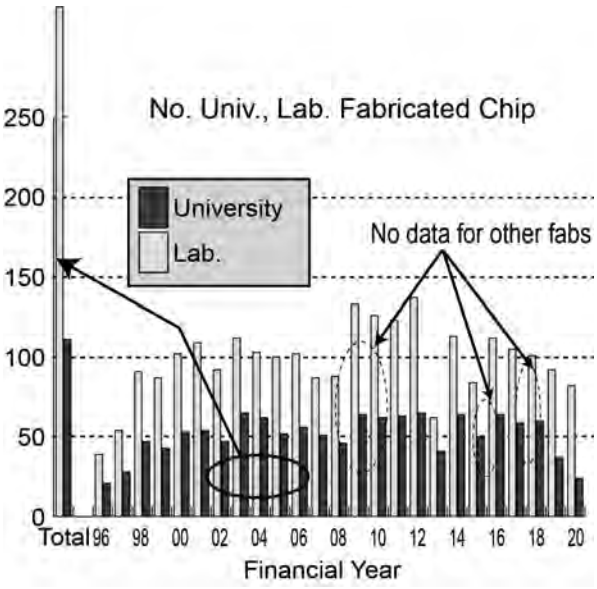


Figure 2.3.2 Trend of number of processors and universities fabricated chip.

A.3 Seminar

Seminars are always needed as the advancement of LSI design technology. In 2021, VDEC has held CAD Seminar, Refresh Seminar, and Designer's Forum, for academic and industrial circuit designers. In this fiscal year, all the seminars were held online due to the pandemic of COVID-19.

A.3.1 CAD Seminar for VDEC users

Along with advancement of circuit design CAD tools, tutorials on these tools are highly demanded. VDEC offers the CAD Seminar twice per year. In the CAD Seminar, VDEC invites lecturers from venders including Cadence, Synopsys and Keysight to give tutorials on their CAD tools. The seminar is held in VDEC, The University of Tokyo and VDEC sub-centers simultaneously in several universities nationally, August, September, and March of one fiscal year. Each tutorial takes one or two days.

Table A.3.1 CAD technical seminar in 2021 fiscal year

CAD Seminar I

Date	Tutorial	Venue	Attendees
8/3	Keysight Empro	Online	40
8/17	Synopsys IC Compiler-II	Online	41
8/24	Synopsys IC Validator	Online	40
8/30	Cadence Virtuoso Schematic, Layout	Online	22
9/22	Synopsys Custom Designer	Online	6
Until 9/30	Cadence Innovus	On-demand	12
Until 9/30	Keysight Empro	On-demand	12

CAD Seminar II

Date	Tutorial	Venue	Attendees
3/4	Cadence Innovus	Online	31
3/8, 9	Cadence Layout (GXL, EAD)	Online	58
3/11	Cadence EMX	Online	34
3/15, 16	Cadence SKILL	Online	37
3/29	Synopsys TCAD Q&A Meeting	Online	29
Until 3/31	Synopsys Design Compiler	On-demand	65
Until 3/31	Synopsys ICC-II	On-demand	61
Until 3/31	Synopsys TCAD	On-demand	38

A.3.2 Refresh Seminar for industry and academia

The fundamental and advanced knowledges are both imperative to integrated circuit design. VDEC offers the Refresh Seminar for industrial and academic people. University professors and highly experienced engineers are invited to give lectures on circuit design, covering the topics on analog, digital, RF, MEMs, and basic design flow. The seminar was originally launched in 1998, with the support of Ministry of Education Technical Education Division. It is now being supported by several industrial/academic societies.

Fig. A.3.1 Refresh Seminar at VDEC seminar room at the University of Tokyo, VDEC.

Fig. A.3.2 Screen shot of Refresh Seminar online.

Table A.3.2 Refresh Seminar

Date	Course	Contents	Lecture	Attendees
5/31, 6/1	CMOS-RF Circuit Design	Modulation/Demodulation Cascaded connection Basic Performance Transceiver Architecture Circuit Element Design Flow	Hiroyuki Ito (Tokyo Inst. of Tech.)	20
8/11, 12	VDEC Digital Circuit Design Flow	Digital circuit design flow using VDEC-collaborated CAD environment and process	Kazutoshi Kobayashi (Kyoto Institute of Technology)	44
8/25, 26, 27	Analog Circuit Design	Analog Circuit Design and simulation Integrated Circuits Verification (LVS, DRC)	Masahiro Sugimoto (Chuo Univ.) Tetsuya Iizuka (The Univ. of Tokyo) Koji Kotani (Tohoku Univ.)	67
9/2, 3	Transistor-Level Circuit Design Flow	Custom circuit design flow using VDEC-collaborated CAD environment and process	Toru Nakura (Fukuoka Univ.)	23

A.3.3 Designer's Forum for academia

VDEC LSI designer forum intended for students and young teachers were held. The VDEC LSI designer forum has aimed to sharing the information that generally hard to be obtained common technical reports or academical papers, such as the failure an LSI designer had been through and the solution, and the construction method in the design milieu in the laboratory.

Table A.3.3 Program of Designers Forum in 2021

9/24 Online Attendees: 54	
9/24	
9:30	Reception
10:00 – 10:15	Opening
10:15 – 11:15	Idea Contest Presentation
11:15 – 12:30	Lunch
12:30 – 13:30	Keynote Speech
13:30 – 13:40	Break
13:40 – 15:00	Design Award Presentation I
15:00 – 15:10	Break
15:10 – 16:30	Design Award Presentation II
16:30 – 16:40	Break
16:40 – 17:40	Design Award Presentation III
17:30 ~	Voting and Award Ceremony

A.4 Venture companies related to VDEC

Some professors related to VDEC started venture companies. The following is a list of the venture companies related to VDEC.

[1] AIL Co.,Ltd. (http://www.ailabo.co.jp/)

Related professor : Professor Kazuo Taki, Kobe Univ. (Representative Director)

Description of business : (1) LSI design service
(2) Engineer dispatching service
(3) Recruitment
(4) Management consulting

[2] Synthesis Corporation

(Merged with Soliton Systems on July 1st in 2017, http://www.synthesis.co.jp/)

Related professor : Professor Emeritus Isao Shirakawa, Osaka Univ. (Director)

Description of business : (1) System LSI development and design service
(2) IP development and sales
(3) Development and sales of IPs
(4) Development of EDA tools

[3] ASIP Solutions (http://www.asip-solutions.com/)

Related professor : Professor Masaharu Imai (Representative Director, CTO)

Description of business : (1) R&D, education and consulting of IoT application system
(2) Sales of ASIP design tool and consulting of ASIP development

[4] Nanodesign Corporation (http://www.nanodesign.co.jp/)

Related professor : Professor Kazuyuki Nakamura, Kyushu Institute of Technology. (Rep-resentative Director)

Description of business : (1) LSI design and development
(2) Development of LSI CAD and LSI evaluation tools
(3) Design consulting, etc.

[5] A-R-Tec Corp. (http://www.a-r-tec.jp/)

Related professor : Professor Emeritus Atsushi Iwata, Hiroshima Univ. (Representative Director)

Description of business : (1) Analog IC design and measurement
(2) PCB noise analysis
(3) Develop human resources, OJT, Lecture

[6] Ishijima Electronics (http://ishi.main.jp/)

Description of business : (1) Electronic circuit and board development
(2) Software development
(3) Consulting

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