Systems Design Lab

東京大学大学院工学系研究科
附属システムデザイン研究センター
先端設計研究部門・先端デバイス研究部門
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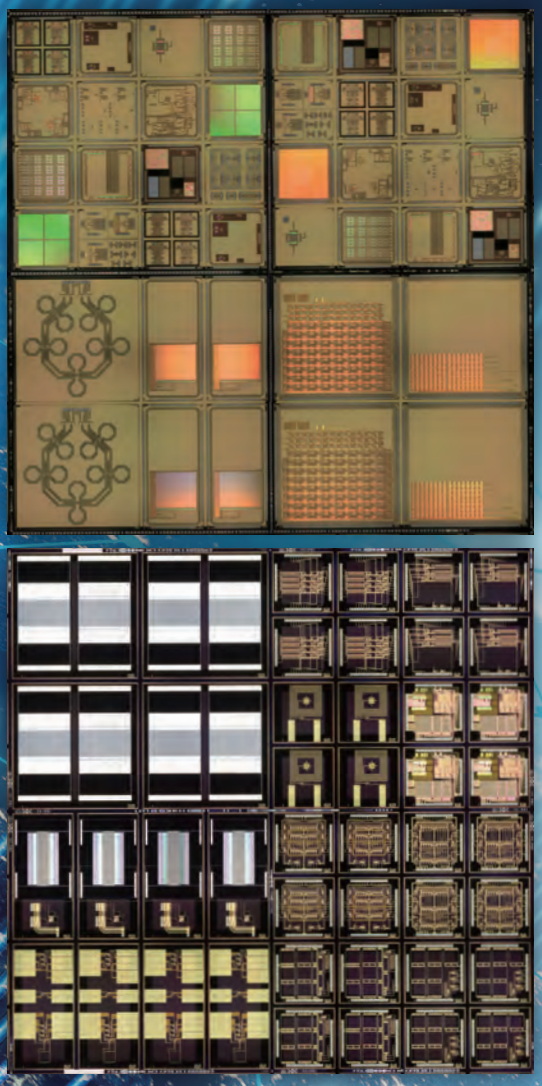
Systems Design Lab, School of Engineering, (VLSI Design and Education Center), The University of Tokyo
Annual Report



Systems Design Lab, School of Engineering
The University of Tokyo 2023

Message from the Director of d.lab

Tadahiro Kuroda

Director
Systems Design Lab (d.lab)
School of Engineering, The University of Tokyo

The book ***Chip War*** by Chris Miller has won a wide audience. As its subtitle of *The fight for the world's most critical technology* suggests, it depicts in detail the history of the battles between nations in the area of semiconductors.

But ***Chip War*** describes only one scenario; there are other possibilities for the future. That was the motivation for me to write the book that I originally called *Semiconductor Democracy*. The book was eventually published in Japanese with the modified title of *The Super-Evolution of Semiconductors – The Future of the Technology that Dominates the World*.

The future described in the book is as follows.

◇◇◇◇◇◇◇◇(Translated from the Postscript)

Semiconductor democracy and chip war are two sides of the same coin. In this book, my focus is on semiconductor democracy.

In the 19th century, Otto von Bismarck explained in a speech how iron made a nation. Indeed, iron created contemporary cities and gave birth to weaponry.

Today, the technology battleground is in semiconductors. Semiconductors make a nation. What will semiconductors create, and what will they break? It will be up to our imagination and wisdom.

Chip makers are engaged in fierce battles to dominate in the manufacturing of next-generation semiconductors.

However, semiconductors are evolving into such a giant collection of technologies that the challenges can no longer be overcome by a single corporation or even a single country. We really should think of semiconductors as a global commons.

As a result, we should not be instigating semiconductor wars; instead, we need to be building ecosystems.

Technology is getting more and more complex. Therefore, we must look at the entire forest instead of the individual trees. The challenge ahead for the world is how to nurture the forest, or in other words, create a rich industrial ecosystem.

We can take hints from the botanical world.

Nowadays plants flourish everywhere across the globe. The revolution that created the world of today was started by flower-bearing plants.

A co-existence relationship born between flowers and insects resulted in their co-evolution where one evolved by promoting evolution in the other, and vice versa.

The birth of flowers provided the trigger for the accelerated evolution of life forms.

According to Darwin's theory of evolution, only the fittest survive and are able to continue their family lines. In a nutshell, life is about competition. However, the hidden mechanism of evolution that is being uncovered by the latest science is that living organisms not only compete with each other but also cooperate to help each other. That is the essence of the theory of super-evolution.

Similarly, to enrich the "semiconductor forest," it is important to find its "flower." It was with that thought in mind that I set forth my theory of the super-evolution of semiconductors in this book.

I started by describing how high-performance semiconductors are developed from the standpoints of More Moore and More than Moore.

Next, I shared my thoughts on what high-performance semiconductors can create from the standpoint of innovation, or in other words, the standpoint of More People.

Will we be able to find the "flower" that is needed to evolve semiconductors from the age of competition to the age of co-existence and co-evolution? It is going to take more than capital and Moore's Law to make semiconductors a global commons.

The need is to get many people involved. That is More People.

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One other point I would like to bring up is agility.

◇◇◇◇◇◇◇◇(Translated from Chapter 1, Section 4, "The Semiconductor Forest: Co-existence and Co-evolution")

Eventually, flowers acquired new power.

It was the shortened lifecycle. The time from pollination to fertilization was shortened from one year to a few hours. That resulted in accelerated evolution of all life forms.

$y = a(1+r)^n$

That is the formula for calculating compound interest, where r is the interest rate and n the number of times interest is compounded. Even if you start with a small principal a, the future value can grow large if you continue the compounding for a long time.

If you replace n with $1/t$, where t is the development cycle time, you get the fundamental equation for the digital economy. The same equation applies to both the improvement in chip performance and the growth of a company.

Put differently, the strategy to grow the digital economy is to repeatedly iterate the improvement cycle at high speed. Rather than the amount of improvement (r), the key is to increase the number of times improvement is made (n), or in other words, reduce the development cycle time (t).

That is why we want to be agile.

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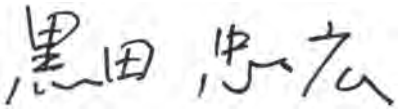
The book presents the fundamental thinking of d.lab. I would appreciate it if you would get hold of a copy and give it a read.



Systems Design Lab

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C O N T E N T S

Chapter 1 Introduction to d.lab

The VLSI Design and Education Center (VDEC) was established at the University of Tokyo in 1996. At the time of its founding, Japan's semiconductor industry held a 50% share of the USD 50-billion global market, and engineers who could hit the ground running were in high demand. VDEC has since provided unparalleled, outstanding education to develop many high-caliber engineers for the semiconductor industry.

However, have these graduates of VDEC been able to fully realize their potential? In the last quarter century, even though the global semiconductor market enjoyed a rapid 7% annual growth rate, Japan's share continued to shrink, falling to the current level of about 10% of a market that is now approaching USD 500 billion.

The current semiconductor business is one of mass production of high volume, low margin general purpose chips. General purpose chips have been able to achieve large volumes because of the wide adoption of the von Neumann computer architecture constructed with the combination of memory and processor chips. While Japan led the world in memory device innovation, it lost the business competition on capital investment.

The mass production, mass consumption model has its limits. Because of the excessive burdens it places on the environment, the world is now facing an energy crisis. The recent trend of applying AI to big data analysis is fueling further growth in energy consumption.

In the middle of this development, a game changer has emerged. Recognizing that it is hard to compete by using general purpose chips procured from semiconductor makers, technology giants including GAFA have started to develop their own specialized logic chips in-house.

In response to this paradigm shift, the University of Tokyo established the Systems Design Lab (d.lab) in October of 2019 and formed a strategic alliance with TSMC a month later. d.lab was formed by establishing the Advanced Design Research Division and the Advanced Device Research Division and adding them to the existing Platform Design Research Division and Platform Device Research Division which had been operating VDEC and the Takeda Clean Room. Subsequently in October of 2020, d.lab started an industrial partnership program which has grown to include more than 40 corporate members.

Furthermore, the Research Association for Advanced Systems (RaaS) was founded in August of 2020 to lay out the framework for the university to collaborate with both the industry and the government. Using d.lab and RaaS to realize a two-pronged strategy of open and closed collaboration respectively, the university is actively promoting cooperation between academia and society as well as collaborative creation with industry. Our research aims to boost the time-performance of semiconductors, with target goals of 10x increase in both energy and development efficiencies.

Japan is aiming to transition from the current industrial/information society to Society 5.0, a human-centric society where knowledge is value. In this knowledge-based society, semiconductors will evolve from being a necessity of industry to the brain cell of society.

What strategy should the semiconductor industry pursue to address this evolution? It is d.lab's mission to find the answer.

Tadahiro Kuroda
Director, Systems Design Lab

Chapter 2 d.lab Overview and FY2022 Annual Report

2.1 Advanced Design Research Division

2.1.1 Division Overview

The Advanced Design Research Division faculty consists of four professors, one associate professor, one lecturer, one project professor, one senior fellow, and one project researcher (joint appointments included). Its goal is to enable the design of integrated circuits with both high energy efficiency and high design efficiency.

In August 2022, NEC Corporation, the University of Tokyo, and Canon Inc. were selected to undertake the research and development of versatile high-level synthesis technology and novel general-purpose, data-flow computing mechanism by the New Energy and Industrial Technology Development Organization (NEDO) under its Project for Innovative AI Chip and Next-Generation Computing Technology Development, R&D Area 4: Technology Development to Accelerate Industrial Application of AI Edge Computing. The research is scheduled to be completed by March 31, 2025.

In addition to its research effort, the Advanced Design Research Division has two organizational responsibilities. First, it operates the d.lab Partnership Program with help from other d.lab divisions. Second, it operates the Research Association for Advanced Systems. The following section is the FY2022 report on these two operations.

2.1.2 d.lab Partnership Program Activities

The d.lab Partnership Program was launched in FY2020 to establish an international center of knowledge-value where system designers and members of the semiconductor industry meet to exchange information and ideas and to engage in open discussion of collaboration between academia and society. The Program aims to create a hub that brings together ideas from system designers in industries including IoT, AI, 5G, automated driving, and healthcare, advanced semiconductor technologies such as advanced CMOS processes and 3D integration technologies, as well as enablers of such technologies including materials and manufacturing equipment. In FY2022, a total of 49 corporations joined the Program, which is 6 more than the prior year. Table 2.1.1 contains the list of FY2022 corporate members. We would like to thank these members again for their participation.

In FY2022, because COVID-19 restrictions had eased off to a certain extent, in addition to organizing various seminars in the form of webinars as in previous years, we were able to pursue our original vision of not only sharing the research accomplishment of d.lab, but also hosting events to enable program members to interact with renowned professors and students from the University of Tokyo, with universities and research organizations from around the world, and with other industrial executives and leaders, as well as events to share information and knowledge from international conferences and introduce and experience the most advanced technologies from the likes of TSMC. The remainder of the section summarizes the Partnership Program activities of FY2022. As in previous years, our activities spanned almost the entire year from May 2022 to March 2023. Table 2.1.2 summarizes the seminars we held in FY2022.

We held our Program kickoff meeting of the fiscal year on May 25, 2022, which also featured special presentations by some of the young researcher winners of the 2021 MIT Technology Review Innovators Under 35 Award. Specifically, three of the young researchers gave talks on next-generation electronics technology, followed by a presentation summarizing the Program activities planned for the year. The first presenter was Motion Lib CEO Takahiro Mizoguchi. Dr. Mizoguchi and his company have developed real haptics technology to control touch sensations and strength adjustment, as well as the ABC-CORE chip at the core of the technology. He discussed their business of helping to solve the labor shortage problem through the use of robots capable of performing delicate tasks.

The second presenter was Dr. Takuya Sasatani, project assistant professor from the Graduate School of Engineering at the University of Tokyo. He has developed technology to provide wireless charging across the space of an entire room. His presentation focused on the research and development of applied technology based on wireless charging

technology for the realization of a cable-free lifestyle.

The third presenter was Dr. Atsutake Kosuge, lecturer from the Systems Design Lab of the Graduate School of Engineering at the University of Tokyo. He is developing ultra-low power AI chip technology. His talk discussed AI sensing technology that enables the widespread adoption and advancement of automation in the field, including factories and construction sites, in order to solve the labor shortage challenges faced by an aging society. He was followed by Professor Tadahiro Kuroda, Director of d.lab, who provided a preview of the FY2022 d.lab Partnership Program activities.

On Jun 22, as a follow-up to our event in Jan 2021, we held an IBM Day to introduce IBM Albany and provide an update on IBM's quantum computing development. This was a hybrid event where, in addition to the normal webcast, we added an onsite visit to IBM's Shin-Kawasaki Facility "Shin-Kawasaki Souzou no Mori." We arranged a tour of a working quantum computer both before and after the presentations. The event also featured a poster session. Regarding IBM Albany, Dr. Shintaro Yamamichi from IBM provided a technology update on the research and development of advanced AI core, chip, and packaging at the IBM AI Hardware Center, as well as explaining how to participate in the development. Regarding IBM quantum computing, Mr. Daiju Nakano and Mr. Norie Iwasaki from IBM introduced its technology and roadmap, as well as its construction of an ecosystem including hardware.

On Jul 20, we hosted a seminar to report on the 2022 IEEE 72nd Electronic Components and Technology Conference (ECTC2022). The conference is organized by the IEEE Electronics Packaging Society to provide a forum for wide ranging discussion of the science and technology of packages, components, and microelectronics systems. It is one of the world's long-established and foremost international conferences, held for the 72nd time last year. It was held onsite for the first time in 3 years. The technology program covered the latest achievement in development and innovative technologies from across the full spectrum of packaging technology. Its main topics included advanced packaging, modeling and simulation, photonics, interconnection, material and process, reliability, manufacturing technology, components and RF, as well as emerging technologies. In our report, we focused on the latest trends and topics in advanced packaging technology that is mainstream for our current activities, and hybrid bonding that is a next-generation core technology.

On Aug 25, we held another seminar to report on the 2022 IEEE VLSI Symposium on Technology & Circuits, which took place from Jun 12 to 17 in Honolulu, USA. Since 1987, this has been a premier international conference for the microelectronics industry on state-of-the-art semiconductor device and process technology, as well as semiconductor circuit technology, jointly held by the IEEE Electron Device Society/Solid State Circuits Society and the Japan Society of Applied Physics (sponsored by the Institute of Electronics, Information and Communication Engineers). Its location alternates between Kyoto, Japan, and Honolulu, USA. In 2022 it was held in the US. (Because of COVID-19, it was held onsite for the first time in 3 years.) With "Technology and Circuits for the Critical Infrastructure of the Future" as its theme, the program covered the latest technology in advanced logic CMOS, memory, image sensor, photonics, machine learning, AI, digital, communication, and analog. Topics discussed also included the development and realization of future technology, as well as how to foster the next-generation professionals. We focused our report on the technology trends and topics in the areas of circuit, communication system, AI, machine learning, advanced CMOS, memory, and 3D integration.

On Oct 26, as a continuation from the year before, we held a technology exchange meeting for our corporate members. By popular demand, the event this year was held onsite at Takeda Hall on the 5th floor of Takeda Building. Thirteen of our corporate members who expressed interest in a panel exhibition delivered a short presentation, followed by a poster session in the foyer. As the organizer, we were delighted to be able to provide a forum for our members to interact and network.

On Nov 29, we organized a tour of the TSMC 3DIC Center together with another onsite member networking event. The TSMC Japan 3DIC R&D Center is the first overseas R&D center established by Taiwan Semiconductor Manufacturing Company (TSMC) outside of Taiwan. Guests including high-ranking government officials were invited to the opening ceremony held on Jun 24, 2022. Given the increasing importance of backend processing, including 3D implementation, the Center aims to pursue R&D of the most advanced 3D IC implementation in

collaboration with materials and semiconductor equipment manufacturers, research institutions, and universities in Japan. The event was made possible thanks to the kind cooperation of the TSMC Japan 3DIC R&D Center. The event started with a presentation by the Center at the Tsukuba International Conference Center, located close to the Tsukuba Central Station and in the vicinity of the Center. Afterwards, participants were divided into 3 groups to take turns to visit the Center. The tour took the participants up to the state-of-the-art clean room and provided an introduction to the latest technology.

To realize further improvement in advanced semiconductor performance, it is essential to simultaneously advance both device scaling technology and advanced packaging technology, the latter exemplified by chiplet. On Dec 13, continuing from the year before, we held an imec Day where we invited leaders of imec, who are driving these technology areas, to introduce to us the world's most advanced 3D system integration technologies. It provided a great opportunity to hear live from imec as the world authority in this domain. We were lucky to have Dr. Naoto Horiguchi, imec Logic CMOS device program director, discuss "Future CMOS device scaling by 3D architectures," and Dr. Eric Beyne, imec Senior Fellow, VP R&D, Program Director 3D System Integration, present on "3D Integration Technology: Enabling Heterogeneous System Scaling."

At the beginning of the year on Jan 18, 2023, we held a seminar to report on IEDM2022. IEDM (International Electron Devices Meeting) is the world's top international conference on device technology organized by IEEE. The conference was held in a hybrid format – allowing both in-person and on-demand access – from Dec 3 to 7. In our meeting, faculty members from d.lab provided an overview of the conference and discussed the latest trends in device technology, focusing on advanced CMOS device technology and materials, non-volatile memory technology, computing technology, and 3D integration technology.

In recent years, the debate over the end of Moore's Law has become increasingly serious, and the development of chiplet and 3D IC semiconductor packages more concrete. As the integration level of semiconductor packages increases, in addition to high-performance, the materials used must be compatible with the process, which is difficult to achieve. On Feb 8, we held a d.lab Materials Seminar where we introduced thermal control technology and the latest packaging technology, as well as d.lab's materials strategy. At the seminar, Prof. Masahiro Nomura from the Institute of Industrial Science at the University of Tokyo discussed "The Key to Semiconductors Thermal Solution: The Physics of Heat Transfer and Thermal Flow Control Technology," while Mr. Hidenori Abe, senior director from Resonac, presented on "Semiconductor Materials Development at the New Resonac, a Chemical Company Based on Co-creation." In addition, Mr. Kazunori Yamamoto, project researcher from d.lab, described the "New Semiconductor Packaging Materials Strategy Envisioned by d.lab."

We ended our FY2022 seminar series with a meeting on Mar 15, 2023, to report on the 2023 International Solid-State Circuits Conference (ISSCC2023). ISSCC celebrated its 70th anniversary this year. In addition to ever more engaging discussion of processor technology for machine learning, there were many presentations on imaging devices and memory, which are strongholds of the Asian region. ISSCC is the top international conference on IC technology held in February. Based on what was seen at the conference, Prof. Makoto Ikeda, who has been for years the chair of ISSCC's technology program, and other faculty members of d.lab discussed the latest trends in IC technology that will likely be driving the semiconductor industry going forward.

In FY2022, while carefully monitoring the development of COVID-19, we organized a mix of remote seminars and in-person events. We were able to incorporate entirely new activities like the tours of IBM and TSMC. In FY2023, we plan to continue to organize events to promote active intellectual exchange between our Program members and the university community, as well as exchange among our Program members.

2.1.3 Research Association for Advanced Systems Activities

The Research Association for Advanced Systems (RaaS) was established on Aug 17, 2020. The goal of RaaS is to increase 10-fold the development efficiency of specialized chips, which are indispensable in a data-driven society, by constructing a design platform for such chips and by adopting an open architecture for hardware design. In addition, RaaS aims to increase 10-fold energy efficiency by

researching and developing 3D integration technology and by stacking multiple chips manufactured in the latest 7nm CMOS technology in a single package.

RaaS believes that the driver of the semiconductor industry is once again swinging back from general purpose to specialized chips, against the backdrop of the unique energy crisis of the data society. The crisis is being spurred by the exponential growth in data and the increasing sophistication of AI processing. On the current trajectory, IT equipment alone is expected to consume close to twice the total available power of today by 2030, and about 200 times the total available power of today by 2050. It will be impossible to realize a sustainable future if digital transformation consumes so much energy as to destroy the earth's environment.

Under such a condition, only those who can improve energy efficiency 10-fold can afford to increase computer performance 10-fold, or extend smartphone use 10-fold. Compared to general purpose chips which are required to handle all tasks, specialized chips achieve orders-of-magnitude improvement in energy efficiency by eliminating unneeded circuits. That is why specialized chips are in demand. In addition, since AI processing utilizes neural networks which process data in parallel, it is difficult for von Neumann architecture designed for sequential processing to deliver adequate performance. As a result, specialized chips are being developed around the world to serve as AI accelerators. Furthermore, the slowing of Moore's Law is providing additional tailwind for specialized chips.

Unfortunately, specialized chips development requires special skills and cannot be easily undertaken by everyone. The latest chips integrate more transistors than there are people in the world. Development costs have skyrocketed in recent years to approach $100 million. It will take even a team of several hundred designers several years to develop a specialized chip, which makes it difficult to keep pace with today's rapid technological advance.

In software development, bugs can be patched after the fact. But hardware cannot be shipped unless it is completely error-free. Compared to software, hardware development is indeed hard and carries more risk.

If technologies similar to compilers used in software development are available to chip development, in other words, if silicon compilers become a reality, we can expect both hardware development cost and risk to drop. In addition, more people can become hardware designers. Eventually, as the open-source culture takes root in hardware development and the supporting ecosystem expands and develops into a multi-layer network, mass collaboration will become possible. When that happens, one will be able to develop chips like writing software.

Alan Kay once said that "People who are really serious about software should make their own hardware." Indeed, system development requires both hardware and software development.

Our goal at RaaS is to democratize access to silicon technology. We aim to create a development platform to realize agile authentic prototyping where prototypes can be created rapidly by innovating silicon compiler technology to enable designing chips like writing software.

Our technology goal is a 10-fold increase in both development efficiency and energy efficiency. We plan to improve development efficiency by creating an agile design platform and adopting an open architecture. In addition, we aim to increase energy efficiency through manufacturing chips in the most advanced CMOS process and implementation of 3D integration.

We provide semiconductors as a service, rather than sell them as a product. It is the role of RaaS to develop the necessary technologies to achieve that goal.

RaaS had planned to bring researchers from member companies together at the Mejirodai International Village campus of the University of Tokyo where they can conduct research while providing stimulation to each other. However, because of COVID-19, RaaS activities have also been limited to center around remote work.

In FY2021, RaaS applied to and was accepted by the "Project for Research and Development of Enhanced Infrastructures for Post 5G Information and Communications Systems / Development of Advanced Semiconductor Manufacturing Technology (b) Development of Advanced Semiconductor Backend Processing Technology (More than Moore)" of the New Energy and Industrial Technology Development Organization (NEDO). The development theme is "(b2) Implementation Technology for Edge Computing."

In system R&D, RaaS, together with the University of Tokyo, authored and presented multiple conference papers in FY2022 to report on its evaluation of a 7nm prototype chip. In technology R&D, based on the NEDO project

mentioned above, RaaS focused its efforts on the establishment and implementation of technology for WoW (wafer-on-wafer) and CoW (chip-on-wafer) integration using Cu-Cu low temperature bonding as part of its direct bonding 3D integration technology development (equipment and process development for WoW and CoW).

Table 2.1.1 List of FY2022 d.lab Partner Members (in Japanese phonetic order)

Aoha, Inc.
Asahi Kasei Microdevices Corporation
ADVANTEST CORPORATION
Analog Devices KK
Ushio Inc.
ORGANO CORPORATION
KIOXIA Corporation
Gigaphoton Inc
Kobe Steel, Ltd.
Kobelco Research Institute, Inc.
Samsung R&D Institute Japan
Siemens Electronic Design Automation Japan K.K.
JSR Corporation
JCU Corporation
Shin-Etsu Chemical Co., Ltd.
SCREEN Holdings Co., Ltd. (Raas)
Sumitomo Corporation
Socionext Inc.
Sony Corporation
Daikin Industries, Ltd. (RaaS)
Dai Nippon Printing Co., Ltd.
DISCO Inc.
Tokyo Electron Ltd.
TOKYO OHKA KOGYO CO., LTD.
Toyobo CO., LTD.
TORAY INDUSTRIES, INC.
Toppan Printing CO., LTD. (RaaS)
Nagase & Co., Ltd
NIKON CORPORATION
IBM Japan, Ltd.
Cadence Design Systems, Japan
Nihon Synopsys G.K.
JEOL Ltd.
NEXTY Electronics
Panasonic Industry Co., Ltd.
Panasonic Connect Co., Ltd. (RaaS)
Semiconductor Energy Laboratory Co., Ltd.
Hitachi, Ltd. (RaaS)
Fujitsu Ltd.
FUJIFILM Corporation (RaaS)
Micron Memory Japan, G.K.
Mitsui Chemicals
Mitsubishi Chemical Corporation
Mitsubishi Electric Corporation
MIRISE Technologies Corporation (RaaS)
Murata Manufacturing Co., Ltd.
Renesas Electronics Corporation
Resonac Corporation
ROHM Co., Ltd.

Table 2.1.2 List of FY2022 d.lab Partnership Program Seminars

Date	Title	Presenter(s)
5/25/2022	Special Presentations by Young Researcher Winners of MIT Technology Review Innovators Under 35 Award and FY2022 Kickoff	Takahiro Mizoguchi, CEO, Motion Lib Takuya Sasatani, Project Assistant Professor, Graduate School of Engineering, University of Tokyo Atsutake Kosuge, Lecturer, d.lab Tadahiro Kuroda, Professor, d.lab
6/22/2022	IBM Day	Daiju Nakano, IBM Norie Iwasaki, IBM Shintaro Yamamichi, IBM
7/20/2022	ECTC 2022 Report	Kai Takeuchi, Project Researcher, d.lab Masaya Kawano, Project Researcher, d.lab Masaaki Niwa, Senior Fellow, d.lab Takeshi Takagi, Principal Researcher, d.lab
8/25/2022	2022 VLSI Symposium Report	Mototsugu Hamada, Project Professor, d.lab Atsutake Kosuge, Lecturer, d.lab Toshiro Hiramoto, Professor, d.lab Shinichi Takagi, Professor, d.lab Masaharu Kobayashi, Associate Professor, d.lab Masaaki Niwa, Senior Fellow, d.lab
10/26/2022	d.lab Partners Technology Exchange	Kazutoshi Wakabayashi, Senior Fellow, d.lab ADVANTEST CORPORATION Kobe Steel, Ltd. Kobelco Research Institute, Inc. JCU Corporation Showa Denko Materials Co., Ltd. Dai Nippon Printing Co., Ltd. DISCO Inc. Toyobo CO., LTD. Toray Industries, Inc. NIKON CORPORATION Cadence Design Systems, Japan Mitsubishi Chemical Corporation Renesas Electronics Corporation
11/29/2022	TSMC 3DIC Center Tour and Onsite Technology Exchange	Tadahiro Kuroda, Professor, d.lab
12/13/2022	imec Day	Naoto Horiguchi, imec Eric Beyne, imec
1/18/2023	IEDM2022 Report	Toshiro Hiramoto, Professor, d.lab Shinichi Takagi, Professor, d.lab Masaharu Kobayashi, Associate Professor, d.lab Ken Takeuchi, Professor, d.lab Takeshi Takagi, Principal Researcher, d.lab
2/8/2023	d.lab Materials Seminar	Masahiro Nomura, Professor, Institute of Industrial Science, University of Tokyo Hidenori Abe, Senior Director, Resonac Kazunori Yamamoto, Project Researcher, d.lab
3/15/2023	ISSCC2023 Report	Makoto Ikeda, Professor, d.lab Atsutake Kosuge, Lecturer, d.lab Mototsugu Hamada, Project Professor, d.lab Tetsuya Iizuka, Associate Professor, d.lab Ken Takeuchi, Professor, d.lab

2.2 Advanced Device Research Division

Advanced Device Research Division is working for the development of three-dimensional (3D) integration technology and advanced device technology aiming at ten times higher energy efficiency of semiconductor systems in the data-driven systems.

In computing technologies such as AI, which require large amounts of data processing, energy consumption associated with large and frequent data transfers between memory and processors has become a major issue. As a technology to solve such problems, we are focusing on direct bonding 3D stacking technology that forms direct bonds at the chip level or wafer level, shortens the distance of data movement, and improves energy efficiency.

In the NEDO project "Post 5G information communication system infrastructure strengthening research and development project / development of advanced semiconductor manufacturing technology (subsidy)" adopted in 2021, The Research Association for Advanced Systems (RaaS), a technology research association on 3D integration technology operated by d.lab as the headquarters, is working with member companies of RaaS on the theme of "Development of direct bonding 3D lamination technology (equipment and process development for WoW and CoW)". This project aims to develop and implement key point technology related to WoW (Wafer on Wafer) bonding technology and CoW (Chip on Wafer) bonding technology by low-temperature hybrid bonding of Cu-Cu.

This year is the second year of the project, and we are focusing on introducing and starting-up of major equipment and developing elemental technologies. The project is off to a good start and is progressing largely according to plan. We are accelerating research and development to achieve the target value of the intermediate gate scheduled for December 2023.

2.3 Platform Design Research Division (VDEC Function) FY 2022 Report and FY 2023 plan

2.3.1 Overview of Platform Design Research Division

Since its establishment in 1996, the VLSI Design and Education Center (VDEC) at the University of Tokyo has been developing projects that contribute to integrated circuit design education at universities and technical colleges in Japan, based on the three major roles: ”spreading the latest information on VLSI design and education,” ”providing licenses of CAD tools,” and ”supporting on VLSI chip fabrications for academic use.” On October 1, 2019, VDEC has been re-organized into Systems Design Lab (d.lab), Graduate School of Engineering, the University of Tokyo as part of an organizational restructuring aimed at strengthening integrated circuit related activities in the University of Tokyo’s semiconductor integrated circuit-related activities. The Platform Design Research Division of d.lab continues to carry out the functions of the VDEC and continues “VDEC activities” seamlessly. Here, the outline of “VDEC activities” of the FY2022 is reported below.

The missions of VDEC are for advancement of researches and education on LSI design in public and private universities and colleges in Japan and send many distinguished VLSI designers into industry. After 27 years of VDEC establishment, educations on CAD software, LSI design and design flow in universities have been well established. On the other hand, advancement on nano-meter CMOS technologies forces design flow and CAD software complicated. We have been continuing CAD tool seminar by the lecturers from EDA vendors for twice a year. We hold the seminar in VDEC and provide distance learning through video streaming. We expect spread of the up-to-date LSI design methodology by using CAD tools.

In order to make it more convenient for the participants, the seminars have been held only in Tokyo since 2009, and at the same time, the seminars have been broadcasted to individual participating lab. The VDEC expects that the latest CAD use-case will be shared among labs through the seminar organized by VDEC, and will be a trigger to spread the technology nationwide. In FY2022, all seminars will be conducted online. Some items were conducted in the form of on-demand plus live Q&A sessions to improve the convenience of participation. In addition, in view of the current situation where the tool-chains of various companies are becoming more complex and it is difficult to fully use the introduced tools, lectures on the tool-chains recommended by each tool vendor were also held in conjunction with the individual tool seminars. From the end of FY2019, we received permission from each EDA vendor to use EDA tools from home, to avoid delay&slowdown in integrated circuit design research and education in Japan.

2.3.2 Status of Education at Platform Design Research Division

The LSI Design Flow Seminar is designed to educate the basic concepts of LSI design and to provide hands-on experience of practical design examples using multiple CAD tools. For this purpose, VDEC has been organizing LSI design education seminars as well as “Refresh Seminar” for re-education programs for engineers. In FY2022, we have canceled “Refresh Seminar.”

In addition to these seminars, VDEC holds the “VDEC Designers’ Forum” once a year, mainly for young faculty members and students. This is a workshop-style meeting, where participants bring their design cases and exchange their successes and failures, in addition to invited lectures from companies and universities. In FY2022, the VDEC Designer Forum had been held in hybrid format at Yupopo Akita Art Village. Since FY2011, the “IEEE SSCS Japan Chapter VDEC Design Award” has been presented as an award for VDEC activities. The final judging and awarding of the “IEEE SSCS Japan Chapter VDEC Design Award” has been held at VDEC Designers’ Forum since 2011, and in 2022, the IEEE SSCS Japan Chapter VDEC Design Award will be presented to Mr. T. Shimada of University of Tokyo. Four VDEC Design Award Excellence Awards, (Mr. T. Shimada(University of Tokyo), Mr. FU XI(Tokyo Institute of Technology), Mr. L. Zheng(Tokyo Institute of Technology), and Mr. R. Okada(Nara Institute of Science and Technology)), and three VDEC Design Award Encouragement Prizes (Mr. Y. Watanabe (Tohoku University), Mr. M. Osada (University of Tokyo), and Mr. S. Yamaguchi(Kyoto University)), and one

VDEC Design Award Commendation Prizes for Idea Contest (Mr. K. Mii(Osaka University)).

Although the educational system through such seminars and forums has enabled students to learn the basics of LSI design, they still face various difficulties in actual LSI design situations. For beginners, setting up the CAD software is the biggest problem. Even after setting up the software, they are often baffled by the "difficult error messages" issued by the CAD software. VDEC users can register for the "CAD mail group" and the "Prototyping Technology User Group" on the VDEC website, where they can post their questions and ask for help. The registered users of the mail groups are not obligated to respond, but in most cases they can get help from experienced users within a few hours or days. We hope that you will take advantage of this system to help solve your problems.

2.3.3 Publications related to Platform Design Research Division

Figure 2.3.1 shows the use of the VDEC facility in the published literature related to VDEC. It can be confirmed that CAD software is widely used in writing papers. Since CAD software is often used not only in chip design but also in the preparation stage of chip prototyping, its contribution as a tool to demonstrate the basic idea of the research is also significant.

2.3.4 Report on AI Chip Design Center

VDEC and the AIST have been jointly commissioned by NEDO to develop a common platform technology for accelerating AI chip development under the "Innovation Promotion Project for Accelerating AI Chip Development / R&D Item 2: Development of Common Platform Technology for Accelerating AI Chip Development" since 2018. In this project, we have established an EDA utilization and design environment for venture companies and small and medium-sized enterprises(SMEs) in Japan, and are working as an "AI chip design center(AIDC)". In this activity, in addition to the introduction of EDA tool licenses that allow venture companies and small and medium-sized companies to prototype up to engineering samples, we have introduced IP for 40nm, 28nm, and 12nm, and are also providing a large-scale, high-speed design and verification environment using a hardware emulator, which was introduced with a subsidy from the Ministry of Economy, Trade and Industry at the start of this project. In FY2020, we have designed a SoC platform with NoC, PCIe, DDR4, etc., and multiple functional IP cores, and taped out the platform as a SoC with multiple AI IP cores designed by multiple users, and after almost 1-year delay, we have received assembled chip in the beginning of Jan. 2022, and after one week we could evaluate most of SoC functionalities and by the end of March 2022, almost all of IPs got fully verified. We have also designed and taped out with 4 AI IP cores in 12nm in June 2022, and all the IP cores have been successfully demonstrated by the end of March 2023. In order to further strengthen this activi-

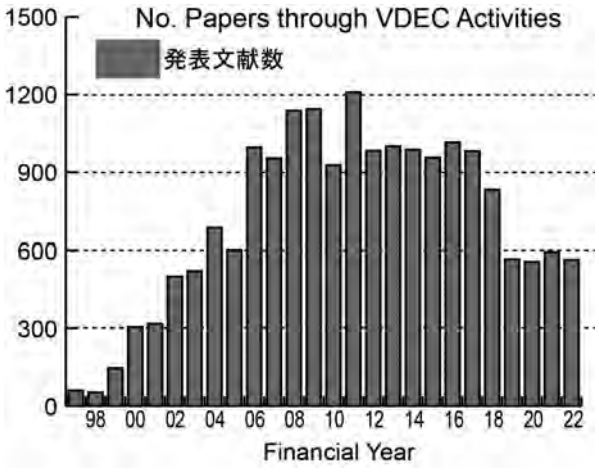

Fig. 2.3.1 Trends of number of papers through VDEC activities.

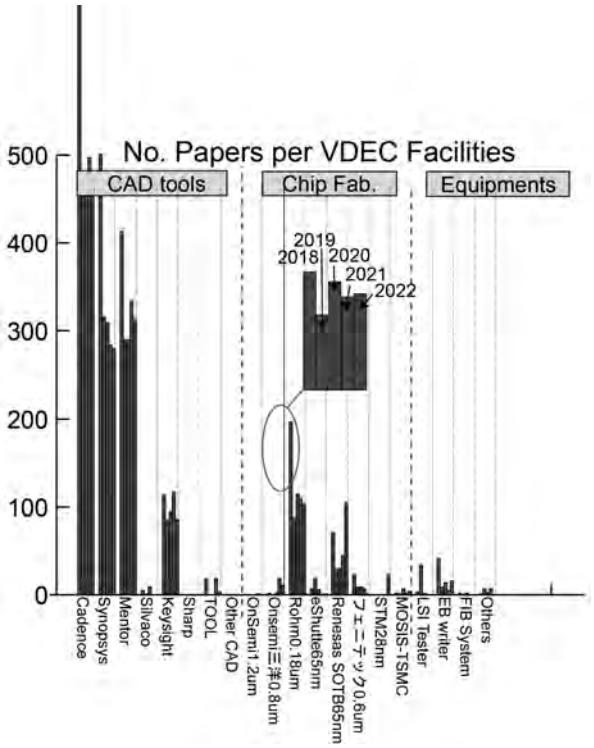

Fig. 2.3.2 Number of papers related to VDEC facilities.

ty, we are accelerating our research by establishing the "AIST-The University of Tokyo AI Chip Design Open Innovation Laboratory" (AIDL) in the Takeda Building, Asano Campus, The University of Tokyo on September 1, 2019.

2.3.5 Plan for FY 2023 "VDEC Activities" of Platform Design Research Division

In FY2023, we will continue the VDEC Activities for academics as before.

【Design related information dispatching/Seminar】

We will continue holding the following seminars: (1) CAD tools seminars which have been continued since 1997, (2) "Refresh seminar" since 1998, (3) "Designer' Forum" since 1997. We will also continue seminars for LSI tester usage at VDEC and sub-centers, workshops on LSI testing technologies initiated by D2T.

【CAD tool support】

We will continue Cadence tools, Synopsys tools and Mentor tools as the main stream design tools. We will continue analog ADS/EMPro/GoldenGate by Agilent, C-based design environment, BachC by Sharp. In addition, we continue trial of several CAD tools, such as layout platform, Lavis by TOOL. Design debugging platform from SpringSoft has merged into Cadence tools and will be continued.

【Chip fabrication services】

We will continue chip fabrication services for 0.18μm CMOS by Rohm, 0.8μm CMOS by On-semiconductor-Sanyo, and IHP SiGeBiCMOS 0.18um as the regular services.

In addition to the above. We will continue to develop an "AIDC" activities, in collaboration with AIST. We will introduce a logic emulator for large-scale AI digital chip design verification, and maintain and operate EDA licenses for industrial applications. The main objective of this project is to provide small and medium-sized venture companies with a development environment for AI chip design, evaluation, and verification in order to accelerate the development of AI chips, but we also plan to improve the environment for use by universities in order to promote university-originated companies in the field of AI-related integrated circuits.

Table 2.3.1 Chip fabrication schedule

【CMOS 1.2μm 2P2M】On-Semiconductor(Former Motorola Japan)

	Chip application deadline	Design deadline	Chip delivery
2023#1	2023/7/3	2023/9/25	2023/12/18
2023#2	2023/1/9	2023/3/25	2023/6/24

【CMOS 0.18μm 1P5M(+MiM)】Rohm

	Chip application deadline	Design deadline	Chip delivery
2023 #1	2023/4/3	2023/6/26	2023/10/13
2023 #2	2023/6/12	2023/9/4	2023/12/16
2023 #3	2023/7/31	2023/10/23	2024/2/9
2023 #4	2023/12/4	2024/2/26	2024/6/7

2.4 Platform Device Research Division

2.4.1 Mission

D.lab platform device research division aims at providing every researcher with three essential elements for research on new devices. The division is with around 30 staffs, powered by Professor Yoshio Mita, the playing division director who himself actively performs experiments in the Cleanroom as a leading researcher, and operated in collaboration with related departments (such as Institute of Engineering Innovation, Electrical Engineering and Information Systems, and Mechanical Engineering) in terms of human and budget resources. Especially in the year 2022, two new institutes was born on the basis of our world-class activity. The objective is to visualize research-oriented activities. To do that, a new center "Nanosystem Integration Center" was established on 1st April 2022, in order to assemble cutting-edge researchers of the Faculty of Engineering. Professor Mita is leading the device research and development division, and aims at raising research activities including international cooperations. The second is endowed division for "Nanosystem Integration Technology Innovation". The purpose is "accumulation", "maturation", and "generation" of technologies to open new research domains, by taking Takeda SCR as an assembling point.

Research in emerging fields of semiconductor electronics devices (such as integrated circuits), sensors and microsystems requires three essential elements: (1) fabrication machines with stupendous amount of budget, (2) rich accumulation of fabrication technology knowledges, and (3) research capability to develop new technologies required for new devices. In Japan, these three elements had been prepared and kept in an individual research group until the end of 20th century. However, due to the technology trends towards advanced fabrication over larger-scale wafers, it has become almost impossible for a research group to purchase and maintain the cutting-edge fabrication machine line, in the 21st century. Originally, it was impossible for every research group in universities, companies, research institutes, and NPOs, to exclusively "own" such large-scale facility and necessary budget by themselves; If researchers wish to "cooperate" with the other researchers in a platform, which is equally open to everybody, they can "effectively own" the most advanced "open platform", and thereby the cutting-edge research activities can be held anywhere in Japan. This is the principle of d.lab's open device platform, which is in fact a lateral expansion of "shared economy model in VLSI design and fabrication" to micro-nano fabrication and measurement research field, originally established by VDEC for Japan in 1996.

Towards that end, d.lab Platform Device Research Division takes full advantages of spaces (of its own and of open rental) in Takeda Sentanchi Building. The building was inaugurated in December 2003, thanks to the enormous donation in 2001 from Mr. Ikuo Takeda (founder of Advantest) to the faculty of engineering (Dean was Professor Hiroshi Komiyama) as well as VDEC (director was Professor Kunihiro Asada). In the building, a 600m^2

Fig.1 Development of Takeda Sentanchi Supercleanroom

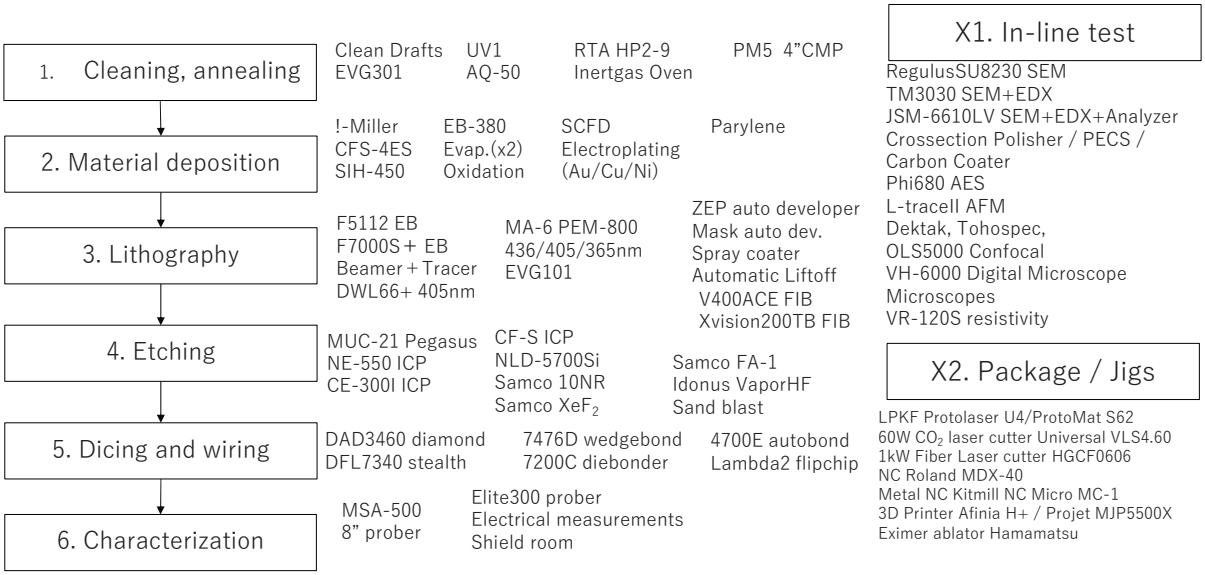

Fig.2 List of equipment under d.lab Platform Device Research Division

-square supercleanroom including "official ISO3 (a.k.a. federal class 1. Once measured as ISO1)" area (Fig.1). The cleanroom and affiliated experimental rooms are equipped with cutting-edge nanofabrication and measurement machines, total valued over 4.3 billion yens (22M euros, due to cheap JPY ratio). The users can openly use such nice machines really inexpensively.

Over 100 apparatuses are openly accessible (Fig.2), including, "world's fastest" large-area direct electron beam (EB) writing machine Advantest F5112+VD01, which has been donated according to the wise decision of Mr Ooura, a chairman of Advantest, fine EB writer Advantest F7000S-VD02 and Silicon Deep Reactive Ion Etching machine SPTS MUC-21 ASE-Pegasus, both purchased by Japanese government's supplemental budget (known as Abenomics, the first arrow), and the scanning electron microscope (SEM) Hitachi Regulus SU8230 that provides highest-class resolution among those obtainable by research laboratory. The machines can cover most of the research steps in nanotechnology, which are cleaning, film deposition, lithography, etching, packaging and characterization. Not all apparatuses are yet installed in Takeda Building, however due to nationwide platform network, researchers can access in another equivalent nanofabrication platform center(s).

2.4.2 "Takeda Sentanchi Supercleanroom" cooperation platform

The platform is called "Nanotechnology Platform UTokyo Nanofabrication site" according to the MEXT's national project, or simply "Takeda Sentanchi Cleanroom" (in short, Takeda CR). The platform is widely open to those who share the "value of cooperation". The most important understanding for every user is the platform must not be considered as a simple outsourcing agent; being understood the value of "own help, mutual help, and public help", the participant can drastically minimize costs (personnel, budget, and time), which should have otherwise been totally covered by each researcher, and can directly jump into advanced research. Key Performance Indicators of such benefits are as follows: over 8.3 billion yens for installation cost of building and equipment, over 350 million yens for yearly operating cost, and reduction of over 20 years' leading time to acquire know-hows in advanced fabrications. These benefits have attracted many research groups. Since ten years, the number of research groups who sent us the letter of consensus exceeded 550. Over 1062 members are yearly subscribed (including renewal and new subscription).

Operation principle is also "own help, public help, and mutual help". Budgetwise, each term of the principle corresponds to: (1) User's payment to participate budget acquisition (charged according to the officially-approved d.lab's internal rule), and (2) national budget allocated to d.lab platform research division, MEXT Nanotechnology Platform project, and (3) major laboratories (who rent space in Takeda Building for their research work) as well as research projects with d.lab operation laboratories (such as Mita Lab). Of course, each budget category is righteously dispensed in perfectly following its own rule de-

fined by corresponding laws and ordinances. The yearly operation cost of 350 million yens are composed of equipment installation, electricity and water fees, maintenance, and personnel. Recently electricity cost is drastically increasing. National Universities have acquired budget flexibility since the date of private agency statuses. It helps a lot to ensure staff employment as well as small to middle sized equipment acquisition.

Platform Device Research Division staffs acquire implicit information for future fabrication technologies, due to daily help to massively parallel research projects. The team develops technologies with high demand and universality and make them accessible by publishing papers.

Moreover, taking full advantage that PDRD is a division of d.lab, the team has been developed for over 10 year, a reliable research scheme for integration of LSI and MEMS devices, known as "Integrated MEMS research domain". As summarized in a peer-reviewed journal [1], through VDEC function of d.lab "LSI foundry", a specific LSI circuit silicon wafers are fabricated through company (such as Phenitec Semiconductor). Then the wafer is "post"-processed in an open nanofabrication platform including Takeda Sentanchi Supercleanroom. The critical advantage of such scheme is that researchers can "easily" obtain silicon wafers with transistor circuits, which has been really difficult for university cleanrooms to acquire reliability, and can fabricate by themselves specific MEMS that no foundry company can provide. Namely, researchers can produce "World's first functionality" with "World's highest quality". Such a flexible scheme is unique in the world. Yearly one multi-chip fabrication is performed (pre-fixed participants upon request), including collaborative research works with industries.

[2] Y. Mita *et al.*, *Japanese Journal of Applied Physics*, **56**, p. 06GA03, 2017 (2017) DOI: 10.7567/JJAP.56.06GA03

2.4.3 Activity Report 2022 of Platform Device Research Division

【Prize】The MEXT Nanotechnology Platform Project gives prizes for good usage of platform. Every year, several projects are selected by specialists' award committee, among solicited candidates selected from over 3000 research project reports. Among the projects that PDRD have solicited, we won again and again the 1st prize "Best use award" (Fig.3). Note that our division has been awarded consecutively for four years, including three last years as the best use award. No equivalent research platform exists in Japan. The awarded group are UTokyo Professor Hitoshi Tabata group as well as Gaianixx.

【No infection case & no decrease in platform uses】In the year 2022, we also continued strict but acceptable anti-pandemic protocol. This year also, zero transfection has been obtained, thereby accumulating the supporting data of validity of our countermasure.

【Post-Nanotech platform national project】The major part of "public" help for cleanroom has been covered by MEXT Nanotechnology platform. Nanotechnology platform project that finished at Reiwa 3rd (31/Mar/2022); MEXT has started another national project, by officially

Fig.3 Group photo after award ceremony

stating “use heritage of nanotech platform”, for digital transformation (DX) in materials including MEMS devices. The name of the new project is called “Advanced Research Infrastructure for Material research (ARIM) ”. Structurally speaking, material DX have adopted “research domain hub-and-spoke” system, in contrast with Nanoplat’s “technology domain system” composed of characterization, nanofabrication, and material syntheses.

d.lab PDRD has been merged with Nano Engineering Center of Institute of Engineering Innovation and Information Technology Center to form a strong hub team, under presidency of Professor Yuichi Ikuhara. The team has been highly appreciated by the evaluation committee and was granted for 10-year project’s “hub” site. Attached to the national project, MEXT continuously grants us a big supplemental budget for our proposal to enhance performance of our cleanroom. Also, d.lab was awarded by MEXT’s “Next generation X-nics research site” and machines have been installed accordingly. In total, we have identified that 4500 millions of yens is necessary to complete competitive Cleanroom; yielding 300M yens per year if we renew everything at every 15 years. The team will try his best to assemble and share “machine, technology, and people”.

2.5 Activity Report of ADVANTEST D2T Research Department

2.5.1 Introduction of ADVANTEST D2T Research Department

2.5.1.1 Aim of establishing ADVANTEST D2T Department (former D2T research division)

ADVANTEST D2T research division was established in VDEC in October 2007. As the name suggests, it is financially supported by ADVANTEST Corporation.

The aim of establishing ADVANTEST D2T research division was to promote the research and education environment with regard to VLSI testing in all universities and colleges in Japan. “D2T” signifies that we consider not only design but also testing. Through our activities, we hope to provide expertise in design and testing for the industry. In addition, we are exchanging researchers with those of other universities and research institutes both in Japan and overseas. Moreover, D2T research division is suitable for collaborations with the industry because VLSI testing is one of the most practical research topics in the industry. On the basis of these activities, our final goal is to become a center of excellence of VLSI testing in Japan.

D2T research division has spent a total of 12 years to develop the first (Oct. 2007 – Sep. 2010), second (Oct. 2010 – Sep. 2013), third (Oct. 2013 – Sep. 2016), and fourth (Oct. 2016 – Sep. 2019) phases. D2T activity report of 2022 presents the last financial year, i.e., Oct. 2021 – Sep. 2022, of the fifth phase. Systems Design Center, School of Engineering, the University of Tokyo has been established in Oct. 2019, and Advantest D2T research department is within the center. D2T research department primarily focuses on D2T research activities and education. The sixth project phase (Oct. 2022 onwards) of D2T project was commenced by courtesy of ADVANTEST Corporation. The details pertaining to the activities of our group are presented in the following sections.

2.5.1.2 Members of ADVANTEST D2T Division

Project Professor	Makoto Ikeda
Postdoctoral research fellow	Zolboo Byambadorj
Project Lecturer	Akio Higo
Researcher	Koji Asami (Advantest Laboratories Ltd.)
Researcher	Masahiro Ishida (Advantest Corporation)
Researcher	Takahiro Yamaguchi
Assistant Clerk	Makiko Okazaki

2.5.2 Report of the 17th D2T Symposium

The 17th D2T Symposium was held on September 15, 2022, hybrid. This year, we will invite lecturers overseas, Assistant Professor, Zhongrui Wang from Hong Kong University, Reika Ichihara from Institute of Memory Technology R&D, Kioxia Corporation, Associate Professor Shintaro Hisatake from Gifu University, Takahiro Nakamura, Ph.D. from AIO Core Co., Ltd., Dr. Motoaki Hara, Senior researcher from National Institute of Information and Communications Technology (NICT), Associate Professor Katsuhiro Tomioka from Hokkaido University, for their distinguished research topics.

We sincerely appreciate each participant for their contributions to the symposium. We look forward to greater participation again at the 18th D2T symposium on Sep. 8 Fri. 2023.

17th D2T Symposium Program ONLINE　September 15, 2022

10:00	**Opening Remarks** **Makoto Ikeda** (d.lab, School of Engineering, the University of Tokyo) **Yoshiaki Yoshida** (President & CEO, ADVANTEST CORPORATION)
10:10	**Session 1** (Chairperson: Tetsuya Iizuka, d.lab, the University of Tokyo) *Measurements in millimeter-wave and THz wave band based on photonics* **Shintaro Hisatake,** Associate Professor (Gifu University) *High-density integrated optical transceiver based on silicon photonics technology"* **Takahiro Nakamura,** Ph.D. (AIO Core Co., Ltd.)
11:40	**Lunch**
13:10	**Session 2** (Chairperson: Atsutake Kosuge, d.lab, the University of Tokyo) *Reliability study of ferroelectric HfO2 memory using advanced analytical techniques* **Reika Ichihara** (Institute of Memory Technology R&D, Kioxia Corporation) *Memristor-based echo state networks* **Zhongrui Wang,** Assistant Professor (Department of Electrical and Electronic Engineering at the University of Hong Kong) **15min break**
14:40	**Session 3** (Chairperson: Yoshio Mita, d.lab, the University of Tokyo)
14:55	*Vertical III-V Nanowire Transistors and Prospects* **Katsuhiro Tomioka,** Associate Professor (Hokkaido University) *CLIFS: Chip Level Integrated Frequency Standard, How do we approach the cliff of CLIFS?* **Motoaki Hara,** Senior Researcher (National Institute of Information and Communications Technology (NICT)) **Session 4** *Recent D2T research department progress*
16:15	**Akio Higo**, Lecturer (d.lab, the University of Tokyo)
16:30	**Closing Remarks** **Tadahiro Kuroda** (Director, d.lab, School of Engineering, the University of Tokyo)

2.5.3 Research Activity Reports of the ADVANTEST D2T Research Department

High-Resolution Analog-to-Digital Converter Based on Stochastic Comparators

Takahiro J. Yamaguchi, Akio Higo, Tetsuya Iizuka, Makoto Ikeda

This project aimed to explore new stochastic analog-to-digital converter (ADC) architectures. To reduce randomness and increase accuracy, an approach for robustly detecting level-crossing time via stochastic median is investigated.

The validity and appropriateness of the root mean square error as a performance measure was verified. Our proposed theory which was developed for "comparators with random fluctuations caused by process variations" was verified by Monte Carlo experiments.

5G multi-channel/millimeter-wave signal measurement

Koji Asami, Zolboo Byambadorj, Ryogo Koike, Sheng Guo, Nguyen Ngoc Mai-Khanh, Akio Higo, Tetsuya Iizuka, Masahiro Fujita, Takashi Matsumoto, Makoto Ikeda

We study and develop fundamental research to measure the millimeter-wave signals in an over-the-air (OTA) environment. A 4-channel planar antenna array has been developed for the near-field measurements of the millimeter-wave antenna. Metasurface was fabricated to reduce the coupling between antennas. Antenna probes were fabricated, and experiments are underway to confirm the characteristics and measure the antennas. In addition, to confirm the measurement algorithm, a commercially available horn antenna was used as a probe to measure antennas for 5G. We confirmed that the far field could be estimated accurately by correcting the influence of the probe from the measured near field.

High-Speed and High-Accuracy Multi-Pin Timing CAL for ATE

Masahiro Ishida, Hidaka Otsuka, Tetsuya Iizuka, Zule Xe, Akio Higo, Masahiro Fujita, Makoto Ikeda

Automatic test equipment (ATE) for Semiconductors has thousands to tens of thousands of signal input and output channels. It requires timing calibration (CAL) to correspond the test signal output's timing to the device under the test (DUT) and the comparison timing of the signals output from the DUT. This research focuses on a high-speed and high-accuracy multi-pin timing CAL method applicable to ATE. This year, we evaluated a prototype TEG circuit fabricated in TSMC 65nm CMOS process last year. We confirmed that the difference in characteristics between the reference timing generator circuits for comparator CAL and the difference between the timing measurement circuits for driver CAL does not change significantly depending on the operating environment (temperature and supply voltage). We found that the target accuracy of the timing CAL was able to be at one ps. The research theme on High-Speed and High-accuracy Multi-Pin Timing CAL for ATE was completed by summarizing issues such as crosstalk, signal extraction, and CAL for CAL circuits when circuits for the timing CAL of many channels are implemented on one chip.

2.5.4 Publication

Journal

[1] Zolboo Byambadorj, Koji Asami, Takahiro J. Yamaguchi, Akio Higo, Masahiro Fujita and Tetsuya Iizuka, "High-Precision Sub-Nyquist Sampling System Based on Modulated Wideband Converter for Communication Device Testing," IEEE Transactions on Circuits and Systems-I: Regular Papers, vol. 69, no. 1, pp. 378 - 388, Jan. 2022

Kuroda and Kosuge Lab
(http://www.kuroda.t.u-tokyo.ac.jp/index.html)

TCI: ThruChip Interface

T. Kuroda, M. Hamada, A. Kosuge, T. Shidei, M. Okada, Wai-Yeung Yip, K. Shiba, T. Omori

TCI is a 3D integration technology that employs inductive coupling between coils created with on chip metal line patterns for data communication across stacked chips. It realizes the same or better performance as TSV (Through Silicon Via) but at a lower cost. This year, we presented research papers on TCI-based 3D SRAM stacking technologies including (a) circuit technology for low-power computation, (b) area efficient coil-design, and (c) computing architecture and AI processing algorithms to use 3D stacked SRAMs efficiently. We presented our achievements at HotChips'22, A-SSCC'22.

TLC: Transmission Line Coupler

T. Kuroda, M. Hamada, A. Kosuge, Y. Hayashi, Ximing Wang

TLC is a data communication technique between circuit boards by utilizing electromagnetic coupling between transmission lines on them. It solves the issues in conventional connectors such as wearing, reliability against vibration, and impedance mismatch, realizing wireless connectors. This year, through joint research with a company, we conducted research and development of compact and high-density TLC mounting technology for connecting packaged boards and PCBs, and research on fully sealed non-contact connector technology for simultaneous communication of non-contact power supply and TLC in close proximity to each other. GND shielding technology is studied to prevent mutual interference between wireless power transmission and contactless communication. We presented our achievements at ICECES'22.

RFID Tag Chip Design

T. Kuroda, M. Hamada, A. Kosuge, R. Miura, S. Shibata

We are developing a wireless tag that integrates an antenna and wireless circuits on a tiny chip less than 1 mm square and combine it with an intelligent reader to pursue an extremely low-cost IoE (Internet of Everything) system. This year, we developed a new collision avoidance function that deterministically avoids collisions based on received signals by utilizing adiabatic circuits. We developed a low-power RFID tag circuit using TSMC 0.18m CMOS process by using our proposed the adiabatic logic circuit. We have also developed a new bonding-less mounting technology in which the coil mounted on the RFID tag is coupled to the coil on the PCB. A test chip was developed and evaluated using TSMC 0.18um CMOS process, and papers were presented at SSC-L'22.

Wired-logic AI Processor

T. Kuroda, M. Hamada, A. Kosuge, K. Shiba, Yao-Chung Hsu, R. Sumikawa, F. Hondo, Zhan Zhijie

We are studying non-von Neumann AI processors focusing on wired-logic to reduce power consumption. The area efficiency is a bottleneck of the wired-logic processor and it is significantly degraded due to the need to implement a huge number of elements on a chip. Therefore, we have developed two new technologies: (1) a technology to optimize the network by removing unnecessary neurons and synapses, called pruning in the human brain, and (2) a nonlinear neural network technology that incorporates the property of human neurons to use a wide variety of nonlinear functions in the right places to increase the representation capability of the network in order to prune more drastically than before and save the number of elements. In addition, we are developing convolutional wired-logic architecture circuits that reuse circuits in accordance with the processing of convolutional algorithms. The FPGA implementation was accepted to HotChips'22. In addition, SRAM-based in-memory computing techniques are researched. The achievements are accepted to NEWCAS, TCAS-1, ASSCC and SSC-L.

mmWave Imaging Radar based Object Recognition

T. Kuroda, M. Hamada, A. Kosuge, Wai-Yeung Yip

In harsh environments (bad weather, night, dirt on cameras), conventional human/object detectors utilizing conventional cameras have low accuracy. Since millimeter wave radar technology has high environmental resistance, the radar is promising solution for the harsh environment. However, unlike image recognition, it has a problem in detection algorithm due to low-resolution blur data. In this research, we are developing a new deep learning AI technology that handles millimeter wave images based on a new semi-automatic training data generation technology and develop a highly accurate AI technology for human/object identification. This year, we mainly studied the characteristics of millimeter-wave radar data and the network structure that matches them and developed a camera-radar cooperative semi-automatic learning data generation technique and developed a millimeter-wave radar AI system that can detect the type and location of six types of objects with the same accuracy as image recognition. The paper is accepted to IEEE Trans. Instrumentation and Measurement.

Takeuchi Laboratory

(https://co-design.t.u-tokyo.ac.jp/)

Computation in memory (CiM)

Ken Takeuchi and Chihiro Matsui

We have developed a comprehensive Computation-in-Memory (CiM) simulation platform. The simulation platform has capability to emulate multi-level cell (MLC) and various memory device non-idealities such as uniform/non-uniform conductance variation and shift. The simulation results address that the conductance shift has much more critical impact than conductance variation on inference accuracy in CiM.

Simulated Annealing

Ken Takeuchi, Chihiro Matsui and Naoko Misawa

Memory error tolerant ReRAM-based Computation-in-Memory (CiM) to solve the knapsack problem, one of the combinatorial optimization problems, is proposed. Proposed log-encoding simulated annealing (SA) on ReRAM CiM reduces the array area of ReRAM CiM by 97.6%. To co-design ReRAM device and SA, error injection is applied. As a result, the asymmetric ReRAM error increases the acceptable bit-error rate (BER) by 10 times and the acceptable bit precision to 5-bit.

In-sensor Computing

Ken Takeuchi and Chihiro Matsui

We have proposes an integration of event-based vision sensor (EVS) and processor (e.g., computation-in-memory, CiM) for low-power processing. By using newly defined characterization method of frame and EVS camera, an event-driven SRAM CiM with partitioned word-line (WL) activation method is proposed for 3D-integration of EVS. The multiple-bit synaptic weights are stored in a set of SRAMs. The proposed CiM for EVS achieves 10^{-6} times energy efficiency compared with CiM for frame camera.

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IoT Network Security

Hiroshi Nakamura

Zigbee is a short-range wireless communication protocol and needs low power and low bandwidth at the sacrifice of its short transfer range and slow speed. Due to this nature, it is widely used in small inexpensive sensors and IoTs that run on batteries, As Zigbee adopts indirect communication to achieve low power consumption, it incurs a vulnerability to LDoS attacks. To address this problem, we proposed a method to prevent LDoS attacks and identify attackers while satisfying the limitations of IoT devices, which require fewer resources for processing and consume less power. In addition, we studied a hardware mechanism to realize this method and clarified its effectiveness.

Coarse-Grain Reconfigurable Architecture

Takuya Kojima, Hiroshi Nakamura

Coarse-grained reconfigurable architectures (CGRAs) are expected as a promising architecture for wide variety of computing including embedded systems and high-performance computing due to its benefit of high-energy efficiency and programmability. CGRA consists of an array of numerous processing element and its efficiency heavily depends on the quality of compiler which maps applications onto these PEs. So far, we have proposed a novel algorithm called GenMap (A Genetic Algorithmic Approach for Optimizing Spatial Mapping), which is a mappaing framework based on a genetic algorithm. We have extended GenMap to deal with not only spatial but also temporal reconfiguration and confirmed its effectiveness. We have also shown that by incorporating approximate calculations, CGRA can achieve the required accuracy while saving area and power.

Lightweight Runtime Environment of ROS2 nodes for Embedded Devices

Hideki Takase, Hiroshi Nakamura

The Robot Operating System (ROS) and ROS2, the latest version of ROS, have attracted attention as a design platform for distributed robot software development. One of the drawbacks of ROS2 is that it is necessary to employ high-performance and power-hunger devices since it requires a Linux environment for operation. This drawback prevents ROS2 from being applied to embedded devices because they must be quick in response and consumes less power. Thus, we have proposed a novel solution called mROS2, which is a lightweight runtime environment of ROS2 nodes. One of the advantages of mROS2 is that it provides efficient communication mechanisms with less memory consumption. Currently, we are designing software architecture for this communication flow. This work is expected to contribute to the power saving and real-time performance enhancement of mobile robot systems.

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Design optimization of high-performance cryptography

M. Ikeda, A. Opasatian, K. Masada, M. Fukuda, and Y. Takeshima

Pairing-based cryptography (PBC) is one of the most important fundamentals for many novel encryption schemes. PBC normally involves extensive computations, so the high-performance cryptographic accelerator would greatly benefit many applications. To meet those needs, we have designed high-performance pairing accelerators targeting different curves (asymmetric pairing: BLS12-381, BLS24-315, BLS24-317, and BLS24-509/symmetric pairing: SS1024) and explore its use case in different applications such as the Identity-based Encryption (IBE), the Searchable Symmetric Encryption (SSE), and the Attribute-based Encryption (ABE). The design is also extended for the hash-to-point accelerator as well. The automatic schedule creation process is introduced to shorten the design time, and the optimization of the modular multiplier module is also investigated.

Implementation of fully homomorphic encryption

M. Ikeda, T. Shimada, and Y. Zhao

Fully homomorphic encryption (FHE) is a way to delegate the processing of your data, without giving a way access to it. It can calculate ciphertexts without secret key. Although FHE is expected to be used in secure delegating computation, it is far from application due to the low speed of FHE. The goal of this research is to speed up the FHE schemes like TFHE and BGV by hardware implementation. The implementation on FPGA is 4 times faster than CPU this year. Further improvement still remains in the next year. Beside hardware implementation, we also pay attention to the optimization of FHE algorithm. After tons of trade-off, we increase the number of input ports of homomorphic logic gates from 3 to 10. We also optimize the parameter of FHE to maintain the running time, decryption failure rate and security level.

Implementation of Post-Quantum Cryptography

M. Ikeda, HQ. Bui, T. Shimada, and K. Kotani

Post-quantum cryptography (PQC) is public-key cryptography and digital signatures (DS) performed by a conventional computer resistant to classical and quantum computer attacks. It aims to replace modern-day cryptography standards such as Diffie-Hellman, RSA, and elliptic curve cryptography (ECC) which all can be cracked in polynomial time with a sufficient quantum computer.

PQC algorithms that will be standardized include CRYSTALS-Kyber (lattice-based PKE/KEM), CRYSTALS-Dilithium (lattice-based DS), FALCON (lattice-based DS), and SPHINCS+ (hash-based DS). Potential algorithms to be standardized (as of 4th round of PQC standardization process) include BIKE (code-based PKE/KEM), Classic McEliece (code-based PKE/KEM), HQC (code-based PKE/KEM), and SIKE (isogeny-based PKE/KEM).

Note that NIST is planning to standardize additional DSs with the first set of proposals submitted by 2023, Jun. 1.

In this study, we have implemented CRYSTALS-Kyber in 65nm ASIC, and SIKE and its basic operations by FPGA.

Security Measures of Crypto-engine

M. Ikeda, K. Abe, and S. Kikuoka

Cryptographic implementations must be resistant to side-channel attacks and their resistance assessments are required. The resistance against side-channel attacks of a 256-bit ECDSA hardware was evaluated by performing template attacks on scalar multiplication using measured current consumption waveforms, and then the performance and the leakage success rate of implementations with some countermeasures that are considered to be effective are evaluated based on the results of logic synthesis and logic simulations. This enabled an evaluation of the effectiveness of each countermeasure and a quantitative leakage evaluation at the design stage. For hardware implementations of elliptic curve pairings, it is important to select the optimal curve that achieves both sufficient security and low cost. We suggested method to estimate the security against solving DLP (discrete logarithm problem) and ECDLP(elliptic curve discrete logarithm problem) and hardware costs such as area, cycles, and latency of paring-based cryptography, using only characteristic as variables, and applied the method to BN, BLS12 and BLS24 curves.

Neural Networks and its Security

M. Ikeda, Z. Wang, Y. Miao, B. Amartuvshin

Spiking neural networks (SNNs), due to their potential energy efficiency, are promising candidates for next-generation neural networks and are also expected to be able to integrate with neuromorphic sensors for efficient information processing. However, currently hardware implementations of SNN face significant difficulties mainly due to the additional membrane potentials introduced by spiking neuron. To this end, we propose a lossless compression method for membrane potentials, which allows, for the first time, the use of a reduced-precision fixed-point format representation for membrane potentials in deep SNNs, thus achieving the lowest resource footprint and energy consumption of any FPGA-based SNN accelerators.

On the other hand, cloud computing has become a popular field in neural network due to its complex calculations. However, the data privacy remains a significant concern in widely applying cloud computing. Fully homomorphic encryption (FHE) is a promising method for privacy protection, but it suffers from the slow speed. To address this, we focused on improving the speed of FHE-based neural network calculations in both software and hardware field. Firstly, we designed a fast algorithm for the inference in FHE-based recurrent neural network (RNN), which avoids the most time-consuming bootstrapping procedure and significantly improves the throughput. Moreover, hardware designed for a fully residue numeral system (RNS) based FHE scheme can further accelerate the calculations. Compared to other hardware design, the hardware resource is highly reduced by avoiding the complicated big number calculation.

Security on Logic Circuits and Processors

M. Ikeda, Z. Ye, J. Xin, T. Matsumoto, F. Arakawa, and T. Kikkawa

Logical locking is a technique used in hardware security to protect digital circuits from unauthorized access and reverse engineering, tampering and counterfeiting. Adding key-dependent elements to the circuit or modifying the circuit's structure in a key-dependent manner achieves this technology. The previously proposed logical locking techniques have had drawbacks, such as high overhead or security flaws. To address these drawbacks, chaotic structures controlled by attractors with a small area consumption have been inserted into the circuit in this study. By adjusting the number of chaotic structures, a balance between security and overhead can be achieved.

We also study integrating a post-quantum crypto-accelerator to RISC-V open-source instruction set architecture, to improve the public-key encryption performance on open-source hardware.

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Phase-Locked Loop Circuit Techniques for Low Phase Noise

Tetsuya Iizuka, Zunsong Yang, Masaru Osada, Ryoga Iwashita

Ring voltage-controlled oscillator (VCO) is attractive for a compact footprint, multiple phases, and no magnetic coupling. However, for the low-jitter PLL higher than 5 GHz, most previous works still resort to LC VCOs where the inductors suffer from a large area and underlying magnetic coupling. We proposed an inductorless cascaded PLL with ultralow jitter that leverages the large performance gap between low- and high-frequency ring oscillators. A single-stage sample-and-hold subsampling phase detector is proposed for the 1st stage, where the oscillator's control voltage is updated only when the impulse sensitivity function is zero, enabling wider loop bandwidth, lower jitter, and lower spur. Fabricated in 65-nm CMOS, the prototype operating at 10GHz achieves –63-dBc reference spur, 175-fs integrated RMS jitter, and –240-dB FOM with a 125-MHz reference clock.

Low-jitter and low-spur PLLs are highly demanded by the emerging high-speed communication systems. Recently, sampling/sub-sampling PLLs with high phase detection gain have shown their capability to simultaneously lower spur, jitter, and power consumption, resulting in a low spur < –65dBc and an excellent jitter-power Figure-of-Merit (FoM) < –258dB. However, to achieve sub-100-fs RMS jitter, they typically require a huge reference buffer to provide a high-slew-rate clock with low PN, penalizing PLL's power efficiency. We proposed a reference-sampling PLL with low-ripple double-sampling phase detector to lower the PD's in-band phase noise (PN) by 3dB without raising PLL's input load and crystal oscillator's power consumption. With a 100-MHz input reference, the prototype in 65-nm CMOS achieves an RMS jitter of 63fs with a spur level of –80dBc. The total power consumption is 3.1mW at 3.4GHz.

Harmonic-Mixer (HM) -Based fractional-N PLLs are excellent solutions to achieve low noise fractional operation without relying on noise cancelling circuits that require heavy calibration. The HM is usually realized by taking advantage of the frequency translation of a Sample-and-Hold (S/H) circuit. Accordingly, properly designed filters must be placed before and after the S/H to filter out unwanted spurs at the PLL output. However, the detailed mechanism for the tone generation and the requirements for the filters were not made clear in the previous works, and their designs were done in an unclear and/or ad-hoc manner. Therefore, in this work, we provided 1) a qualitative explanation of the generation mechanism of the HM related tones and how the filter helps to suppress them, 2) some detailed analysis of the spur location and amplitude, and 3) the requirements for the filters to appropriately suppress the tones to a desired level. The results were backed by behavioral and schematic level simulation results.

Ring VCO based PLLs have many advantages over their LC VCO based counterparts, making them an attractive solution for many area intensive or coupling sen-

sitive applications among others. At the same time, calibration free fractional-N PLLs are attractive circuits due to their robust operation, ease of implementation, and improved locking time compared to PLLs that rely on calibration heavy circuits. Naturally, ring VCO based calibration-free fractional-N PLLs are a topic of great interest. However, both ring VCO based PLLs and fractional-N PLLs are known for their large noise compared to their LC VCO based or integer-N counterparts. Therefore, in this work, we propose a PLL architecture that combines the HM based PLL with a previously reported method that uses a nested PLL as a phase-domain filter. As a result, this PLL simultaneously achieves a wide loop bandwidth to suppress the ring VCO phase noise, and effective suppression of the quantization noise coming from fractional-N operation. The implemented design achieves an FoM of -227.6dB at 3.1GHz using a 50MHz reference, which is a state-of-the-art value among calibration-free ring VCO based fractional-N PLLs.

Based on the conventional second-order ΔΣ FDC(Frequency-to-Digital Converter)-PLL that can reduce phase noise with noise shaping, we proposed a higher-order MASH(Multi-stAge noise SHaping) 2-k FDC-PLL for a wider loop bandwidth and lower phase noise. The MASH 2-1 FDC-PLL can be designed by using a SAR ADC for the first stage, and using a ΔΣ ADC with FIAs(Floating Inverter Amplifiers) for the next stage. We designed the proposed FDC-PLL in 65nm CMOS process and demonstrated that the proposed FDC-PLL achieves -102dBc/Hz in-band noise and -230dB FoM with 26MHz reference clock by post-layout simulation.

High-Precision Analog-to-Digital Conversion Circuits and its Design Automation Techniques

Tetsuya Iizuka, Shuowei Li, Ryoya Shibata, Haoming Zhang, Yo Kumano, Ritaro Takenaka

Analog circuits based on standard cells have numerous advantages, such as high reusability, high integration, compatibility with automated design, and reliability, making them highly promising for current and future research. In this study, we propose a novel design for a synthesizable SAR CADC that uses entirely standard cells, enabling automatic placement and routing (P/R) using a commercial digital implementation tool. Due to the limited tape-out time, we opted to complete the P/R process manually for this prototype. We also suggest a differential architecture for this design that utilizes an inverter-based CDAC, which offers higher feasibility and a more extensive input range. Leveraging our previous research on MOSFET-based gate-voltage-independent capacitors, we propose an inverter-based gate-voltage-independent capacitor that can sample and hold the input voltage and generate the DAC voltage while mitigating its capacitance variation due to the input voltage by connecting the source and drain of the p-MOSFET and n-MOSFET in the inverter. Moreover, we demonstrate the principle of DAC voltage linearity compensation when using the extracted series-capacitor unit from the inverter as the CDAC unit. To switch analog signals, we propose a fully-inverter-based switch embedded in a dummy switch, eliminating the need for any uncommon digital cell or process in the overall design.

Stochastic resonance is a phenomenon where noise of a certain intensity contributes to system performance in nonlinear systems, and has been studied and applied in various fields. We have verified the effectiveness of applying this phenomenon to a successive approximation register analog-to-digital converter (SAR ADC), which requires multiple comparisons when performing analog-to-digital conversion in a binary search. In the proposed circuit, additional comparisons are repeated after the normal SAR ADC operation to achieve higher resolution. In addition, by using the noise in the circuit for stochastic resonance, the power normally used for noise suppression is reduced to achieve low power consumption. Optimal conditions for the number of the additional comparisons and noise intensity were obtained through the performance analysis and simulations, and the results show that the power efficiency of the proposed circuit is higher than that of a normal SAR ADC.

Dynamic circuit is a one type of CMOS integrated circuit. It's faster than static CMOS circuit while it cannot

be used in standard cell design since it's difficult to characterize because of its complex timing. In this research, we first proposed a timing model for dynamic circuit which we use to characterize the dynamic circuit, then we define several timing parameters for the dynamic cell based on this timing model. To get the values of the timing parameter, we did simulation of the circuit. And we used these values to construct a liberty file for the cell. After that, we execute the static timing analysis (STA) to verify it. To get a more accurate and convincing result, as a second part, we design a test structure to measure the required timing parameters for dynamic circuit characterization. After the chip is taped out, we will do the measurement and replace the simulation result with measured result to construct the liberty file for dynamic circuit.

For high-precision and power-efficient ADC design, we studied a fully dynamic discrete-time Delta-Sigma ADC using a Floating Inverter Amplifier (FIA). We have evaluated Correlated level shifting (CLS) and sampling noise cancellation techniques, which have been continued from the previous year, by actual measurements, and are investigating new techniques to further improve performance based on this measurement. A circuit configuration that cancels the noise effect of dither to achieve multi-bit quantizer and an integrator configuration with higher DC gain are required.

High-speed wireless and wired communications require high-speed, high-precision analog-to-digital converters (ADCs). Time-interleaving is a technique to speed up the conversion by operating multiple ADCs in parallel and is essential for multi GS/s ADCs. The performance of time-interleaved ADCs is severely affected by the errors between each ADC such as DC offset and clock skew, so it is important to minimize or calibrate them. For each factor, we proposed an optimal implementation based on theoretical analysis, and designed an 8-channel 4GS/s ADC in 28nm FD-SOI process. Simulated performance with noise and layout parasitics achieved a Schreier FoM of 161.6dB, which is higher than the state-of-the-art ADCs.

Design of Low-Noise Receiver for Deep-Space Probes

Tetsuya Iizuka, Takamichi Horikawa, Sota Kano

As there has been an increasing demand for the miniaturized spacecrafts in recent years, it has become essential to reduce the size and weight of the micro-wave transponders. Although current transponders use off-the-shelf electronic components to achieve downsizing, the combination of consumer products makes it difficult to guarantee long-term reliable operation during deep space exploration. To achieve miniaturization and reliability at the same time, one promising solution is to integrate the entire building blocks including the analog RF front-end as well as the digital signal processing on a single chip.

For deep space probes, receiver noise figure (NF) and radiation hardness are important specifications of the integrated receiver front-end. To avoid the very small signal from the earth being buried in the noise floor and unable to be demodulated, it is necessary to improve receiver sensitivity and dynamic range by minimizing the noise added in the circuits.

In this work, we proposed a 7.2 GHz on-chip receiver front-end with a narrowband noise-cancelling technique. In addition to the conventional receiver path consisting of a low noise amplifier (LNA) and a down-conversion mixer, an auxiliary noise-cancelling path is placed to cancel out the thermal noise caused by inductors in the LNA. The proposed receiver front-end is designed with radiation-hardened 130-nm SiGe BiCMOS process to mitigate the irradiation effects in the space. The schematic-level simulation using ideal behavioral models only for LO generation and GM blocks demonstrates 1.03 dB NF at room temperature, which is 1.61 dB lower than the case only with the main path. The temperature dependence can be compensated by calibrating the input bias voltage of the LNA.

Design of Time-Domain Neuron Devices and Evaluation of Learning Systems

Tetsuya Iizuka, Xiangyu Chen, Byambadorj Zolboo, Ckristian Duran, Shun Ito, Yuto Wakui

Deep neural networks (DNNs), which are the second generation of artificial neural networks (ANNs), have extensively explored in recent years for the growing number of applications. However, their huge energy consumption especially for the memory access in conventional von-Neumann architecture has forced people to find an alternative way to achieve more power-efficient solutions. Spiking neural network (SNN) is one of the attractive solutions as the third generation of ANNs that can realize a learning function with low power by mimicking biological neurons. SNNs consist of neurons and synapses, and are usually built using a bottom-up approach, which means that each component of the SNNs needs to be designed first.

Many hardware implementations of pulsed neurons or synapses have been reported. To implement the leaky integrate function of neurons, conventional designs usually build integrators with operational amplifiers (op-amps) and often use large on-chip capacitors and resistors to mimic the millisecond time constants of biological neurons. Moreover, to implement the neuron "fire" function, a dedicated circuit structure of a continuous-time or clocked comparator is usually used to set the threshold for neuron excitation. The bias current of the continuous-time comparator undoubtedly increases the power consumption of the neuron, while the clocked comparator requires additional clock signal distribution and the complex comparator structure occupies a large chip area. While more advanced processes can achieve low power consumption by reducing supply voltage and static leakage current, this also leads to a narrower dynamic range, smaller available margin, and degraded noise immunity of the voltage/current-domain analog circuits. This is detrimental to conventional neural networks that use analog quantities, such as voltage and current, to communicate with each other. On the other hand, thanks to the scaled transistors that have an improved operation speed with sharp signal transitions, the analog information can be represented more efficiently in time domain, i.e., a time interval of two signal transitions. This so-called time-domain circuit have another advantage in its power efficiency as it often consists of inverters or logic gates that ideally consume no DC power. Thus, time-domain circuits are ideal for future implementations of low-power SNNs.

TSMC 65nm process designed neuron, synapse, and weight circuits were prototyped and measured. The measured results were submitted to the APL, while a circuit was designed to expand the oscillation frequency range of the created synaptic circuit to solve the problem of the small oscillation frequency range of the synaptic circuit used to implement the SNN. The circuit was designed using TSMC's 65nm process, and the first prototype was able to expand the oscillation frequency from 15Hz to 130kHz. This oscillation frequency range is based on actual measurements. This was achieved by changing the oscillator part to a differential inverter and grounding the NMOS source of the oscillator. However, to output an oscillation frequency of 130 kHz, it was necessary to use a 10 MHz input, which did not match the input-output order; in the second prototype, the oscillation frequency could be increased from 400 Hz to 6 MHz. These values are from simulations with parasitic capacitance; it allows for inhibitory inputs in addition to excitatory inputs, and a Schmitt trigger inverter was added to prevent chattering. The steady-state value of the oscillation frequency is 20 kHz, with a maximum output frequency of 6 MHz with excitatory input and a minimum output frequency of 400 Hz with inhibitory input. The input frequency is 10 MHz for the maximum output frequency of 6 MHz, solving the problem of the 1st prototype input and output not matching the order of the frequency. These two circuits solved the problem of the small oscillation frequency range of the synaptic circuit.

In addition, we tested whether sine waves can be learned correctly by connecting actual designed synaptic circuits together, using the spiking neural network. As a result, only sine waves around a specific frequency could be learned. Since the frequency at which learning was possible varied up and down in the simulation using imagi-

nary circuits in which the voltage leakage and output frequency of the synaptic circuit were changed, it is considered necessary to use different circuits depending on what is to be learned.

Antenna Measurement and Testing Techniques for Wireless Communications

Tetsuya Iizuka, Mai Khanh Nguyen Ngoc, Byambadorj Zolboo, Sheng Guo

In 5G technologies, over the air (OTA) measurements are necessary for 5G antennas due to the technologies rely on millimeter-wave frequencies and small-sized terminals. The conventional OTA measurement is based on far-field measurement. However, the far-field measurement is almost infeasible in the millimeter-wave due to high path loss and low measurement accuracy. Therefore, near-field measurement takes place of OTA measurement in the millimeter-wave range. The far-field measurement data can be achieved from near-field measurement by using near-field to far-field methods.

In this research, there are plenty of challenges from hardware to software including automated near-field measurement equipment, millimeter-wave probe, and near-field to far-field transformation methods. In near-field measurement, one of the easiest ways is to measure S-parameters on the planar scanning area in front of the antenna under test (AUT).

For the near-field probing hardware and measurement setup, we design and fabricate a low-cost planar monopole on PCB. The proposed NF antenna operates at 28-GHz frequency by employing an arrow-shaped structure to enhance the total electric field at the head when point-by-point scanning on the AUT's surface. A prototype is then fabricated and measured to validate the simulation results. The measurement results of the proposed antenna show a wide bandwidth of 2.6 GHz and a center frequency of 28 GHz. In addition, we successfully built a compact anechoic chamber with automate motorized control for near-field measurement in mm-wave frequency range.

The far-field pattern has been achieved under 0.5 dB error within 120º on both elevation and azimuth directions when the measurement setup is correctly calibrated, and the measurement parameters is chosen with proper values. To capture such 120º range of the AUT, a probe with low directivity is necessary. The preliminary measurement results show that it is possible to effectively reduce the sampling points in near-field measurement to reduce the measurement time and cost.

Design of High-Sensitivity On-Chip Network Analyzer Circuits

Tetsuya Iizuka, Zunsong Yang, Yuyang Zhu, Zhenyu Cheng

A VNA system is a test instrument for measuring electrical network parameters, which is essential for radio frequency (RF) and microwave component analysis of a wide variety of passive and active devices, including filters, antennas, and power amplifiers. VNA can provide stimulus signal to the device under test (DUT) and measures the vector response over frequency with phase and magnitude information, like transmission, reflection, impedance measurements, as well as S-parameters S11, S12, S21, S22. Nevertheless, most VNA systems are external system, which are area-consuming and expensive. Meanwhile, it is also a challenge to test a very weak signal buried in noise that come out from the DUT in a wide frequency range (for us, is 1-5GHz).

In this work, we proposed an on-chip VNA with a phase interpolator (PI), a low-noise amplifier (LNA) and a lock-in amplifier (LIA), to test the S-parameter of our DUT, which contains two-port inputs and has ultra-low S21 and S23 parameters (the minimum can reach -95dB). The 1-5GHz PI is used to apply two phase-adjustable signals to the DUT for testing S23 parameter versus input phase difference. The LNA and LIA are used to measure the weak output signal from the DUT.

Until now, we have designed the whole circuit and finished the layout of the chips (including PI chip, LNA chip, LIA chip, and an overall chip containing all parts) in TSMC CMOS 65nm process. For PI, at 2.5GHz, the maximum DNL is 0.67LSB and maximum INL is 2.4LSB; at 5GHz, the maximum DNL is 0.38LSB and

the maximum INL is 3.24LSB. For the LNA, the post-simulation indicates noise figure of 3-5 dB over 1-5 GHz. For the whole system, the pre-simulation and post-simulation showed similar S21 and S23 curves to the measured results of our DUT, which suggests that the proposed structure can work properly. The real-chip test will be done after getting the chip.

The next step of our work is aiming to improve the noise performance of our system, at the meanwhile, a 1-5G PLL will be made to provide multi-phase clock signals for PI.

Verification of Topological Quantum State based on Electrical Circuits

Tetsuya Iizuka, Yuan Haochen

Topological quantum computing (TQC) is a method of fault-tolerant quantum computing, in which a single quantum gate could be generated by the braiding of certain topological quantum objects, named "anyons", and topological quantum computing has the natural property of being immune to decoherence and accurately executing predefined algorithms. One simplest realization of a non-Abelian anyon is a quasiparticle named Majorana fermion which obeys ordinary Fermi-Dirac statistics and owns a particular mechanism, Majorana zero mode (MZM). Therefore, we focus on the 1D circuit chain realization of Majorana zero-energy edge states to discover whether the MZM will appear at the boundaries, by measuring the nodes' two-point impedance between the left/right edge nodes.

Based on CMOS 180 nm process, we implemented integrated circuit realization of Su-Schrieffe-Heeger and Kitaev models on the chip. By simulating in the EM simulation tools and measuring on the real chip, we observe the impedance peaks at the edges of these chains demonstrating the existence of MZMs.

On the 1st version chip, for the Kitaev model, we have constructed three topological circuit chains with different resonant frequencies by adjusting the values of capacitors and inductors, also with three trivial chains for comparison. The rapidly increasing two-point impedance is found in the EM simulation and on-chip measurement at the topological phase, implementing the existence of MZMs at both edges.

Then, on the 2nd version chip, we added the CMOS switches to control the topological properties of the whole SSH chain and each unit cells in the Kitaev chain. We have observed from the measurement that impedance peaks emerging at the edges of the SSH model chains. On the Kitaev topological-trivial switchable circuit chain, by generating the proper control signals, we simulate how two topological segments moving, splitting and fusing on the Kitaev chains with two different resonant frequencies, and observe the impedance peaks at each topological-trivial boundaries in the real measurements, corresponding to the existence of zero-energy modes acquired for the braiding operations of the topological quantum computation.

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Variability in Nano-Scale CMOS Devices

Toshiro Hiramoto and Masaharu Kobayashi

As the size of MOS transistors is miniaturized, the effect of random variability of device characteristics is becoming too large to be overlooked. Although the main reason in conventional bulk transistors is the fluctuation of the number of dopants, the variability causes of nanowire transistors, which is one of the next-generation device candidates, remain unknown. In this study, we have clarified that the quantum confinement fluctuation caused by line width roughness is the new origin of random threshold voltage variability. We are also investigating the effect on the drain current variability.

Low Temperature Characteristics of Nano-Scale CMOS Devices

Toshiro Hiramoto and Masaharu Kobayashi

The quantum computing has attractive much attention for a future computing technology that is fundamentally different from classical computing by CMOS circuits. In the quantum computing systems, conventional CMOS

circuits are utilized to control quantum bits. Therefore, it is essential to clarify and model CMOS transistor characteristics at low temperature. In this study, we are studying the subthreshold swing of bulk and nanowire transistors. We are also evaluating the characteristics variability at low temperature.

Silicon Power Devices

Toshiro Hiramoto

Although new materials such as SiC or GaN are widely studied for power devices, silicon IGBT (Insulated Gate Bipolar Transistor) is still a mainstream device for power electronics in very wide range of rated voltages. In this study, we are pursuing the potential of silicon IGBT based on new concepts of IGBT scaling and double-gate IGBT.

Research on atomic layer deposition of oxide semiconductor and its application to 3D integrated memory devices.

Masaharu Kobayashi, Toshiro Hiramoto

While 2D scaling is getting challenging, 3D monolithic integration that requires active device formation in BEOL layers is getting more attentions. Oxide semiconductor is attractive because it can be formed in BEOL layers at low process temperature. Sputtering has been used for flat panel display device of oxide semiconductor, but cannot be used for conformal deposition on 3D structure. In this research, we developed In2O3 deposition method by using Atomic Layer Deposition (ALD). Then we designed 3D vertical channel ferroelectric transistor memory with HfO2-based ferroelectric. We demonstrated good memory characteristics and reliability by experiment.

Research on the physical understanding of the emergence of ferroelectricity in HfO2-based material

Masaharu Kobayashi, Toshiro Hiramoto

In this research, we aimed at elucidating the physical mechanism of the emergence of the ferroelectricity in HfO2-based material for 3D-structureed ferroelectric devices. This year, we illustrated that ferroelectric grains are horizontally aligned after crystallization anneal but they are vertically aligned after applying voltage cycling. This indicates that ferroelectricity can emerge even in 3D-structure.

Takagi Laboratory

(https://sites.google.com/g.ecc.u-tokyo.ac.jp/mosfet/)

III-V Metal-Oxide-Semiconductor (MOS) FETs and the 3-dimensional integration

Shinichi Takagi, Kei Sumita, Ryohei Yoshizu, Kasidit Toprasertpong, Mitsuru Takenaka

3D-integrated CMOS, in which transistors are vertically stacked, is expected to be a key device for future logic LSIs. In order to realize such stacked MOSFETs, channels such as III-V compound semiconductors and Ge are promising because they can be fabricated at low temperatures and are expected to have high mobility and injection speed. In our laboratory, we are investigating the identification of channel materials with high mobility in extremely-thin channel thickness, the realization of ultra-thin III-V-On-Insulator (III-V-OI) structures on Si substrates, and the performance improvement of III-V n-MOSFETs using these structures aiming at application to 3D stacked CMOS. In this fiscal year, we addressed the quantitative assessment of channel materials that can achieve high mobility even under thickness fluctuation (surface roughness) scattering, which is an important scattering mechanism that determines the mobility of thin-film channel MOSFETs, revealing the usefulness of (111) InAs-OI and (111) Ge-On-Insulator (GOI) n-MOSFETs, where electrons can transfer into the L-valleys. Furthermore, as a method to accurately determine the interface state density at the InAs MOS interfaces, we proposed an evaluation method using CV characteristics at cryogenic temperatures and experimentally demonstrated that the interface state density can be evaluated with high accuracy.

Ge Metal-Oxide-Semiconductor (MOS) FETs and the 3-dimensional integration

Shinichi Takagi, Chia Tsong Chen, Xueyang Han, Kasidit Toprasertpong, Mitsuru Takenaka

We are investigating the technology to realize ultra-thin Ge-On-Insulator (GOI) structures on Si substrates, the performance improvement of high-performance GOI CMOS using these structures, and the device physics that determines the electrical characteristics, with the aim of applying them to 3D integrated CMOS. In this fiscal year, we have demonstrated that high hole mobility can be obtained even in extremely-thin GOI p-MOSFETs by introducing uniaxial compressive strain into (110) Si-Ge-On-Insulator (SGOI) structures, fabricated by Ge condensation of (110) SiGe/SOI substrates. We also experimentally demonstrated that additional oxidation after the completion of Si oxidation in the Ge condensation process can introduce a larger tensile strain than expected by the thermal expansion coefficient.

HfO_2-based Ferroelectric devices

Shinichi Takagi, Kasidit Toprasertpong, Makoto Kawano, Koichiro Iwashige, Masaki Ootomo, Zhenhong Liu, Mitsuru Takenaka

MOSFETs using ferroelectrics (FeFETs) with polarization reversal as gate dielectrics and FeRAM using metal sandwich structures (MFM structures) as memory cells are expected to be future devices for ultra-low power memory and logic. In particular, devices based on ferroelectric and anti-ferroelectric materials such as $Hf_{1-x}Zr_xO_2$ and ZrO_2, which have been discovered recently, are of great interest because of their extremely high compatibility with current Si CMOS technology. We are studying the properties of these ferroelectric thin films deposited by an ALD method, the device operation principle of FeFETs, and the optimum device structures to realize excellent device characteristics. In this fiscal year, we investigated the mechanism that determines the memory window of FeFET memory, proposed an analytical expression for it, and clarified the impacts of various physical parameters on the memory window. Also, we found that, in a 4 nm-thick ultra-thin MFM capacitor for FeRAM applications, the low operating electric field decreases the polarization due to fatigue of the ferroelectric film occurs, whereas this fatigue can be recovered by applying a higher electric field pulse.

Reservoir computing based on ferroelectric devices

Shinichi Takagi, Kasidit Toprasertpong, Eishin Nako, Rikuo Suzuki, Mitsuru Takenaka, Ryosho Nakane

Reservoir computing has recently attracted attention as an AI computation method with computational load for learning. We have proposed that FeFETs and FeRAMs with memory-in-logic and nonlinear analog computation capabilities are promising hardware for the physical implementation of reservoir computing. Thus, we are searching for methods to improve AI performance of reservoir computing based on ferroelectric devices by examining operating schemes and device characteristics. In this fiscal year, we demonstrated that AI performance can be improved by utilizing not only drain current but also source current and substrate current as output data. For application to speech recognition, we proposed a system that performs the task of spoken digit classification using a parallel-operating FeFET reservoir and experimentally achieved a classification accuracy of 95.9%.

Understanding of Si CMOS operation under ultra-low temperatures for quantum computing application

Shinichi Takagi, Minsoo Kang, Yutong Chen, Kasidit Toprasertpong, Mitsuru Takenaka

In quantum computing systems, Si CMOS circuits that can operate at cryogenic temperatures such as 4 K must be placed close to the qubit chip in order to improve the number of qubits. For this purpose, we are conducting experimental and theoretical studies to quantitatively describe the electrical characteristics of MOS transistors at cryogenic temperatures and to clarify their physical mechanisms. In this fiscal year, we experimentally evaluated the change in SS (sub-threshold swing) values of Si n-MOSFETs with different substrate concentrations from room

temperature to 4 K. We found that the tail states and localized interface states near the band edge, which affect SS values, increase with an increase in the substrate concentration, and that the tail states and localized interface states have a similar physical origin, judging from the experimental results of the substrate bias dependence of the SS values.

Takenaka Laboratory

(https://sites.google.com/g.ecc.u-tokyo.ac.jp/takenaka-lab/)

On-chip/Off-chip optical interconnect

Mitsuru Takenaka, Rui Tang, Hanzhi Tang, Yuto Miyatake, Tipat Piyapatarakul, Kazuma Taki, Taketoshi Nakayama, Tomohiro Akazawa, Sheng Fu, Hiroya Sakumoto

We have been conducting research on optical interconnection and I/O of LSIs using silicon photonics and other technologies. We have successfully demonstrated a Si hybrid waveguide-coupled photodetector using an InGaAs membrane on a Si slot waveguide. Using a Si slot waveguide, the absorption in the InGaAs membrane can be enhanced. As a result, we have successfully achieved a high responsivity and low capacitance simultaneously.

Si photonic integrated circuit for AI

Mitsuru Takenaka, Rui Tang, Hanzhi Tang, Yuto Miyatake, Kazuma Taki, Mingzhi Huang, Tomohiro Akazawa, Masahiro Fujita, Yosuke Wakita

We have been conducting research on deep learning for AI using programmable photonic circuits such as universal optical circuits. We have developed a new phase change material, GeSbTeS (GSTS) and demonstrated that the optical absorption of GSTS is reduced significantly at a wavelength of 2.34 μm. As a result, we have successfully demonstrated a low-loss optical phase shifter using GSTS.

Ge mid-infrared photonic integrated circuit

M. Takenaka, Yuto Miyatake, Chao Zhang

We have been studying mid-infrared photonic integrated circuits based on Ge waveguides formed on Ge-on-insulator (GeOI) wafer. We have successfully demonstrated avalanche photodetection through defect-mediated process using a Ge waveguide with a lateral PIN junction We have achieved the device operation at > 1 Gbps.

2D material devices

Mitsuru Takenaka, Tipat Piyapatarakul

We have been studying semiconductor devices using graphene and molybdenum disulfide. We have proposed a new MOS-based optical modulator using a III-V membrane waveguide with a graphene transparent electrode. Since the optical absorption and resistivity of the graphene electrode can be reduced simultaneously by doping, we have numerically revealed that the proposed modulator enables low-loss and high-speed modulation.

Uchida Laboratory

(http://www.ssn.t.u-tokyo.ac.jp)

In the Internet-of-Things (IoT) era, every physical device will be connected to network. In this framework, any physical devices will have sensors that will continuously obtain various kinds of physical as well as chemical information around us. We expect that big data consisting of these sensor outputs will be analyzed with AI and valuable information will be extracted to improve our quality of life. In our group, low-energy sensors and information processing devices have been developed by pursuing physics of nano-mateials and nano-devices. Recent research topics are as follows.

1. Metal nano-film sensors for breath diagnosis
2. Thermal transport analysis of nano-meterials for low-energy sensors
3. Electron-phonon interactions at the interface of insulator and semiconductor
4. Supramolecular sensors
5. Information processing devices beyond von Neumann architecture

Someya-Yokota-Lee Laboratory

(http://www.ntech.t.u-tokyo.ac.jp/, https://fles.t.u-tokyo.ac.jp/)

Improvement of photo-stability in Organic Photodetectors

Wijaya Theodorus, Tomoyuki Yokota,
Sunghoon Lee, and Takao Someya

By using optical devices, biological information such as blood pressure, pulse rate, and blood oxygen concentration can be non-invasively acquired. We have successfully improved the stability of organic photodetectors by using an electron transport layer (ETL) made of thermally treated zinc oxide (ZnO) or the mixture of ZnO and polyethyleneimine (PEI). The sol-gel method, which is highly compatible with flexible substrates, has been widely used to form ZnO ETL. However, the conventional annealing temperature was low at 180°C, and there was a problem of traps in the ETL due to the presence of remaining precursors. These traps are considered to be one of the causes of increased dark current when exposed to light. For wearable sensor applications that require long-term stability, it was necessary to improve the stability against light irradiation. It was found that increasing the annealing temperature of the ZnO layer to 350°C dramatically improved photo-stability. This is believed to be due to the reduction in trap density caused by the high annealing temperature. Furthermore, by using a mixture of ZnO precursor and the polymer PEI as PEI-Zn in the electron transport layer, we succeeded in reducing the trap density and improving stability even at the conventional annealing temperature of 180°C. Additionally, by integrating these devices with organic light-emitting diodes, we have successfully realized a wearable pulse wave sensor that can be attached and used in everyday life to sense pulse waves over a long period of time.

Mita Laboratory

(http://www.if.t.u-tokyo.ac.jp)

TopoMEMS: Development of Ideal Variable MEMS in view of Future Topological Quantum Computing

Y. Mita, K.Tsuji, A.-C.Eiler,A.Higo, T.Iizuka, Z.Xu,
M.Ezawa (Dept. Applied Physics)

Recently, new computation methods that use Topological nature are drawing much attentions in view of future Quantum computing. Calculation takes advantages Topological natures existing in several different fields expressed as Hamiltonian matrices. Our team, granted by JST CREST project, tries to explore electrical expression of Hamiltonian matrices used for computation. Team Mita will develop ideal variable electrical devices as well as ideal MEMS devices. We named such devices and systems "TopoMEMS". As an initiating study, we have taken Su-Schriffer-Heeger model. We have developed a MEMS state-variable capacitor integrated SSH electrical circuit and have been successful in Topological / Trivial state switching due to MEMS device. The result has been presented in the top MEMS conference. Then, we have identified another interesting computation scheme by directly using dynamics of MEMS. Towards that end, a bistable MEMS actuator towards MEMS Ising machine was published in peer-reviewed journal, and multi-level bistable MEMS actuator has been accepted in the top international conference..

Programmable Matter - Study on LSI-MEMS energy-autonomous distributed microsystems for realization of deformable matter

Y. Mita, K.Misumi, N. Usami (Dept. of Aeronautics and Astronautics), E. Lebrasseur,
G. Hwang (LIMMS, CNRS-UTokyo IIS / CNRS C2N),
G. Ulliac, (LIMMS, CNRS-UTokyo IIS, FEMTO-ST),
J.Bourgeois, B.Piranda (FEMTO-ST, France),
S. Delalande (Groupe PSA, France)

As one example of future integrated MEMS that is expected to open new research and industrial application fields, the authors are trying to show a top-down applica-

tion of energy-autonomous distributed microrobots. A number of identical tiny robots, sized below 1cm, will be released in an environment. Individual robot can communicate with their neighbor, stick each other, and share energy, to realize cooperative function. The PI is receiving a French National Research Center (ANR) grant on behalf of host professor of CNRS laboratory in the Institute of Industrial Science (LIMMS, CNRS-IIS, UMI 2820), together with FEMTO-ST Laboratory and PSA-Peugeot Laboratory for such "micro robots that can realize deformable substance by cooperative action, named Programmable Matter". In year 2020, an electrostatic chucking actuator system that attaches and detaches the external skeleton of the Matter has been presented in an international conference. Based on the actuation force electromagnetically analyzed, the ideal structure of the flexible electrode (named Flexiboard) has been identified, and a reliable integration process with thinned high-voltage photovoltaic cells have been presented in the international conference.

Integration of electrode devices on MEMS fluidic devices

Y. Mita, A.-C. Eiler, A. Higo, T.Ezawa, E.Ota,
Y.Okamoto (AIST), N.Washizu (Advantest),
A.Takada (Advantest), M. Fujiwara, T.Sawamura

Towards the goal of production of brand-new sensor devices with higher sensitivity and functionality, the team is working on small-gap electrode fabrication process. This year, we have post-processed Fully-Depleted SOI VLSI device for massively parallel measurement and its integration is underway.

Fine Large-Area Electron Beam Lithography Exposure Methods

A. Higo, Y. Ochiai, M. Fujiwara, T.Sawamura, Y. Mita

The team explores newly-acquired (in 2013) rapid electron beam writer F7000S-VD02. The capability of high electron dose and sharp edge due to cell (character) projection machine configuration is being examined. The breakthrough in question is to extend the large-area EB lithography, whose pattern approximation have been limited to rectangular shapes, into expressing free-form smooth shapes and a number of periodical small patterns. This year, pattern and process design has been successful to obtain gap structure less than 16-nm wide. The result has been presented as a peer-reviewed journal.

Universities-Industries collaborative research on highly-functional system by MEMS post-process of CMOS-VLSI

Y. Mita, T. Yamaguchi, S. Nakajima,
R. Shimamura, T. Lévi(IMS-CNRS,Bordeaux),
G. Larrieu (LAAS-CNRS,Toulouse), Y.Ikeuchi (IIS),
K.Saito (Nihon Univ.)

The research targets are new sensor devices, made by post-process at clearnrooms such as d.lab Takeda Supercleanroom and others, of VLSI wafer made through VDEC. The important finding has been that VLSI wafer acquired just after transistor fabrication could sustain processes even with heat treatment, such as deposition, ion implantation, and drive-in. In 2016, a VLSI device made on Silicon-on-Insulator (SOI) wafer was successfully Deep-RIE processed. The industrial interest is its versatility – many different types of application devices, which differ one from another according to request of market, can be fabricated by using the same technology. More and more companies are interested in the scheme and are working on the technology on the collaborative research projects, including international cooperative research projects. This year, a world's lowest-level (1.5V) soft microactuator with highest figure-of-merit has been developed and presented in a peer-reviewed journal paper and domestic conference (was late news award finalist).

Test Structure for high-density CMOS-MEMS hybrid integrated Technology

Y.Mita, H. Matsuoka, Y.Ebihara, A.Mizushima,
T.Yoda (TITech), K.Hirakawa (TITech),
M.Iwase (TITech), M.Ogasawara (TITech),
A.Higo and Y.Ochiai

Chip-level highly-dense bonding integration is drawing

high attention to simply obtain high-functional system; it has been almost impossible to individually examine pad-to-pad connections, whose size is in an order of several microns and whose number is order of 1 million. New test structures and methods are mandatory. We have proposed a two-pads-per-probe scheme, in which one of the pad is used for testing pad to make what we call “loop-back test”. A test LSI have been designed, fabricated, and integrated with gold bumps as well as MEMS test structures.

Appendix

A.1 VDEC CAD Tools

Since 1996, VDEC has provided CAD software licenses to the registered researchers in universities and colleges in Japan. The CAD tools we provided in 2023 through the activities of VDEC in Systems Design Lab (d.lab) are shown in Table A.1.1. The researchers can use those CAD tools when their local machines, whose IP addresses are registered in advance, are authorized by one of VDEC license server located in the ten VDEC subcenters shown in Figure A.1.1. For each CAD tool, VDEC provides 10-1000 floating licenses. Those CAD tools can be utilized only for research and education activities in national universities, other public universities, private universities, and colleges.

Table A.1.1 VDEC CAD tools

Name	Function	Vendor
Cadence tool set	Verilog-HDL/VHDL entry, Simlation, Logic synthesis, Test pattern generation, Cell-based (including macros) place, route, and back-annotation, Interactive schematic and layout editor, Analog circuit simulation, Logic verification, Circuit extraction	Cadence Design Systems, Inc.
Synopsys tool set	Verilog-HDL/VHDL simulation, Logic synthesis, Test pattern generation, Cell-based (including macros) place, route, and back-annotation, Circuit simulation, Device simulation	Synopsys, Inc.
Siemens tool set	Layout verification, Design rule check	Siemens Electronic Design Automation Japan K.K.
Silvaco tool set	Fast circuit simulation	Silvaco Japan Co., Ltd.
ADS/Golden Gate	Design and verification of high-frequency circuits	Keysight Technologies
Bach system	BachC-based design, synthesis, and verification	Sharp
LAVIS	Layout visualization platform	TOOL

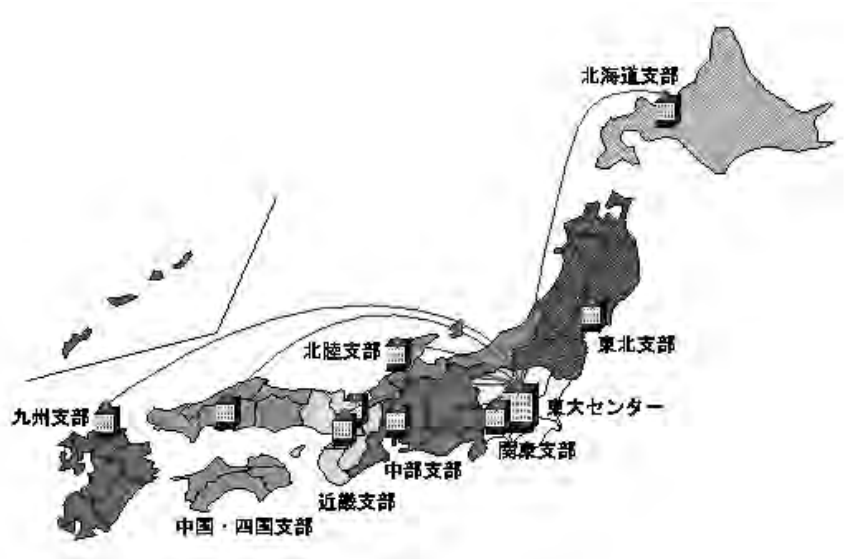
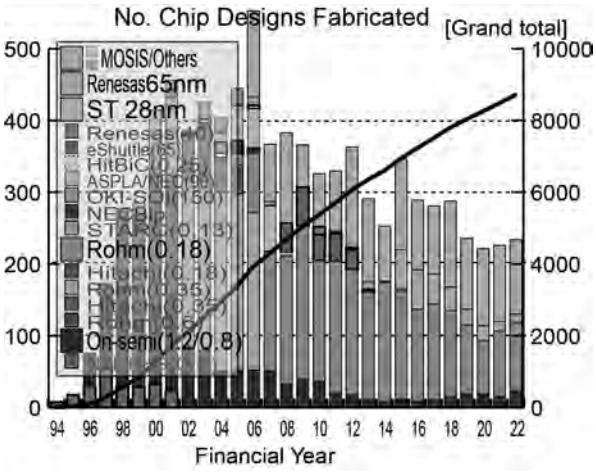


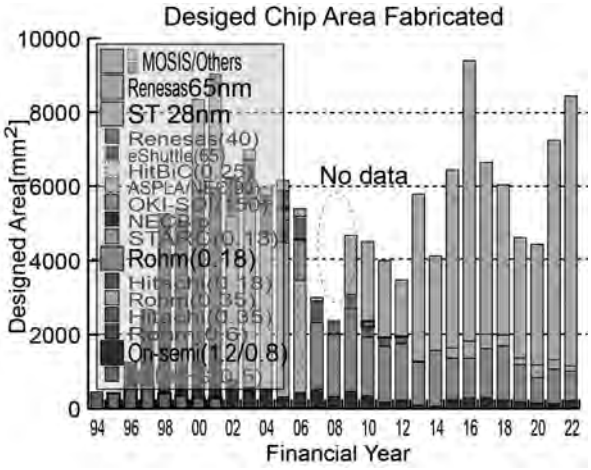
Fig. A.1.1 VDEC Subcenters

A.2 Status of Chip Fabrication Support at Platform Design Research Division

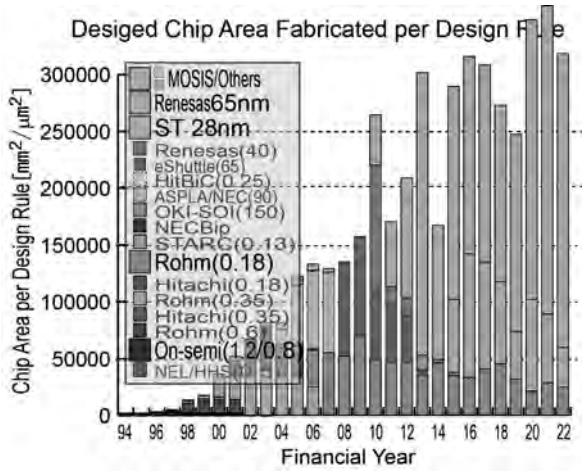
As for the support for VLSI chip prototyping, in the pilot project in FY 1994 and 1995, there was only one foundry, NEL's CMOS 0.5μm (the process was later continued by Hitachi Hokkai Semiconductor). After the inauguration of VDEC in 1996, the 1.2-μm CMOS process of Motorola Japan (which was continued by ON Semiconductor in 1999) started cooperation, and the 0.6-μm CMOS process of ROHM was added in 1997. In 1997, CMOS 0.6μm from ROHM was added, followed by 0.35μm from Hitachi, Ltd. in 1998, and 0.35μm from ROHM in 1999. In addition, as part of the IP development project, a prototype of STARC 0.13μm was developed. Since FY 2001, we have been providing services of CMOS 0.18μm from Hitachi, Ltd. In 2002, under the leadership of Dr. Iwata of Hiroshima University, we conducted a trial trial fabrication service in cooperation with VDEC and MOSIS. This service provides overseas fabs such as TSMC and IBM at low cost through MOSIS. Furthermore, under the leadership of Dr. Shibata of the University of Tokyo, NEC Compound Device, Inc. provided a prototype service for bipolar LSI. In 2004, we started prototyping Oki Electric CMOS SOI 0.15μm process and ASPLA 90nm process as test prototypes, and the 90nm prototype was operated as a regular prototype from 2005 in the form of public solicitation. In FY2006, we started trial production of 0.18μm process by ROHM and test production of 0.25μm SiGeBiCMOS by Hitachi, Ltd. In FY 2007, we started to study an advanced process to succeed 90nm CMOS, which was terminated in FY 2007, and in FY 2008, we started trial production of eShuttle's 65nm CMOS. In addition, as part of the METI-STARC project "Next Generation Semiconductor Circuit Architecture Commercialization Support Project," prototype production using Renesas Electronics' 40nm CMOS was also started. On the other hand, CMOS1.2μm was terminated in September 2011, Renesas Electronics' 40nm CMOS prototyping was terminated in 2012, and eShuttle's 65nm CMOS prototyping was terminated in August 2013. As a successor to CMOS 1.2μm, a test prototype of CMOS 0.8μm was conducted in October 2012 with the cooperation of Onsemi-Sanyo Semiconductor Manufacturing Co. As for the leading-edge prototyping,



(a) Trend of number of designs fabricated.



(b) Trend of designed area.



(c) Trend of designed area normalized by design rule.

Figure A.2.1 Trend of number of designs and designed chip area.b

STMicroelectronics started FD-SOI 28nm CMOS prototyping through CMP of France in FY 2013. In addition, we started SOTB 65nm CMOS prototyping by Renesas Electronics as a regular prototyping in FY2015, and concluded in FY2022. In FY2021, we started BiCMOS 0.18um prototypes under an agreement with IHP of Germany.

Fig. A.2.1(a) shows trends of number of chip designed for VDEC chip fabrication. For the first 6 years until 2001, the number of designed chips shows steady increase, which means drastic improve of the effectiveness researches and education of LSI design, and we assume drastic increase of number of students related to LSI chip design and education. During few years of stable number around 400 chip designs per year, we can see transition of designs toward finer process. In 2007, we saw a large drop, which was caused by sudden process transition from 0.35μm CMOS to 0.18μm CMOS, and in 2008, we also saw another drop by process transition from 90nm CMOS to 65nm CMOS.

Fig. A.2.1(b) shows trends of designed chip area, which shows much clear trends of drop by process migration. On the other hand, Fig. 2.3.1(c) shows trends of designed chip area normalized by design rule, which assume to be strong relation with design efforts. Coming from the fact that the normalized chip area is still growing, we assume the major reason for decrease of number of chips and designed area is increase of design effort per chip and per unit area due to process scaling.

Fig. A.2.2 shows trends number of professors and universities fabricated chip. Number of professors who have contracted NDA for process technologies to access design rules and design libraries are, 93, 294, and 55, respectively, for 65nm CMOS, 0.18 μm CMOS, and 0.8um CMOS.

Table A.2.1 lists chip fabrication schedule in 2022. Please refer to list in Appendix B for details of designers and contents of chip designed.

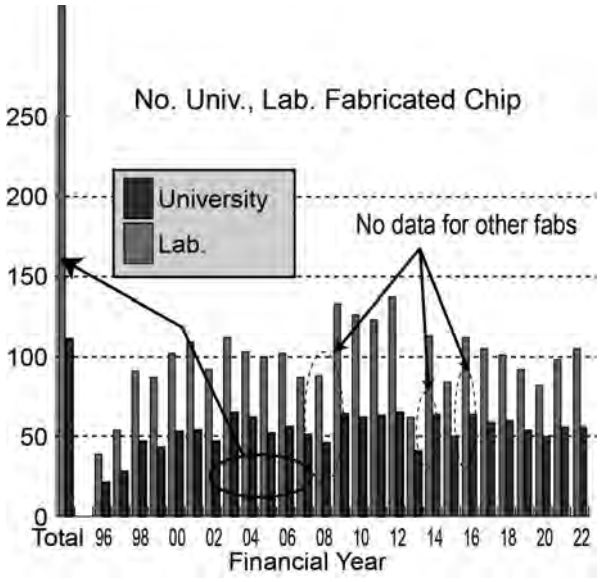


Figure A.2.2 Trend of number of processors and universities fabricated chip.

Table A.2.1 Chip fabrication schedule in 2022

0.8 µm CMOS (On-Semiconductor - Sanyo)

	Chip application deadline	Design deadline	Chip delivery
2021 #1	2022/7/4	2022/9/26	2023/1/31
2021 #2	2023/1/10	2023/3/27	2023/6/6

0.18 µm CMOS (Rohm)

	Chip application deadline	Design deadline	Chip delivery
2021 #1	2022/4/4	2022/6/27	2022/9/27
2021 #2	2022/6/13	2022/9/5	2022/12/20
2021 #3	2022/8/1	2022/10/24	2023/2/7
2021 #4	2022/12/5	2023/2/27	2023/6/19

SOTB 65nm CMOS

	Chip application deadline	Design deadline	Chip delivery
2022 #1	2022/6/13	2022/7/25	2023/3/E

A.3 Seminar

Seminars are always needed as the advancement of LSI design technology. In 2022, VDEC has held CAD Seminar and Designer's Forum, for academic circuit designers.

A.3.1 CAD Seminar for VDEC users

Along with advancement of circuit design CAD tools, tutorials on these tools are highly demanded. VDEC offers the CAD Seminar twice per year. In the CAD Seminar, VDEC invites lecturers from venders including Cadence, Synopsys and Keysight to give tutorials on their CAD tools. The seminar is held in VDEC, The University of Tokyo and VDEC sub-centers simultaneously in several universities nationally, in March of one fiscal year. Each tutorial takes one or two days.

Table A.3.1 CAD technical seminar in 2022 fiscal year

CAD Seminar I

Date	Tutorial	Venue	Number of Applicants
2/28-3/1	Keysight ADS Advanced	online	34
3/13-14	Cadence Virtuoso Layout Suite-L	online	72
3/15	Cadence Clarity 3D Solver	online	21
3/13-17	Synopsys TCAD (On-Demand　Web Training)	online	47
3/13-17	Synopsys IC Compiler II (On-Demand　Web Training)	online	73
3/17	Synopsys Q&A Meeting	online	22
3/28	Cadence Innovus Digital Implementation System	online	34

A.3.2 Designer's Forum for academia

VDEC LSI designer forum intended for students and young teachers were held. The VDEC LSI designer forum has aimed to sharing the information that generally hard to be obtained common technical reports or academical papers, such as the failure an LSI designer had been through and the solution, and the construction method in the design milieu in the laboratory.

Table A.3.2 Program of Designers Forum in 2022

9/30-10/1 Hybrid　Attendees: On-Site 28, Online 7	
9/30	
13:00-	Reception
13:30-13:35	Opening
13:35-14:35	Keynote Speech
14:35-14:45	Lunch
14:45-16:05	Design Award Presentation I
16:05-16:10	Break
16:10-17:10	Design Award Presentation II
17:10-17:15	Break
17:15-18:15	Design Award Presentation III
10/1	
9:00-10:00	Design Award Presentation IV
10:00-10:45	Idea Contest Presentation
10:45-10:50	Break
10:50-12:20	PhD Session
12:20-	Voting and Award Ceremony

A.4 Venture companies related to VDEC

Some professors related to VDEC started venture companies. The following is a list of the venture companies related to VDEC.

[1] AIL Co.,Ltd. (http://www.ailabo.co.jp/)

Related professor : Professor Kazuo Taki, Kobe Univ. (Representative Director)

Description of business : (1) LSI design service
(2) Engineer dispatching service
(3) Recruitment
(4) Management consulting

[2] Synthesis Corporation

(Merged with Soliton Systems on July 1st in 2017, http://www.synthesis.co.jp/)

Related professor : Professor Emeritus Isao Shirakawa, Osaka Univ. (Director)

Description of business : (1) System LSI development and design service
(2) IP development and sales
(3) Development and sales of IPs
(4) Development of EDA tools

[3] ASIP Solutions (http://www.asip-solutions.com/)

Related professor : Professor Masaharu Imai (Representative Director, CTO)

Description of business : (1) R&D, education and consulting of IoT application system
(2) Sales of ASIP design tool and consulting of ASIP development

[4] Nanodesign Corporation (http://www.nanodesign.co.jp/)

Related professor : Professor Kazuyuki Nakamura, Kyushu Institute of Technology. (Representative Director)

Description of business : (1) LSI design and development
(2) Development of LSI CAD and LSI evaluation tools
(3) Design consulting, etc.

[5] A-R-Tec Corp. (http://www.a-r-tec.jp/)

Related professor : Professor Emeritus Atsushi Iwata, Hiroshima Univ. (Representative Director)

Description of business : (1) Analog IC design and measurement
(2) PCB noise analysis
(3) Develop human resources, OJT, Lecture

[6] Ishijima Electronics (http://ishi.main.jp/)

Description of business : (1) Electronic circuit and board development
(2) Software development
(3) Consulting

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