Systems Design Lab

東京大学大学院工学系研究科
附属システムデザイン研究センター
先端設計研究部門・先端デバイス研究部門
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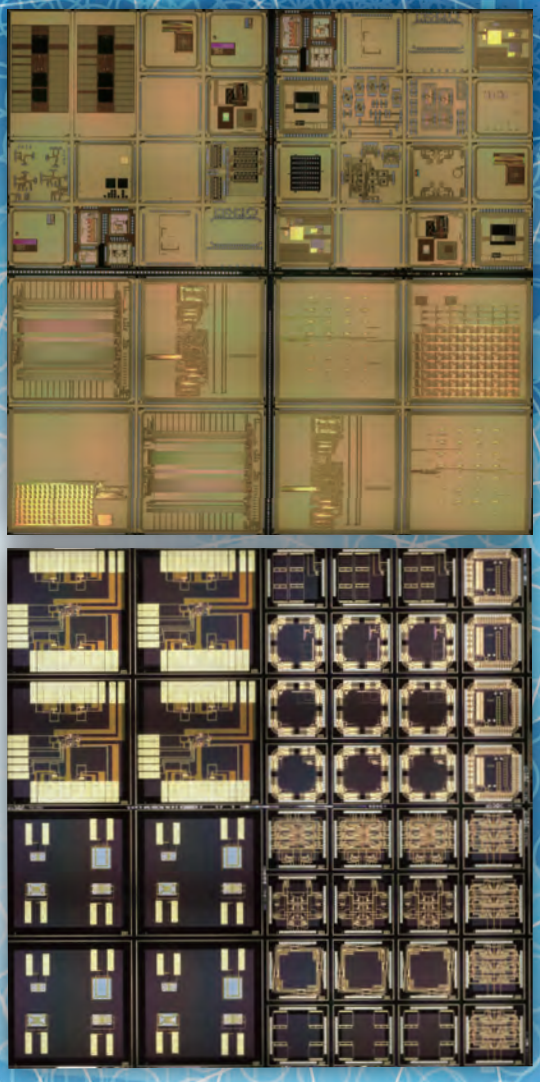
Systems Design Lab, School of Engineering, (VLSI Design and Education Center), The University of Tokyo
Annual Report



Systems Design Lab, School of Engineering
The University of Tokyo 2024

Message from the Director of d.lab

Tadahiro Kuroda

Director
Systems Design Lab (d.lab)
School of Engineering, The University of Tokyo

The book ***Chip War*** by Chris Miller has won a wide audience. As its subtitle of *The fight for the world's most critical technology* suggests, it depicts in detail the history of the battles between nations in the area of semiconductors.

But ***Chip War*** describes only one scenario; there are other possibilities for the future. That was the motivation for me to write the book that I originally called *Semiconductor Democracy*. The book was eventually published in Japanese with the modified title of *The Super-Evolution of Semiconductors – The Future of the Technology that Dominates the World*.

The future described in the book is as follows.

◇◇◇◇◇◇◇◇(Translated from the Postscript)

Semiconductor democracy and chip war are two sides of the same coin. In this book, my focus is on semiconductor democracy.

In the 19th century, Otto von Bismarck explained in a speech how iron made a nation. Indeed, iron created contemporary cities and gave birth to weaponry.

Today, the technology battleground is in semiconductors. Semiconductors make a nation. What will semiconductors create, and what will they break? It will be up to our imagination and wisdom.

Chip makers are engaged in fierce battles to dominate in the manufacturing of next-generation semiconductors.

However, semiconductors are evolving into such a giant collection of technologies that the challenges can no longer be overcome by a single corporation or even a single country. We really should think of semiconductors as a global commons.

As a result, we should not be instigating semiconductor wars; instead, we need to be building ecosystems.

Technology is getting more and more complex. Therefore, we must look at the entire forest instead of the individual trees. The challenge ahead for the world is how to nurture the forest, or in other words, create a rich industrial ecosystem.

We can take hints from the botanical world.

Nowadays plants flourish everywhere across the globe. The revolution that created the world of today was started by flower-bearing plants.

A co-existence relationship born between flowers and insects resulted in their co-evolution where one evolved by promoting evolution in the other, and vice versa.

The birth of flowers provided the trigger for the accelerated evolution of life forms.

According to Darwin's theory of evolution, only the fittest survive and are able to continue their family lines. In a nutshell, life is about competition. However, the hidden mechanism of evolution that is being uncovered by the latest science is that living organisms not only compete with each other but also cooperate to help each other. That is the essence of the theory of super-evolution.

Similarly, to enrich the "semiconductor forest," it is important to find its "flower." It was with that thought in mind that I set forth my theory of the super-evolution of semiconductors in this book.

I started by describing how high-performance semiconductors are developed from the standpoints of More Moore and More than Moore.

Next, I shared my thoughts on what high-performance semiconductors can create from the standpoint of innovation, or in other words, the standpoint of More People.

Will we be able to find the "flower" that is needed to evolve semiconductors from the age of competition to the age of co-existence and co-evolution? It is going to take more than capital and Moore's Law to make semiconductors a global commons.

The need is to get many people involved. That is More People.

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One other point I would like to bring up is agility.

◇◇◇◇◇◇◇◇(Translated from Chapter 1, Section 4, "The Semiconductor Forest: Co-existence and Co-evolution")

Eventually, flowers acquired new power.

It was the shortened lifecycle. The time from pollination to fertilization was shortened from one year to a few hours. That resulted in accelerated evolution of all life forms.

$y = a(1+r)^n$

That is the formula for calculating compound interest, where r is the interest rate and n the number of times interest is compounded. Even if you start with a small principal a, the future value can grow large if you continue the compounding for a long time.

If you replace n with $1/t$, where t is the development cycle time, you get the fundamental equation for the digital economy. The same equation applies to both the improvement in chip performance and the growth of a company.

Put differently, the strategy to grow the digital economy is to repeatedly iterate the improvement cycle at high speed. Rather than the amount of improvement (r), the key is to increase the number of times improvement is made (n), or in other words, reduce the development cycle time (t).

That is why we want to be agile.

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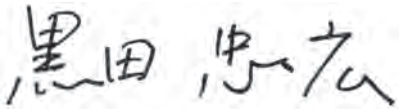
The book presents the fundamental thinking of d.lab. I would appreciate it if you would get hold of a copy and give it a read.



Systems Design Lab

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C O N T E N T S

Chapter 1 Introduction to d.lab

The VLSI Design and Education Center (VDEC) was established at the University of Tokyo in 1996. At the time of its founding, Japan's semiconductor industry held a 50% share of the USD 50-billion global market, and engineers who could hit the ground running were in high demand. VDEC has since provided unparalleled, outstanding education to develop many high-caliber engineers for the semiconductor industry.

However, have these graduates of VDEC been able to fully realize their potential? In the last quarter century, even though the global semiconductor market enjoyed a rapid 7% annual growth rate, Japan's share continued to shrink, falling to the current level of about 10% of a market that is now approaching USD 500 billion.

The current semiconductor business is one of mass production of high volume, low margin general purpose chips. General purpose chips have been able to achieve large volumes because of the wide adoption of the von Neumann computer architecture constructed with the combination of memory and processor chips. While Japan led the world in memory device innovation, it lost the business competition on capital investment.

The mass production, mass consumption model has its limits. Because of the excessive burdens it places on the environment, the world is now facing an energy crisis. The recent trend of applying AI to big data analysis is fueling further growth in energy consumption.

In the middle of this development, a game changer has emerged. Recognizing that it is hard to compete by using general purpose chips procured from semiconductor makers, technology giants including GAFA have started to develop their own specialized logic chips in-house.

In response to this paradigm shift, the University of Tokyo established the Systems Design Lab (d.lab) in October of 2019 and formed a strategic alliance with TSMC a month later. d.lab was formed by establishing the Advanced Design Research Division and the Advanced Device Research Division and adding them to the existing Platform Design Research Division and Platform Device Research Division which had been operating VDEC and the Takeda Clean Room. Subsequently in October of 2020, d.lab started an industrial partnership program which has grown to include more than 40 corporate members.

Furthermore, the Research Association for Advanced Systems (RaaS) was founded in August of 2020 to lay out the framework for the university to collaborate with both the industry and the government. Using d.lab and RaaS to realize a two-pronged strategy of open and closed collaboration respectively, the university is actively promoting cooperation between academia and society as well as collaborative creation with industry. Our research aims to boost the time-performance of semiconductors, with target goals of 10x increase in both energy and development efficiencies.

Japan is aiming to transition from the current industrial/information society to Society 5.0, a human-centric society where knowledge is value. In this knowledge-based society, semiconductors will evolve from being a necessity of industry to the brain cell of society.

What strategy should the semiconductor industry pursue to address this evolution? It is d.lab's mission to find the answer.

Tadahiro Kuroda
Director, Systems Design Lab

Chapter 2 d.lab Overview and FY2023 Annual Report

2.1 Advanced Design Research Division

2.1.1 Division Overview

The Advanced Design Research Division faculty consists of four professors, one associate professor, one lecturer, one project professor, and one senior fellow (joint appointments included, as of Mar 2024). Its goal is to enable the design of integrated circuits with both high energy efficiency and high design efficiency.

In August 2022, NEC Corporation, the University of Tokyo, and Canon Inc. were selected to undertake the research and development of versatile high-level synthesis technology and novel, general-purpose, data-flow computing mechanism by the New Energy and Industrial Technology Development Organization (NEDO) under its Project for Innovative AI Chip and Next-Generation Computing Technology Development, R&D Area 4: Technology Development to Accelerate Industrial Application of AI Edge Computing. The research is scheduled to be completed by Mar 31, 2025.

In addition to its research effort, the Advanced Design Research Division has two organizational responsibilities. First, it operates the d.lab Partnership Program with help from other d.lab divisions. Second, it operates the Research Association for Advanced Systems. The following section is the FY2023 report on these two operations.

2.1.2 d.lab Partnership Program Activities

The d.lab Partnership Program was launched in FY2020 to establish an international center of knowledge-value where system designers and members of the semiconductor industry meet to exchange information and ideas and to engage in open discussion of collaboration between academia and society. The Program aims to create a hub that brings together ideas from system designers in industries including IoT, AI, 5G, automated driving/control, and healthcare, advanced semiconductor technologies such as advanced CMOS processes and 3D integration technologies, as well as enablers of such technologies including materials and manufacturing equipment. In FY2023, a total of 51 corporations joined the Program. Table 2.1.1 contains the list of FY2023 corporate members. We would like to thank these members again for their participation.

In FY2023, because of the reclassification in May of COVID-19 into a Class 5 infectious disease that lifted government-imposed restrictions on daily activities, in addition to organizing various seminars in the form of webinars as in previous years, we were able to pursue our original vision of not only sharing the research accomplishment of d.lab, but also hosting multiple in-person events to enable program members to interact with renowned professors and students from the University of Tokyo, with universities and research organizations from around the world, and with other industrial executives and leaders, as well as events to share information and knowledge from international conferences, and to introduce and offer the chance to experience the most advanced technologies from the likes of Samsung Electronics. The remainder of the section summarizes the Partnership Program activities of FY2023. As in previous years, our activities spanned almost the entire year from May 2023 to Mar 2024. Table 2.1.2 summarizes the events and seminars we held in FY2023.

We held our first event of the fiscal year on May 31, 2023, in Ito Hall at the University of Tokyo which featured a Program kickoff Meeting with special presentations followed by a reception. With the start of a new semiconductor era, advanced semiconductors have become a strategic resource for economies of this century that is more important than oil was in the past. As a result, it is attracting a lot of investments and great expectations. With that as the backdrop, the d.lab Partnership Program Kickoff Meeting was honored to have Tetsuro Higashi, Chairman of the Board of Directors of Rapidus Corporation, deliver a special presentation entitled "The Establishment of Rapidus and LSTC for the Sustainable Development of the Most Advanced Semiconductors," where he provided an overview of Rapidus and LSTC and his expectations for the future of Japan's semiconductor industry. It was followed by an introduction to the four major R&D projects underway at d.lab, as well as an overview of the research being pursued by d.lab's faculty

members. The event was held in a hybrid format, accommodating both online and in-person participation at Ito Hall. After the meeting, in-person participants joined a reception for networking and idea exchange.

On Jun 28, we hosted a seminar to report on the 2023 IEEE 73rd Electronic Components and Technology Conference (ECTC2023). The conference is organized by the IEEE Electronics Packaging Society to provide a forum for wide-ranging discussions of the science and technology of packages, components, and microelectronics systems. It is one of the world's long-established and foremost international conferences, held for the 73rd time last year. It was held in Orlando, Florida, USA. The technology program covered the latest achievements in development and innovative technologies from across the full spectrum of packaging technology. Its main topics included chiplets, hybrid bonding, modeling and simulation, interconnection, material and process, reliability, and manufacturing technology. In our report, we focused on the latest trends and topics in advanced packaging technology and next-generation core technology.

On Jul 12, we held another seminar to report on the 2023 VLSI Symposium on Technology & Circuits, which took place from Jun 11 to 16 in Kyoto, Japan. Since 1987, this has been a premier international conference for the microelectronics industry on state-of-the-art semiconductor device and process technology, as well as semiconductor circuit technology, jointly held by the IEEE Electron Device Society/Solid State Circuits Society and the Japan Society of Applied Physics (sponsored by the Institute of Electronics, Information and Communication Engineers). Its location alternates between Kyoto, Japan, and Honolulu, USA. In 2023 it was held in Kyoto. With "Rebooting Technology and Circuits for a Sustainable Future" as its theme, the program covered the latest technologies in advanced logic CMOS, memory, image sensor, photonics, machine learning, AI, digital, communication, and analog. We focused our report on the technology trends and topics in the areas of circuit/communications system, AI/machine learning, advanced CMOS, advanced memory, and process technology for 3D integration.

On Sep 5, we welcomed Samsung Electronics, which is expanding its R&D activities in Japan, to Takeda Hall for a series of presentations. Executives from the company headquarters and its Japan research center presented on the company's foundry business strategy, advanced packaging technology, and semiconductor equipment of the future, as well as its R&D strategy in Japan.

On Sep 25 and 26, the d.lab Partnership Program organized its first two-day, one-night field trip. The destination was the island of Kyushu, which is attracting the most attention in the revival of Japan's semiconductor industry today. We started Day 1 with a visit to Tokyo Electron Kyushu, Ogic Technologies, and Rorze Corporation. That was followed by a technical exchange meeting with members of the Kumamoto 3D Consortium, where seminars and poster sessions stimulated in-depth discussions. The night was spent in Kumamoto City. The following day, we traveled by bus to Itoshima City, Fukuoka Prefecture, to visit the 3D Semiconductor Research Center. In addition to touring the facility, we listened to presentations on the research accomplishments of the Center. We would like to thank everyone from the prefectural office who provided consultation starting from the planning stage of the trip, as well as everyone who welcomed us to their organizations during this tour. Thanks to them we were able to feel firsthand the passion and commitment of the people of Kumamoto and Fukuoka to semiconductors in these two days.

On Oct 25, we held a seminar entitled "The Latest Devices and Processes Enabling AI and Logic LSI" where we introduced the latest technologies and explored the possibilities they enable. First, Associate Professor Kobayashi of d.lab presented nanosheet FET which is expected to replace FinFET starting with the 2nm generation. That was followed by an introduction to nanobridge technology by Mr. Tada of NanoBridge Semiconductor, Inc., which enables post-fabrication circuits reconfiguration by embedding ultra-small switches within the multiple wiring layers of logic LSI chips. The final presentation was delivered by Mr. Aiko on the cuLitho technology from nVidia that is expected to both reduce power consumption and shorten turnaround time of photomask patterning, which is one of the bottlenecks in semiconductor development today.

On Nov 24, we held a technical exchange meeting for our corporate members in Takeda Hall of Takeda Building at the University of Tokyo. Presentations by nine of our corporate members were followed by a poster session in the foyer participated by eleven member companies.

The event was marked by a lively atmosphere with our members not only networking with each other but also engaging in discussions with our faculty members and students.

On Dec 13, we held a seminar focused on materials. We are in an era of fierce competition around the world to develop semiconductor-related technologies. Various proposals are being put forth to deliver system performance, including chiplet and 3D IC, which create diverse requirements for semiconductor materials. In addition, there are demands to shorten the development cycle all the way to productization. The seminar started with a presentation by Mr. Tamura from the Data-driven Algorithm Team of the National Institute for Materials Science on the innovative approach to materials exploration that is based on automated materials development and testing using materials informatics. It was followed by a discussion of the latest trends in semiconductor packaging delivered by Mr. Ozaki of Namics Corporation, who is serving as vice-chairman of the JEITA Jisso Technology Roadmap Advisory Committee, as well as chief of WG1 and deputy chief of WG3. The seminar ended with an introduction by Professor Mita of d.lab to the University of Tokyo's super-clean room that can be used to confirm the suitability of materials developed through such R&D efforts.

At the beginning of the year on Jan 19, 2024, we held a seminar to report on IEDM2023. IEDM (International Electron Devices Meeting) is the world's top international conference on device technology organized by IEEE. The conference was held in a hybrid format – allowing both in-person and on-demand participation – from Dec 3 to 7. In our meeting, faculty members from d.lab provided an overview of the conference and discussed the latest trends in device technology, focusing on advanced CMOS device technology and materials, non-volatile memory technology, computing technology, and 3D integration and implementation technology.

We ended our FY2023 seminar series with a meeting on Mar 18, 2024, to report on the 2024 International Solid-State Circuits Conference (ISSCC2024). The conference was held from Feb 18 to 22 in San Francisco, USA. The papers presented this year had to go through an especially competitive selection process. Our faculty members presented an overview of the conference and summarized the keynote presentations as well as presentations in the areas of imaging devices, memory, machine learning, RF, wireless, data converters, digital architecture, digital circuits, power management/analog, wireline, and technology directions.

In FY2023, to meet the needs of the times in the post-COVID era, we organized a mix of remote seminars that offer convenience to participants and in-person events that promote deeper exchange and relationship building. We were able to incorporate entirely new activities like the two-day field trip to tour the Kyushu area. In FY2024, we plan to continue to organize events to promote active intellectual exchange between our Program members and the university community, as well as exchange among our Program members.

2.1.3 Research Association for Advanced Systems Activities

The Research Association for Advanced Systems (RaaS) was established on Aug 17, 2020. The goal of RaaS is to increase 10-fold the development efficiency of specialized chips, which are indispensable in a data-driven society, by constructing a design platform for such chips and by adopting an open architecture for hardware design. In addition, RaaS aims to increase 10-fold energy efficiency by researching and developing 3D integration technology and by stacking multiple chips manufactured in the latest 7nm CMOS technology in a single package.

RaaS believes that the driver of the semiconductor industry is once again swinging back from general-purpose to specialized chips, against the backdrop of the unique energy crisis of the data society. The crisis is being spurred by the exponential growth in data and the increasing sophistication of AI processing. On the current trajectory, IT equipment alone is expected to consume close to twice the total available power of today by 2030, and about 200 times the total available power of today by 2050. It will be impossible to realize a sustainable future if digital transformation consumes so much energy as to destroy the earth's environment.

Under such a condition, only those who can improve energy efficiency 10-fold can afford to increase computer performance 10-fold, or extend smartphone use 10-fold. Compared to general-purpose chips which are required to handle all tasks, specialized chips achieve orders-of-magnitude improvement in energy efficiency by eliminating

unneeded circuits. That is why specialized chips are in demand. In addition, since AI processing utilizes neural networks which process data in parallel, it is difficult for von Neumann architecture designed for sequential processing to deliver adequate performance. As a result, specialized chips are being developed around the world to serve as AI accelerators. Furthermore, the slowing of Moore's Law is providing additional tailwind for specialized chips.

Unfortunately, specialized chips development requires special skills and cannot be easily undertaken by everyone. The latest chips integrate more transistors than there are people in the world. Development costs have skyrocketed in recent years to approach $100 million. It will take even a team of several hundred designers several years to develop a specialized chip, which makes it difficult to keep pace with today's rapid technological advance.

In software development, bugs can be patched after the fact. But hardware cannot be shipped unless it is completely error-free. Compared to software, hardware development is indeed hard and carries more risk.

If technologies similar to compilers used in software development are available to chip development, in other words, if silicon compilers become a reality, we can expect both hardware development cost and risk to drop. In addition, more people can become hardware designers. Eventually, as the open-source culture takes root in hardware development and the supporting ecosystem expands and develops into a multi-layer network, mass collaboration will become possible. When that happens, one will be able to develop chips like writing software.

Alan Kay once said that "People who are really serious about software should make their own hardware." Indeed, system development requires both hardware and software development.

Our goal at RaaS is to democratize access to silicon technology. We aim to create a development platform to realize agile authentic prototyping where prototypes can be created rapidly by innovating silicon compiler technology to enable designing chips like writing software.

Our technology goal is a 10-fold increase in both development efficiency and energy efficiency. We plan to improve development efficiency by creating an agile design platform and adopting an open architecture. In addition, we aim to increase energy efficiency through manufacturing chips in the most advanced CMOS process and implementation of 3D integration.

We provide semiconductors as a service, rather than sell them as a product. It is the role of RaaS to develop the necessary technologies to achieve that goal.

In FY2021, RaaS applied to and was accepted by the "Project for Research and Development of Enhanced Infrastructures for Post 5G Information and Communications Systems / Development of Advanced Semiconductor Manufacturing Technology (b) Development of Advanced Semiconductor Backend Processing Technology (More than Moore)" of the New Energy and Industrial Technology Development Organization (NEDO). The development theme is "(b2) Implementation Technology for Edge Computing."

In system R&D, we welcomed new members Advantest and Riken in FY2023 and commenced research under a new 3-year plan with new objectives. In technology R&D, based on the NEDO project mentioned above, RaaS focused its efforts on the establishment and implementation of technology for WoW (wafer-on-wafer) and CoW (chip-on-wafer) integration using Cu-Cu low temperature bonding as part of its direct bonding 3D integration technology development (equipment and process development for WoW and CoW).

Table 2.1.1 List of FY2023 d.lab Partnership Program Members (in Japanese phonetic order)

Aoha, Inc.
Asahi Kasei Microdevices Corporation
ADEKA Corporation
ADVANTEST CORPORATION (RaaS)
Analog Devices KK
Ushio Inc.
ORGANO CORPORATION
KIOXIA Corporation
Kobe Steel, Ltd.
Kobelco Research Institute, Inc.
Foundation for Promotion of Material Science and Technology of Japan
Samsung R&D Institute Japan
Siemens Electronic Design Automation Japan K.K.
JSR Corporation
JCU Corporation
Shin-Etsu Chemical Co., Ltd.
SCREEN Holdings Co., Ltd. (Raas)
Sumitomo Corporation
Socionext Inc.
Sony Corporation
Daikin Industries, Ltd. (RaaS)
Dai Nippon Printing Co., Ltd.
DISCO Inc.
DIPSOL CHEMICALS Co., Ltd.
Tokyo Electron Ltd.
TOKYO OHKA KOGYO CO., LTD.
Toyobo CO., LTD.
TORAY INDUSTRIES, INC.
Toppan Printing CO., LTD. (RaaS)
Nagase & Co., Ltd
NIKON CORPORATION
IBM Japan, Ltd.
Cadence Design Systems, Japan
Nihon Synopsys G.K.
JEOL Ltd.
NEXTY Electronics
Panasonic Industry Co., Ltd.
Panasonic Connect Co., Ltd. (RaaS)
Semiconductor Energy Laboratory Co., Ltd.
Hitachi, Ltd. (RaaS)
Fujitsu Ltd.
FUJIFILM Corporation (RaaS)
Micron Memory Japan, G.K.
Mitsubishi Chemical Corporation
Mitsubishi Electric Corporation
MIRISE Technologies Corporation (RaaS)
Murata Manufacturing Co., Ltd.
RIKEN (RaaS)
Renesas Electronics Corporation
Resonac Corporation
ROHM Co., Ltd.

Table 2.1.2 List of FY2023 d.lab Partnership Program Seminars

Date	Title	Presenter(s)
5/31/2023	FY2023 d.lab Partnership Program Kickoff with Special Presentations	Tetsuro Higashi, Chairman of the Board, Rapidus Corporation Tadahiro Kuroda, Professor, d.lab Masaaki Niwa, Senior Fellow, d.lab Kazutoshi Wakabayashi, Senior Fellow, d.lab Tohru Mogami, Project Researcher, d.lab Makoto Ikeda, Professor, d.lab Yoshio Mita, Professor, d.lab Masaharu Kobayashi, Associate Professor, d.lab Tetsuya Iizuka, Associate Professor, d.lab Atsutake Kosuge, Lecturer, d.lab
6/28/2023	ECTC 2023 Report	Masaya Kawano, Project Researcher, d.lab Takeshi Takagi, Principal Researcher, d.lab Kazunori Yamamoto, Project Researcher, d.lab Katsuya Kikuchi, Research Group Leader, 3D Integration System Group, AIST
7/12/2023	2023 VLSI Symposium Report	Mototsugu Hamada, Project Professor, d.lab Atsutake Kosuge, Lecturer, d.lab Toshiro Hiramoto, Professor, d.lab Shinichi Takagi, Professor, d.lab Masaharu Kobayashi, Associate Professor, d.lab Masaaki Niwa, Senior Fellow, d.lab
9/5/2023	Samsung Day	Kim Seonsik, EVP at HQ & University Relations Center (URC), Samsung Electronics Jeong Gibong, EVP, Samsung Foundry Park Cheolmin, VP, Advanced Package (AVP) Songyun Kang, Master at Mechatronics Research Hiroichi Kawahira, R&D Center Chief, Samsung Device Solutions R&D Japan, & SVP, Samsung Japan
9/25-26/2023	Kyushu Tour	Tokyo Electron Kyushu Ogic Technologies Rorze Corporation Kumamoto 3D Consortium 3D Semiconductor Research Center
10/25/2023	The Latest Devices and Processes Enabling AI and Logic LSI	Tohru Mogami, Project Researcher, d.lab Masaharu Kobayashi, Associate Professor, d.lab Munehiro Tada, VP, NanoBridge Semiconductor, Inc. Hiroshi Aiko, Marketing Manager, nVidia
11/24/2023	d.lab Partners Technical Exchange	Kobe Steel, Ltd. Mitsubishi Chemical Corporation Kobelco Research Institute, Inc. JSR Corporation Socionext Inc. Renesas Electronics Corporation IBM Japan, Ltd. KIOXIA Corporation Murata Manufacturing Co., Ltd. Cadence Design Systems, Japan Nihon Synopsys G.K. ADEKA Corporation Siemens Electronic Design Automation Japan K.K.

Date	Title	Presenter(s)
12/23/2023	d.lab Materials Seminar	Kazunori Yamamoto, Project Researcher, d.lab Ryo Tamura, Leader, Data-driven Algorithm Team, National Institute for Materials Science Yuji Ozaki, Vice-Chairman, JEITA Jisso Technology Roadmap Advisory Committee, Chief of WG1, Deputy Chief of WG3, Manager, Namics Corporation Yoshio Mita, Professor, d.lab
1/19/2024	IEDM2023 Report	Toshiro Hiramoto, Professor, d.lab Shinichi Takagi, Professor, d.lab Masaharu Kobayashi, Associate Professor, d.lab Ken Takeuchi, Professor, d.lab Takeshi Takagi, Principal Researcher, d.lab
3/18/2024	ISSCC2024 Report	Makoto Ikeda, Professor, d.lab Ken Takeuchi, Professor, d.lab Tetsuya Iizuka, Associate Professor, d.lab Mototsugu Hamada, Project Professor, d.lab Atsutake Kosuge, Lecturer, d.lab

2.2 Advanced Device Research Division

Advanced Device Research Division is working for the development of three-dimensional (3D) integration technology and advanced device technology aiming at ten times higher energy efficiency of semiconductor systems in the data-driven systems.

In computing technologies such as AI, which require large amounts of data processing, energy consumption associated with large and frequent data transfers between memory and processors has become a major issue. As a technology to solve such problems, we are focusing on direct bonding 3D stacking technology that forms direct bonds at the chip level or wafer level, shortens the distance of data movement, and improves energy efficiency.

In the NEDO project "Post 5G information communication system infrastructure strengthening research and development project / development of advanced semiconductor manufacturing technology (subsidy)" adopted in 2021, The Research Association for Advanced Systems (RaaS), a technology research association on 3D integration technology operated by d.lab as the headquarters, is working with member companies of RaaS on the theme of "Development of direct bonding 3D lamination technology (equipment and process development for WoW and CoW)". This project aims to develop and implement key point technology related to WoW (Wafer on Wafer) bonding technology and CoW (Chip on Wafer) bonding technology by low-temperature hybrid bonding of Cu-Cu.

This year is the third year of the project, and the main equipment has been built up and basic performance has been confirmed. In addition, basic characteristics were demonstrated in the development of elemental technology and the intermediate targets were achieved. RaaS passed the stage gate examination conducted in January 2024, and is accelerating research and development toward achieving the final goal in June 2026.

In addition, in collaboration with the Institute of Industrial Science and the Department of Materials Engineering, we proposed a new proposal to JST ALCA-Next titled "Development of 3DIC heat dissipation technology based on phonon engineering," which was adopted. We plan to research and demonstrate 3DIC heat dissipation technology during the small phase leading up to the stage gate scheduled for the end of 2026.

2.3 Platform Design Research Division (VDEC Function) FY 2023 Report and FY 2024 plan

2.3.1 Overview of Platform Design Research Division

Since its establishment in 1996, the VLSI Design and Education Center (VDEC) at the University of Tokyo has been developing projects that contribute to integrated circuit design education at universities and technical colleges in Japan, based on the three major roles: ”spreading the latest information on VLSI design and education,” ”providing licenses of CAD tools,” and ”supporting on VLSI chip fabrications for academic use.” On October 1, 2019, VDEC has been re-organized into Systems Design Lab (d.lab), Graduate School of Engineering, the University of Tokyo as part of an organizational restructuring aimed at strengthening integrated circuit related activities in the University of Tokyo's semiconductor integrated circuit-related activities. The Platform Design Research Division of d.lab continues to carry out the functions of the VDEC and continues “VDEC activities” seamlessly. Here, the outline of “VDEC activities” of the FY2023 is reported below.

The missions of VDEC are for advancement of researches and education on LSI design in public and private universities and colleges in Japan and send many distinguished VLSI designers into industry. After 27 years of VDEC establishment, educations on CAD software, LSI design and design flow in universities have been well established. On the other hand, advancement on nano-meter CMOS technologies forces design flow and CAD software complicated. We have been continuing CAD tool seminar by the lecturers from EDA vendors for twice a year. We hold the seminar in VDEC and provide distance learning through video streaming. We expect spread of the up-to-date LSI design methodology by using CAD tools.

In order to make it more convenient for the participants, the seminars have been held only in Tokyo since 2009, and at the same time, the seminars have been broadcasted to individual participating lab. The VDEC expects that the latest CAD use-case will be shared among labs through the seminar organized by VDEC, and will be a trigger to spread the technology nationwide. In FY2022, all seminars will be conducted online. Some items were conducted in the form of on-demand plus live Q&A sessions to improve the convenience of participation. In addition, in view of the current situation where the tool-chains of various companies are becoming more complex and it is difficult to fully use the introduced tools, lectures on the tool-chains recommended by each tool vendor were also held in conjunction with the individual tool seminars. From the end of FY2019, we received permission from each EDA vendor to use EDA tools from home, to avoid delay&slowdown in integrated circuit design research and education in Japan.

2.3.2 Status of Education at Platform Design Research Division

The LSI Design Flow Seminar is designed to educate the basic concepts of LSI design and to provide hands-on experience of practical design examples using multiple CAD tools. For this purpose, VDEC has been organizing LSI design education seminars as well as “Refresh Seminar” for re-education programs for engineers. In FY2022, we have canceled “Refresh Seminar,” but restarted it in FY2023 with help from adjunct professors of VDEC.

In addition to these seminars, VDEC holds the “VDEC Designers’ Forum” once a year, mainly for young faculty members and students. This is a workshop-style meeting, where participants bring their design cases and exchange their successes and failures, in addition to invited lectures from companies and universities. In FY2023, the VDEC Designer Forum had been held in hybrid format at Kawatana Grand Hotel. Since FY2011, the “IEEE SSCS Japan Chapter VDEC Design Award” has been presented as an award for VDEC activities. The final judging and awarding of the “IEEE SSCS Japan Chapter VDEC Design Award” has been held at VDEC Designers’ Forum since 2011, and in 2023, the IEEE SSCS Japan Chapter VDEC Design Award will be presented to Mr. Y. Yamasaki of Tokyo Institute of Technology. Four VDEC Design Award Excellence Awards, (Mr. Y. Yamazaki (Tokyo Institute of Technology), Mr. Y. Nakanishi (Nara Institute of Science and Technology), Mr. Li Shuowei (University of Tokyo), and Ms. Y. Shishido (Kyushu

Institute of Technology)) and two VDEC Design Award Encouragement Prizes (Mr. R. Okada (Nara Institute of Science and Technology), Ms. A. Otani (Ritsumeikan University)), and two VDEC Design Award Commendation Prizes for Idea Contest (Mr. A. Roberto (Yamagata University) and Mr. R. Hotta (Ritsumeikan University)). This year, we also recognize three as the finalist of VDEC Design Award (Mr. S. Tanabe (Shizuoka University), Mr. K. Tatsuta (Ritsumeikan University), and Mr. H. Zhang (University of Tokyo)).

Although the educational system through such seminars and forums has enabled students to learn the basics of LSI design, they still face various difficulties in actual LSI design situations. For beginners, setting up the CAD software is the biggest problem. Even after setting up the software, they are often baffled by the "difficult error messages" issued by the CAD software. VDEC users can register for the "CAD mail group" and the "Prototyping Technology User Group" on the VDEC website, where they can post their questions and ask for help. The registered users of the mail groups are not obligated to respond, but in most cases they can get help from experienced users within a few hours or days. We hope that you will take advantage of this system to help solve your problems.

2.3.3 Publications related to Platform Design Research Division

Figure 2.3.1 shows the use of the VDEC facility in the published literature related to VDEC. It can be confirmed that CAD software is widely used in writing papers. Since CAD software is often used not only in chip design but also in the preparation stage of chip prototyping, its contribution as a tool to demonstrate the basic idea of the research is also significant.

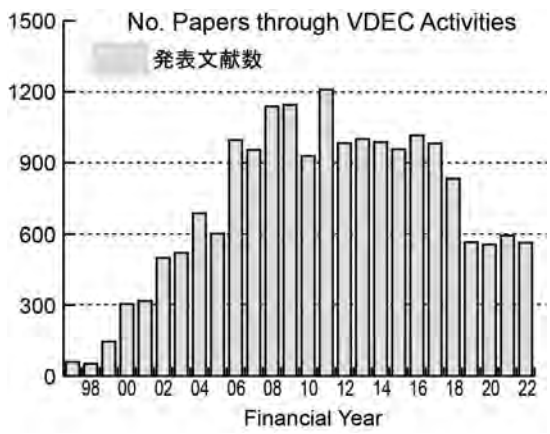


Fig. 2.3.1 Trends of number of papers through VDEC activities.

2.3.4 Report on AI Chip Design Center

VDEC and the AIST have been jointly commissioned by NEDO to develop a common platform technology for accelerating AI chip development under the "Innovation Promotion Project for Accelerating AI Chip Development / R&D Item 2: Development of Common Platform Technology for Accelerating AI Chip Development" since 2018. In this project, we have established an EDA utilization and design environment for venture companies and small and medium-sized enterprises(SMEs) in Japan, and are working as an "AI chip design center(AIDC)". In this activity, in addition to the introduction of EDA tool licenses that allow venture companies and small and medium-sized companies to prototype up to engineering samples, we have introduced IP for 40nm, 28nm, and 12nm, and are also providing a large-scale, high-speed design and verification environment using a hardware emulator, which was introduced with a subsidy from the Ministry of Economy, Trade and Industry at the start of this project. In FY2020, we have designed a SoC platform with NoC, PCIe, DDR4, etc., and multiple functional IP cores, and taped out the platform as a SoC with multiple AI IP cores designed by multiple users, and after almost 1-year delay, we have received assembled chip in

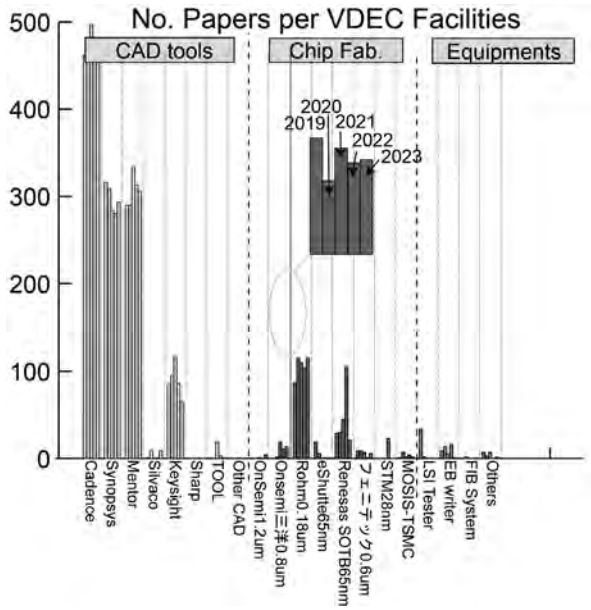


Fig. 2.3.2 Number of papers related to VDEC facilities.

the beginning of Jan. 2022, and after one week we could evaluate most of SoC functionalities and by the end of March 2022, almost all of IPs got fully verified. We have also designed and taped out with 4 AI IP cores in 12nm in June 2022, and all the IP cores have been successfully demonstrated by the end of March 2023. In order to further strengthen this activity, we are accelerating our research by establishing the "AIST-The University of Tokyo AI Chip Design Open Innovation Laboratory" (AIDL) in the Takeda Building, Asano Campus, The University of Tokyo on September 1, 2019.

2.3.5 Plan for FY 2024 "VDEC Activities" of Platform Design Research Division

In FY2024, we will continue the VDEC Activities for academics as before.

【Design related information dispatching/Seminar】

We will continue holding the following seminars: (1) CAD tools seminars which have been continued since 1997, (2) "Refresh seminar" since 1998, (3) "Designer' Forum" since 1997. We will also continue seminars for LSI tester usage at VDEC and sub-centers, workshops on LSI testing technologies initiated by D2T.

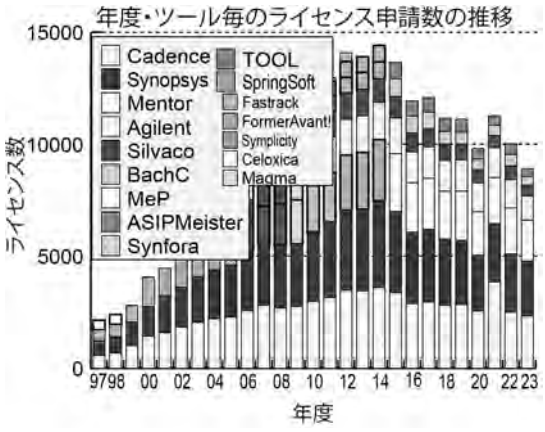
【CAD tool support】

We will continue Cadence tools, Synopsys tools and Mentor tools as the main stream design tools. We will continue analog ADS/EMPro/GoldenGate by Agilent, C-based design environment, BachC by Sharp. In addition, we continue trial of several CAD tools, such as layout platform, Lavis by TOOL. Design debugging platform from SpringSoft has merged into Cadence tools and will be continued.

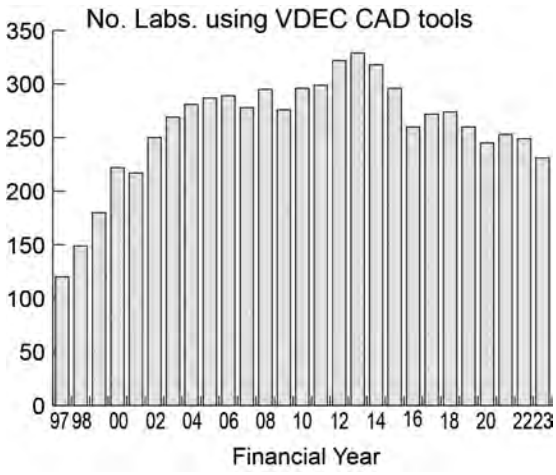
【Chip fabrication services】

We will continue chip fabrication services for 0.18μm CMOS by Rohm, 0.8μm CMOS by JS Foundry (former On-semiconductor-Sanyo/Motorola Japan), and IHP SiGeBiCMOS 0.18um as the regular services.

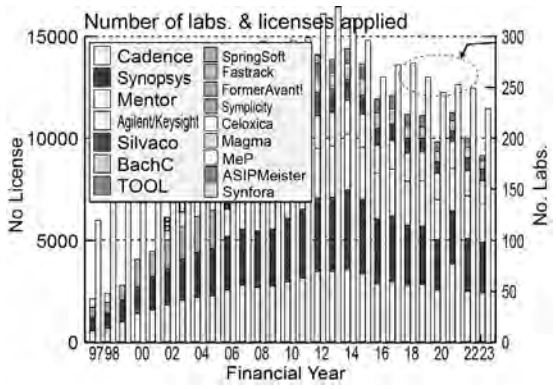
In addition to the above. We will continue to develop an "AIDC" activities, in collaboration with AIST. We will introduce a logic emulator for large-scale AI digital chip design verification, and maintain and operate EDA licenses for industrial applications. The main objective of this project is to provide small and medium-sized venture companies with a development environment for AI chip design, evaluation, and verification in order to accelerate the development of AI chips, but we also plan to improve the environment for use by universities in order to promote university-originated companies in the field of AI-related integrated circuits.



CADUserLicense



CADUser



CADLicense

Table 2.3.1 Chip fabrication schedule

【CMOS 1.2μm 2P2M】 JS Foundry (Former On-Semiconductor/Motorola Japan)

	Chip application deadline	Design deadline	Chip delivery
2024#1	2024/7/16	2024/9/24	2024/12/16
2024#2	2025/1/6	2025/3/24	2025/6/23

【CMOS 0.18μm 1P5M(+MiM)】 Rohm

	Chip application deadline	Design deadline	Chip delivery
2024 #1	2024/4/1	2024/6/24	2024/10/9
2024 #2	2024/6/10	2024/9/2	2024/12/14
2024 #3	2024/7/29	2024/10/21	2025/2/18
2024 #4	2024/11/14	2025/2/3	2025/5/16

2.4 Platform Device Research Division

2.4.1 Mission

D.lab platform device research division aims at providing every researcher with three essential elements for research on new devices. The division is with around 30 staffs, empowered by Professor Yoshio Mita, the playing division director who himself actively performs experiments in the Cleanroom as a leading researcher, and operated in collaboration with related departments (such as Institute of Engineering Innovation, Electrical Engineering and Information Systems, and Mechanical Engineering) in terms of human and budget resources. Research in emerging fields of semiconductor electronics devices (such as integrated circuits), sensors and microsystems requires three essential elements: (1) fabrication machines with stupendous amount of budget, (2) rich accumulation of fabrication technology knowledges, and (3) research capability to develop new technologies required for new devices. In Japan, these three elements had been prepared and kept in an individual research group until the end of 20th century. However, due to the technology trends towards advanced fabrication over larger-scale wafers, it has become almost impossible for a research group to purchase and maintain the cutting-edge fabrication machine line, in the 21st century. Originally, it was impossible for every research group in universities, companies, research institutes, and NPOs, to exclusively "own" such large-scale facility and necessary budget by themselves; If researchers wish to "cooperate" with the other researchers in a platform, which is equally open to everybody, they can "effectively own" the most advanced "open platform", and thereby the cutting-edge research activities can be held anywhere in Japan. This is the principle of d.lab's open device platform, which is in fact a lateral expansion of "shared economy model in VLSI design and fabrication" to micro-nano fabrication and measurement research field, originally established by VDEC for Japan in 1996.

Towards that end, d.lab Platform Device Research Division takes full advantages of spaces (of its own and of open rental) in Takeda Sentanchi Building. The building was inaugurated on 17th December 2003, thanks to the enormous donation in 2001 from Mr. Ikuo Takeda (founder of Advantest) to the faculty of engineering (Dean was Professor Hiroshi Komiyama) as well as VDEC (director was Professor Kunihiro Asada). In the building, a 600m^2-square supercleanroom including "official ISO3 (a.k.a. federal class 1. Once measured as ISO1)" area (Fig.1). The cleanroom and affiliated experimental rooms are equipped with cutting-edge nanofabrication and measurement machines, total valued over 5.0 billion yens (32M euros, due to low JPY ratio). The users can openly use such nice machines really inexpensively.

Fig.1 Development of Takeda Sentanchi Supercleanroom

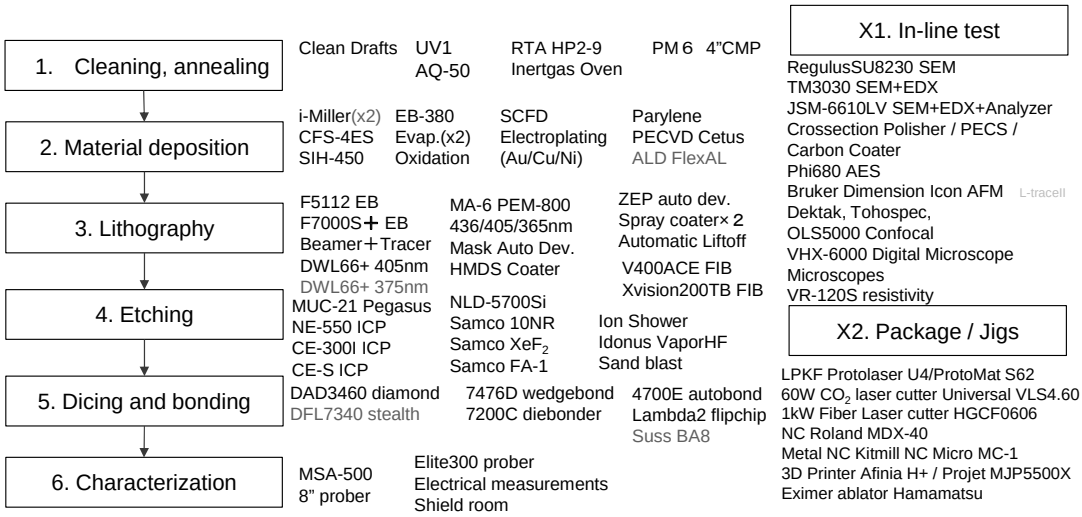


Fig.2 List of equipment under d.lab Platform Device Research Division

Over 100 apparatuses are openly accessible (Fig.2), including, "world's fastest" large-area direct electron beam (EB) writing machine Advantest F5112+VD01, which has been donated according to the wise decision of Mr Ooura, a chairman of Advantest, fine EB writer Advantest F7000S-VD02 and Silicon Deep Reactive Ion Etching machine SPTS MUC-21 ASE-Pegasus, both purchased by Japanese government's supplemental budget (known as Abenomics, the first arrow), and the scanning electron microscope (SEM) Hitachi Regulus SU8230 that provides highest-class resolution among those obtainable by research laboratory. The machines can cover most of the research steps in nanotechnology, which are cleaning, film deposition, lithography, etching, packaging and characterization. Not all apparatuses are yet installed in Takeda Building, however due to nationwide platform network, researchers can access in another equivalent nanofabrication platform center(s).

2.4.2 "Takeda Sentanchi Supercleanroom" cooperation platform

The platform is called "Advanced Research Infrastructure on Materials (ARIM) UTokyo Nanofabrication site" according to the MEXT's national project, or simply "Takeda Sentanchi Cleanroom" (in short, Takeda CR). The platform is widely open to those who share the "value of cooperation". The most important understanding for every user is the platform must not be considered as a simple outsourcing agent; being understood the value of "own help, mutual help, and public help", the participant can drastically minimize costs (personnel, budget, and time), which should have otherwise been totally covered by each researcher, and can directly jump into advanced research. Key Performance Indicators of such benefits are as follows: over 9.0 billion yens for installation cost of building and equipment, over 350 million yens for yearly operating cost, and reduction of over 20 years' leading time to acquire know-hows in advanced fabrications. These benefits have attracted many research groups. Since ten years, the number of research groups who sent us the letter of consensus exceeded 780. Over 1128 members are yearly subscribed (including renewal and new subscription).

Operation principle is also "own help, public help, and mutual help". Budgetwise, each term of the principle corresponds to: (1) User's payment to participate budget acquisition (charged according to the officially-approved d.lab's internal rule), and (2) national budget allocated to d.lab platform research division, MEXT Nanotechnology Platform project, and (3) major laboratories (who rent space in Takeda Building for their research work) as well as research projects with d.lab operation laboratories (such as Mita Lab). Of course, each budget category is righteously dispensed in perfectly following its own rule defined by corresponding laws and ordinances. The yearly operation cost of 350 million yens are composed of equipment installation, electricity and water fees, maintenance, and personnel. Recently electricity cost is drastically increasing. National Universities have acquired budget flexibility since the date of private agency statuses. It helps a lot to

ensure staff employment as well as small to middle sized equipment acquisition.

Platform Device Research Division staffs acquire implicit information for future fabrication technologies, due to daily help to massively parallel research projects. The team develops technologies with high demand and universality and make them accessible by publishing papers.

Moreover, taking full advantage that PDRD is a division of d.lab, the team has been developed for over 10 year, a reliable research scheme for integration of LSI and MEMS devices, known as "Integrated MEMS research domain". As summarized in a peer-reviewed journal [1], through VDEC function of d.lab "LSI foundry", a specific LSI circuit silicon wafers are fabricated through company (such as Phenitec Semiconductor). Then the wafer is "post"-processed in an open nanofabrication platform including Takeda Sentanchi Supercleanroom. The critical advantage of such scheme is that researchers can "easily" obtain silicon wafers with transistor circuits, which has been really difficult for university cleanrooms to acquire reliability, and can fabricate by themselves specific MEMS that no foundry company can provide. Namely, researchers can produce "World's first functionality" with "World's highest quality". Such a flexible scheme is unique in the world. Yearly one multi-chip fabrication is performed (pre-fixed participants upon request), including collaborative research works with industries.

[2] Y. Mita *et al.*, *Japanese Journal of Applied Physics*, **56**, p. 06GA03, 2017 (2017) DOI: 10.7567/JJAP.56.06GA03

2.4.3 Activity Report 2023 of Platform Device Research Division

【KPI】In FY2023, we had 195 active research groups, composed by company:external:UTokyo external:UTokyo Eng.dept = 1:1:1:1, with 1128 subscribers.

For 43 top-used machines, 47% of usage rate (4422 days for 9404 available machine days) and 67.6% of external use rate (2990 days for 4422 used days) have been obtained. This record highly oversatisfy the requirement of National ARIM project (30% external use), underlining that our site is "one of the most democratic open platforms in the world".

【Anniversary】"20th anniversary of Takeda Building" was held on 20th December 2023 [3](Fig.3). Celebration speeches included Professor Teruo Fujii (president of UTokyo), Professor Yasuhiro Kato (dean of faculty of engineering), MEXT, METI, and Advantest Corporation. Resent activities were reported from platform design research division, advantest D2T endowment division, and platform device research division, SONY semiconductor solutions as a plenary talk, and two outstanding use award winners' presentations (from Innovastella and Professor Tetsuo Kan of UEC). Participants celebrated the anniversary with research poster session from participating laboratories, and the day was concluded by special lecture from Professor emeritus Hiroshi Komiyama, president of Mitsubishi Research Institute, "20 years with the country with advanced issues"

[3] https://www.if.t.u-tokyo.ac.jp/~mita/Takeda-Anniversary2023.pdf

Fig.3 Professor Hiroshi Komiyama (right) celebrating 20th anniversary with Professor Yoshio Mita (left), head of Platform Device Research Division of d.lab.

【High-level engineering exchange with worldwide Nanotech Platforms】Such cleanroom platform as an open innovation base has been widely established, such as National Nanotechnology Coordinated Infrastructure in the USA, RTB-RENATECH operated by French National Research Center (CNRS), Australian AIFF network. Our PDR division has especially close collaboration relationship with RENATECH, and its European extension called EuroNanoLab, due to Pr Mita's 25 years' network. Two engineers (Hugues Granier and David Bourrier) from LAAS laboratory that is one of the five "big" core facilities in France were invited to d.lab at the end of FY2022. They worked for common interest in eletroplating. The engineering research knowledges were then submitted to the European National Research Infrastracture Symposium (ENRIS). Eight out of eight presentations have been accepted, and the engineers as well as professors of the team has been sent to C2N laboratory (Paris-Saclay). In total, 24 open facilities presented their cleanroom KPIs in terms of posters. Comparison was made in an efficient way (Fig.4). The benchmarking has revealed that standard cleanroom size exceeds 1000 meter squares (UTokyo Takeda has only 600 meter squares), many cleanrooms have bigger amount of budgets (UTokyo has got 8th place), but the number of users, 1100, is an outstanding number. As a post-conference activity, the team has visited several research institutes such as CNAM (Paris, France), IEMN (Lille, France), LAAS (Toulouse, France), KU Leuven and IMEC (Belgium).

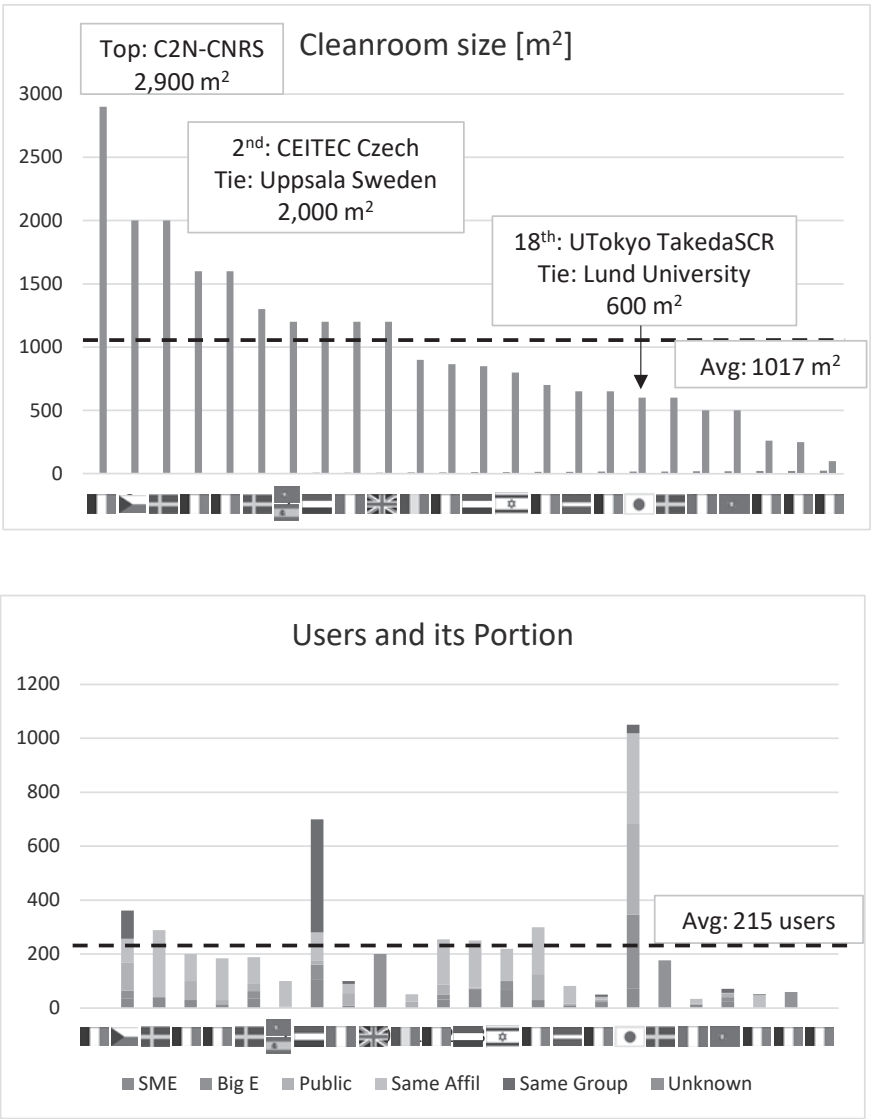


Fig.4 Takeda SCR is categorized as "small" platform nowadays (top), however the number of users is remarkably big (bottom)

2.5 Activity Report of ADVANTEST D2T Research Department

2.5.1 Introduction of ADVANTEST D2T Research Department

2.5.1.1 Aim of establishing ADVANTEST D2T Department (former D2T research division)

ADVANTEST D2T research division was established in VDEC in October 2007. As the name suggests, it is financially supported by ADVANTEST Corporation.

The aim of establishing ADVANTEST D2T research division was to promote the research and education environment with regard to VLSI testing in all universities and colleges in Japan. “D2T” signifies that we consider not only design but also testing. Through our activities, we hope to provide expertise in design and testing for the industry. In addition, we are exchanging researchers with those of other universities and research institutes both in Japan and overseas. Moreover, D2T research division is suitable for collaborations with the industry because VLSI testing is one of the most practical research topics in the industry. On the basis of these activities, our final goal is to become a center of excellence of VLSI testing in Japan.

D2T research division has spent a total of 15 years to develop the first (Oct. 2007 – Sep. 2010), second (Oct. 2010 – Sep. 2013), third (Oct. 2013 – Sep. 2016), fourth (Oct. 2016 – Sep. 2019) and fifth (Oct. 2019 – Sep. 2022), phases. D2T activity report of 2022 presents the 1st financial year, i.e., Oct. 2022 – Sep. 2023, of the sixth phase. Systems Design Center, School of Engineering, the University of Tokyo has been established in Oct. 2019, and Advantest D2T research department is within the center. D2T research department primarily focuses on D2T research activities and education. The sixth project phase (Oct. 2022 onwards) of D2T project was commenced by courtesy of ADVANTEST Corporation. The details pertaining to the activities of our group are presented in the following sections.

2.5.1.2 Members of ADVANTEST D2T Division

Project Professor	Makoto Ikeda
Postdoctoral research fellow	Zolboo Byambadorj
Project Lecturer	Akio Higo
Researcher	Koji Asami (Advantest Laboratories Ltd.)
Researcher	Masahiro Ishida (Advantest Corporation)
Researcher	Takahiro Yamaguchi
Assistant Clerk	Makiko Okazaki

2.5.2 Report of the 17th D2T Symposium

The 18th D2T Symposium was held on September 8, 2023, hybrid. This year, we will invite lecturers overseas, Professor, Zhongrui Wang from Hong Kong University, Reika Ichihara from Institute of Memory Technology R&D, Kioxia Corporation, Associate Professor Shintaro Hisatake from Gifu University, Takahiro Nakamura, Ph.D. from AIO Core Co., Ltd., Dr. Motoaki Hara, Senior researcher from National Institute of Information and Communications Technology（NICT）, Lecturer Atsutake Kosuge from Systems Design Lab. the University of Tokyo, for their distinguished research topics.

We sincerely appreciate each participant for their contributions to the symposium. We look forward to greater participation again at the 19th D2T symposium on Sep. 6 Fri. 2024.

18th D2T Symposium Program ONLINE　September 8, 2023

10:00	**Opening Remarks** Tadahiro Kuroda (Director, d.lab, School of Engineering, the University of Tokyo) **Yoshiaki Yoshida** (President & CEO, ADVANTEST CORPORATION)
10:15	**Session 1** (Chairperson: Makoto Ikeda, d.lab, the University of Tokyo) *Classical Cryo-CMOS Systems for Quantum Computing: from a Wild Idea to Working Silicon* **Edoardo Charbon**, Professor (EPFL) *Digital neuromorphic computing systems featuring dendrite-spines in human cerebrum* **Atsutake Kosuge**, *Lecturer (d.lab, University of Tokyo)*
11:45	**Free coffee and Tea break (KESCO supported)**
14:00 15:30 15:45	**Session 2** (Chairperson: Tetsuya Iizuka, d.lab, the University of Tokyo) *Boosting defect coverage for analog/mixed-signal ICs: machine learning to the rescue* **Georges Gielen**, Professor (KU Leuven) *Algorithm-Centric Design of Reliable and Efficient Deep Learning Processing Systems* **Alex Orailoglu**, Professor (University of California, San Diego) **15min break**
	Session 3 (Chairperson: Masahiro Fujita, the University of Tokyo) *Understanding Circuit Timing Marginalities that Cause Silent Data Corruption Ratio based Resistive Memory Cells for Low Error Rate and High Energy Efficiency* **Adit Singh**, Professor Auburn University *"Design, Architecture and Integration of Next-Generation Edge AI Chips: Challenges and Opportunities"* **K.-T. Tim Cheng**, *Professor U-Tokyo Fellow (Hong Kong University of Science and Technology)* **Session 4** *Recent D2T research department progress* **Akio Higo**, Lecturer (d.lab, the University of Tokyo)
17:30	**Closing Remarks** **Makoto Ikeda** (d.lab, School of Engineering, the University of Tokyo)

2.5.3 Research Activity Reports of the ADVANTEST D2T Research Department

High-Resolution Analog-to-Digital Converter Based on Stochastic Comparators

Takahiro J. Yamaguchi, Akio Higo, Tetsuya Iizuka, Makoto Ikeda

This project aimed to explore new stochastic analog-to-digital converter (ADC) architectures. To reduce randomness and increase accuracy, an approach for robustly detecting level-crossing time via stochastic median is investigated. A new theory for detecting LC-time using N "Comparator with ZERO Process Variability" was developed and verified by Monte Carlo experiments. It was shown, unlike a single comparator (CP), this approach uses *N* ideal CPs in order to detect LC events of an input waveform, it has the accuracy limitation in detecting LC times.

5G multi-channel/millimeter-wave signal measurement

Koji Asami, Zolboo Byambadorj, Ryogo Koike, Sheng Guo, Nguyen Ngoc Mai-Khanh, Akio Higo, Tetsuya Iizuka, Masahiro Fujita, Takashi Matsumoto, Makoto Ikeda

We study and develop fundamental research to measure the millimeter-wave signals in an over-the-air (OTA) environment. A 4-channel planar antenna array has been developed for the near-field measurements of the millimeter-wave antenna. Metasurface was fabricated to reduce the coupling between antennas. Antenna probes were fabricated, and experiments are underway to confirm the characteristics and measure the antennas. In addition, to confirm the measurement algorithm, a commercially available horn antenna was used as a probe to measure antennas for 5G. We confirmed that the far field can be estimated accurately by correcting the influence of the probe from the measured near field.

High-Speed and High-Accuracy Multi-Pin Signal Integrity CAL for ATE

Kazuki Shirahata, Masahiro Ishida, Tetsuya Iizuka, Akio Higo, Toru Nakura, Makoto Ikeda

Automatic test equipment (ATE) for Semiconductors has thousands to tens of thousands of signal input and output channels. It requires signal integrity calibration (CAL) to correspond the test signal outputs to the device under the test (DUT). This research focuses on a high-speed and high-accuracy multi-pin signal integrity CAL method applicable to ATE. This year, we decided research objectives and began investigating the signal integrity CAL method. First, we conduct a preliminary survey for signal integrity CAL, and decided the research target to establish the theory of the signal integrity CAL which includes transmission line characteristics estimation using time domain reflectometry (TDR) measurement and waveform estimation at CAL point with the estimated transmission characteristics. Then we began considering the basic concept of the signal integrity CAL with TDR measurement, and showed that it is possible to calculate transmission characteristics and signal waveform at a CAL point from TDR waveforms for a known transmission line model by using circuit simulations and numerical operations.

Development of Security-aware Test-driven Semiconductor Design

Genichi Tanaka, Kaoru Masada Kotaro Hasegawa, Manabu Kimura, Akio Higo, Makoto Ikeda

We have studied the feasibility of a cryptographic architecture to ensure and guarantee the authenticity and security of semiconductors in the semiconductor test process. The physical layout of the core circuit of the architecture was designed and its feasibility is verified.

Kuroda and Kosuge Lab

(http://www.kuroda.t.u-tokyo.ac.jp/en/index.html)

(https://klab.t.u-tokyo.ac.jp/en/research_theme/)

TCI: ThruChip Interface

T. Kuroda, M. Hamada, A. Kosuge, T. Shidei, M. Okada, Wai-Yeung Yip, Y. Mitarai

TCI is a 3D integration technology that employs inductive coupling between coils created with on-chip metal line patterns for data communication across stacked chips. It realizes the same or better performance as TSV (through-silicon via) but at a lower cost. This year, we presented research papers on TCI-based 3D SRAM stacking technologies and performed related research on architecture and AI processing algorithms, as well as jointly designed with RaaS an SRAM test chip for TCI-based 3D integration. In addition, we developed design and verification methodologies for TCI-based 3D integration. Our research results were published in international academic journals such as JSSC.

TLC: Transmission Line Coupler

T. Kuroda, M. Hamada, A. Kosuge, Y. Hayashi

TLC is a data communication technique between circuit boards which utilizes electromagnetic coupling between transmission lines. It solves issues in conventional connectors such as wear and tear, reliability against vibration, and impedance mismatch and realizes low-cost, high-performance wireless connectors. This year, through joint research with a company, we conducted research and development of compact and high-density TLC mounting technology for connecting package substrates and PCBs, as well as fully sealed, non-contact connector technology for simultaneous wireless power delivery and TLC communication by placing the couplers coaxially and in close proximity to each other.

Ultra Low Power AI Processor

T. Kuroda, M. Hamada, A. Kosuge, R. Sumikawa, K. Kobayashi

We are studying non-von Neumann AI processors that use wired-logic architecture to dramatically reduce power consumption by minimizing access to memory including DRAM and SRAM. However, area efficiency is a bottleneck since it requires the implementation of a large number of elements on a chip. Therefore, we are developing three technologies to boost area efficiency: (1) a technology to optimize neural networks by removing unnecessary neurons and synapses, which is similar to pruning of the human brain, (2) nonlinear neural network technology that incorporates the property of human neurons of using a wide variety of nonlinear functions individually optimized for each neuron to increase the representation capability of the network in order to enable more drastic pruning than ever before, so as to reduce the number of elements, and (3) a convolutional wired-logic architecture that reuses circuits in processing of convolutional algorithms. This year, we studied the fundamental technology for classification of 10 general objects using the CIFAR-10 dataset, developed the training algorithm, proved the concept through FPGA implementation, and published the results in IEEE Micro, an international academic journal. In addition, we developed circuit technology to improve area efficiency and an ASIC to confirm a 2048x power saving in voice commands recognition compared to conventional GPUs, and presented the results at VLSI Symposium 2023 and SSCL. Our research earned high regards, mentions in news releases, and recognition by JST as outstanding research.

Takeuchi Laboratory

(https://co-design.t.u-tokyo.ac.jp/)

Computation in memory (CiM)

Ken Takeuchi and Chihiro Matsui

We have developed a comprehensive Computation-in-Memory (CiM) simulation platform. The simulation platform has capability to emulate multi-level cell (MLC) and various memory device non-idealities such as uniform/non-uniform conductance variation and shift. The simulation results address that the conductance shift has much more critical impact than conductance variation on inference accuracy in CiM.

Simulated Annealing

Ken Takeuchi, Chihiro Matsui and Naoko Misawa

Memory error tolerant ReRAM-based Computation-in-Memory (CiM) to solve the knapsack problem, one of the combinatorial optimization problems, is proposed. Proposed log-encoding simulated annealing (SA) on ReRAM CiM reduces the array area of ReRAM CiM by 97.6%. To co-design ReRAM device and SA, error injection is applied. As a result, the asymmetric ReRAM error increases the acceptable bit-error rate (BER) by 10 times and the acceptable bit precision to 5-bit.

In-sensor Computing

Ken Takeuchi and Chihiro Matsui

We have proposes an integration of event-based vision sensor (EVS) and processor (e.g., computation-in-memory, CiM) for low-power processing. By using newly defined characterization method of frame and EVS camera, an event-driven SRAM CiM with partitioned word-line (WL) activation method is proposed for 3D-integration of EVS. The multiple-bit synaptic weights are stored in a set of SRAMs. The proposed CiM for EVS achieves 10^{-6} times energy efficiency compared with CiM for frame camera.

Nakamura Laboratory

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IoT Network Security

Hiroshi Nakmaura

We considered a method for detecting scanning behavior executed at the early stage of ransomware attacks targeting networks connected by IoT devices through SDN (Software Defined Network). SDN (Software Defined Networking) is an approach to network management where the control of packet forwarding and routing is separated into SDN controllers and SDN switches. One advantage is the ability to flexibly modify settings using software. By making use of this advantage, we created a detection model based on machine learning that utilizes lightweight features derived from statistical information requests from SDN controller to SDN switch during communication, and from flow rules set in the SDN switch.

Coarse-Grain Reconfigurable Architecture

Takuya Kojima, Hiroshi Nakamura

Coarse-grained reconfigurable architectures (CGRAs) are expected as a promising architecture for wide variety of computing including embedded systems and high-performance computing due to its benefit of high-energy efficiency and programmability. CGRA consists of an array of numerous processing element and its efficiency heavily depends on the quality of compiler which maps applications onto these PEs.

To overcome this difficulty, we developed a mapping method dedicated to Elastic CGRA in which PEs exchange data asynchronously using a handshake protocol. Due to the asynchronous communication, complexity of the mapping problem is expected to be reduced.

We developed a new mapping method for Elastic CGRA using ILP (Integer Linear Programming) and confirmed that mapping time is drastically reduced.

Lightweight Runtime Environment of ROS2 nodes for Embedded Devices

Hideki Takase, Hiroshi Nakamura

The Robot Operating System (ROS) and ROS2, the latest version of ROS, have attracted attention as a design platform for distributed robot software development. One of the drawbacks of ROS2 is that it is necessary to employ high-performance and power-hunger devices since it requires a Linux environment for operation. This drawback prevents ROS2 from being applied to embedded devices because they must be quick in response and consumes less power. Thus, we have proposed a novel solution called mROS2, which is a lightweight runtime environment of ROS2 nodes. One of the advantages of mROS2 is that it provides efficient communication mechanisms with less memory consumption. Currently, we are designing software architecture for this communication flow. This work is expected to contribute to the power

saving and real-time performance enhancement of mobile robot systems.

Ikeda Laboratory
(http://www.mos.t.u-tokyo.ac.jp)

Design of Functional Encryption Accelerator and its automated design techniques

M. Ikeda, A. Opasatian, K. Masada, M. Fukuda, and Y. Suzuki

When implementing complex algorithms such as pairing operations, dedicated hardware development using ASICs and FPGAs is expected to achieve lower power consumption and latency by taking advantage of parallelism, compared to software implementation on CPUs. On the other hand, it takes a huge human and time cost to explore suitable architecture and optimize parallel processing in consideration of data dependencies. We have therefore reduced the design time by automating the scheduling creation process. The higher-level synthesis methods by Python using libraries such as NumPy is also investigated to realize more flexible designs.

Implementation of Post-Quantum Cryptography

M. Ikeda, Y. Takeshima, P. Sun, K. Nakamura, and Y. Nakamura

With the advent of practical quantum computing, there is a threat that classical cryptographic methods, such as RSA and elliptic curve cryptography, will be compromised. In response, researchers have developed several Post-Quantum Cryptography (PQC) algorithms, which are resistant to quantum computing. Our team is working on the acceleration through dedicated hardware for key encapsulation mechanisms such as CRYSTALS-Kyber and SIKE, as well as digital signatures like CRYSTALS-Dilithium and SPHINCS+.

For CRYSTALS-Kyber, we have designed hardware capable of supporting multiple security levels through pipelining and parallelization. This design has proven to be superior in terms of the area-delay product when compared to existing hardware. Furthermore, we are researching implementations aimed at hardware integration with CRYSTALS-Dilithium, and have successfully developed a number theoretic transform hardware that can be used in both systems.

In addition to the accelerator used alongside CRYSTALS-Kyber, standalone hardware targeting CRYSTALS-Dilithium for high resource compression and low clock consumption is also in progress. With a focus on extensive resource reuse and maximizing segmented pipelining design, the achievement is poised to reduce clock requirements by over 30% compared to existing solutions, while maintaining nearly unchanged or even better resource consumption and maximum frequency conditions.

For SPHINCS+, we aimed to achieve low latency by designing it with multiple hash processors for efficient computation. We demonstrated that, even in its minimal configuration, the deployed strategy can perform operations faster than other ASIC implementations while maintaining an equivalent area. By adjusting the number of cores, we achieved a further reduction in the area-delay product.

In our research on SIKE, we have reconsidered the computational paths of cryptographic computations with the goal of designing dedicated hardware. We designed a general-purpose hardware capable of executing all computation paths. Within that hardware, we sought the optimal computation path from the perspective of the area-delay product. We have successfully found an optimal path that differs from the one specified in the SIKE specification, achieving a speedup of 3.5 times compared to the fastest hardware implementation in prior research.

Neural network and Its security

M. Ikeda, Z. Wang, Y. Miao, and B. Amartuvshin

Spiking neural networks (SNNs), due to their potential energy efficiency, are promising candidates for next-generation neural networks and are also expected to be able to integrate with neuromorphic sensors for efficient information processing. However, currently hardware implementations of SNN face significant difficulties

mainly due to the additional membrane potentials introduced by spiking neuron. To this end, we propose a lossless compression method for membrane potentials, which allows, for the first time, the use of a reduced-precision fixed-point format representation for membrane potentials in deep SNNs, thus achieving the lowest resource footprint and energy consumption of any FPGA-based SNN accelerators.

On the other hand, the techniques of cloud computing have been used to overcome the huge computing cost of deep neural networks on personal computers, while it suffers from the concern of data privacy. Homomorphic encryption (HE), which enables encrypted computations, is a promising solution. However, the computation on ciphertexts is typically slower than that on plaintexts by 1000-10000 times. In our research, fast computing schemes and customized hardware are designed to accelerate the HE computations. On computing scheme design, we propose a guideline of building bootstrapping-free Gated Recurrent Unit (GRU) networks, by which fast inference is achieved while the accuracy is almost preserved. On hardware design, a ciphertext multiplier, including key switching, modular switching and NTT/INTT blocks, is designed to accelerate ciphertext multiplication, which costs most computing time of HE-based NN inference on CPU.

Implementation of secret sharing

M. Ikeda, and Y. Zhao

Secure multi-party computation (MPC) is a cryptographic protocol enabling multiple parties to jointly compute a function over their inputs while keeping those inputs private. Compared with other approaches, computing time of Secret Sharing Technique is faster than others, but its computing is sensitive to the network latency and its communication round is increasing with the computation depth. We have evaluated in systems like close-memory computation and on-chip secret-sharing computation where communication resources is almost unlimited.

Security Measures of Crypto-engine

M. Ikeda, S. Kikuoka, K. Masada, and Q. Wang

It is important to start working on practical use now for cryptography that is expected to be utilized in the future, such as pairing-based cryptography with high scalability to advanced functional cryptography and lattice-based cryptography with resistance to attacks by quantum computers. We suggested method to estimate the security and hardware costs such as area and latency of hardware implementation, that can calculate pairing operations or lattice operations and that is implemented in ASIC, based on logic synthesis results. And then the results were evaluated for optimal ate pairing and CRYSTALS-Kyber. Also BLS signature has provable security which is currently desirable. We estimated the computation cost of BLS signature on a curve chosen based on the tightness of reduction. Also, we compared the parameter sizes of different signatures.

Research on Logic Locking

M. Ikeda, Z. Ye, J. Xin, T. Matsumoto

Logic locking is a technology that protects the intellectual property and security of integrated circuits by incorporating specific logic gates into circuit designs. We have applied post-quantum crypto-algorithm for the logic locking to realize robust logic lock system resistant to quantum computing.

The implementation of post-quantum crypto-algorithm(PQC) is becoming indispensable for cryptography in IoT devices. In this study, we have investigated the implementation of Crystals-Kyber accelerator, one of the PQCs, in RISC-V, an open-source processor, aiming to guarantee the security of future IoT devices.

Iizuka Laboratory

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Phase-Locked Loop Circuit Techniques for Low Phase Noise

Tetsuya Iizuka, Masaru Osada, Haoming Zhang, Yuyang Zhu

Ring VCO is a good candidate as the oscillator in a PLL because it has smaller area, less coupling, and multiple phases. However, its Phase Noise (PN) performance is generally much worse than the LC VCO, and requires the PLL to have the very wide bandwidth (BW) to high-pass-filter its noise. This contradicts with the necessity of the narrow BW required in the fractional PLL, because the quantization noise is low-pass-filtered by the PLL. The Harmonic-Mixer (HM) -Based fractional-N PLL is good candidate to use Ring VCO, because can achieve effective quantization noise suppression without using calibration, releasing the BW requirement to filter the quantization noise. Nonetheless, the DSM operating frequency is low in a common dual-feedback HM-PLL so that the quantization noise is still dominant when the main PLL BW is high. Thus, in this research, we added a nested PLL after the fractional divider to raise the DSM operating frequency and further filter the quantization noise. The chip has been successfully fabricated and the measurement results has proven the effectiveness of our idea.

Although HM-PLL is effective for quantization noise suppression, the downside of this architecture is that at least one extra PLL is required, potentially resulting in noise and power overhead that leads to a degradation in terms of jitter-power performance. Our second work is to propose a feed-forward noise cancellation technique that can be used inside the HM-based PLL to mitigate the noise and power overhead from the first-stage PLL and overcome its performance limitation. The proposed technique can also potentially be used in other cascaded PLL architectures to reduce the overhead from having multiple PLLs. The chip has been designed successfully, and the measurement result has proven our proposal.

We also focused on the enhancement of self-dithered MASH (multi-stage noise shaping) digital delta-sigma modulators (DDSMs) within fractional-N frequency synthesizers. To solve the problem of spurs with low input bit widths in conventional self-dithered MASH 1-1-1 DDSMs employing shaped dithering, we introduce to use self-dithering in a MASH 1-1-1-1 structure. The novel self-dithered MASH 1-1-1-1 structure suppresses fractional spurs effectively, even with low input bits, and does not require an external LFSR. This approach also offers an additional order of noise shaping, enhancing the PLL's phase noise and spur performance.

High-Speed and High-Precision Data Conversion Circuits and Design Automation Techniques

Tetsuya Iizuka, Shuowei Li, Ximing Wang, Haoming Zhang, Yo Kumano, Ritaro Takenaka, Yunjie Chen, Yuhao Xu

Standard cell-based analog circuits have many advantages, including high reusability, high integration, compatibility with automated design, reliability, and stability, making them highly promising for current and future research. We have designed a new standard cell-based synthesizable SAR ADC that employs a new differential architecture. This architecture eliminates the need for pre-biasing the DAC for each bit estimation, thereby reducing the CDAC power consumption. The control logic has been simplified, which also reduces the power consumption of the logic cells. Additionally, we have introduced a new inverter-based switch whose performance matches that of CMOS switches with dummies. This new structure helps to suppress the nonlinear effects of the switches. The reference voltage converges to the general power supply with less significant bit estimation, reducing the performance requirements of the comparator. The Walden Figure of Merit (FoMw) of this design can achieve one-eighth of that of the previous design. This design is being experimented with using digital synthesis tools to generate the layout. Furthermore, we have introduced a standard cell-based amplifier that can achieve a gain of over x60 while maintaining acceptable linearity. Based on this amplifier, we have also introduced

a synthesizable pipelined SAR ADC.

Dynamic circuit belongs to the digital circuit families which are used to realize digital logic function. However, unlike static CMOS digital circuit with both pull-up and pull-down network, dynamic circuit is asymmetric because it gets rid of one of the pull up/down network, replacing it with a single transistor for faster speed. In spite of the improved speed, the extra clock signal to control its operation phases (pre-charge and evaluation) has introduced huge difficulty in this timing characterization. Thus, the dynamic circuit has never included into the automatic digital circuit design flow as the static CMOS circuit up to now. To counter this trend, in this research we are aiming to provide a timing model for the timing characterization of dynamic circuit, and a on-chip test structure to extract the timing parameters including delays and setup/hold time after fabrication. The proposed timing model has been utilized and verified based on Synopsys Prime Time, a mature EDA used in modern industry. The chip of the test structure has been designed with TSMC 65nm process and successfully fabricated. The measurement results have well-proven our proposal.

For high-precision and high-power efficiency ADC design, we continued our research on fully dynamic discrete-time ΔΣ ADC using the Floating Inverter Amplifier (FIA) this year. Based on previous research about gain boost through CLS and noise cancellation via SNC, we proposed a novel technique called Fast Self-Quenching FIA reusing CRES for SNC to enhance the power efficiency of the integrator. We designed the circuit and fabricated a chip for a second-order 5-level fully dynamic discrete-time ΔΣ ADC, evaluating its performance through practical measurements. Additionally, we applied random dithering to the quantizer and analyzed the quantizer characteristics of the ΔΣ ADC based on the quantizer input histogram. Numerical analysis confirmed the correctness of the analytical approach, and approximate analysis demonstrated reproducibility of key elements. Furthermore, we highlighted an example of optimal design points to minimize quantizer nonlinearity in the second-order ΔΣ ADC, revealing a trade-off relationship between quantizer nonlinearity and integrator output amplitude.

High-speed and high-accuracy ADCs are required in many applications such as wireless transceivers and radars. We focused on a high-resolution subranging ADC. Compared with previous pipelined ADCs, this architecture is suitable for deeply scaled CMOS technology. We proposed a reverse biased amplifier, which has the small non-linear input capacitance, and a power-efficient multiple-reference comparator. We also proposed a split-reference C-DAC, which reduces the on-chip decoupling capacitors without an additional regulator. These ideas are implemented in a 14bit, 500MS/s ADC. The measurement results show the proposed ADC achieved the Schreier DR FoM of 179.4dB.

The standards of communication technology have evolved from 4G to 5G, and now research is being conducted towards the next generation, 6G. The new communication standards aim to feature ultra-wideband capabilities, support a wider range of frequency bands, and significantly improve data transfer speeds. As one of the technologies enabling ultra-fast data communication, the research and development of ultra-high-speed digital-to-analog converters (DACs) is urgently needed. Due to the internal parasitics and component characteristics of a single DAC, further enhancing its performance is difficult. In recent years, interleaving techniques have been frequently ultilized into DACs. Especially Time-interleaved DAC (TI-DAC). Previous work on TI-DAC has uncovered some potential design issues in 4 channel case like aligining the phase error between different frequency clock and extremely samll output scale. In this year's work, we have proposed a 20 GHz time-interleaved DAC which effectively addresses key issues in existing design, while maintaining the sampling rate and achieving a comparable SFDR. The proposed TI-DAC features a single-stage MUX and direct summation at the final output. It can sustain a SFDR of 63dB up to 65% of the Nyquist frequency in ideal case while in contrast, the existing TI-DAC can reach Nyquist frequency but suffers a 8dB reduction in SFDR due to output power losses.

This proposed structure replaces the second stage MUX by directly adding outputs from two MUX TI-DACs together. This modification simplifies the clock design significantly, reducing complexity while maintaining the accuracy of the system.

We examined methods to avoid the speed performance bottleneck caused by internal logic circuits in Successive Approximation Register (SAR) Analog-to-Digital Converters (ADCs) and optimize their performance by improving sampling speed. Traditionally, logic circuits have been designed using static logic circuits, which are simple to operate and easy to assemble. However, this simplicity can cause the logic circuits to become a bottleneck for the entire ADC. On the other hand, dynamic logic circuits offer faster speeds but are more complex to operate, making logic synthesis difficult and requiring time-consuming manual design In this study, we optimized the speed and power consumption performance of digital control circuits designed with static logic circuits by detecting critical paths in dynamic logic circuits and replacing the circuits within these paths with faster dynamic logic circuits. Using a 10-bit SAR ADC designed with a 28nm CMOS process as an example, we analyzed two designs using static logic circuits and demonstrated performance improvements by replacing some of the circuits with dynamic logic circuits. Furthermore, we organized and verified the necessary conditions and workflows for replacing static logic circuits with dynamic logic circuits to prepare for future automation of this replacement process.

Design of Low-Noise Transceiver for Deep-Space Probes

Tetsuya Iizuka, Sota Kano, Taku Hamazaki

The demand for miniaturization of deep space probes is increasing, with a particular emphasis on the miniaturization, lightweight design, and cost reduction of communication modules. Recent ultra-small planetary exploration probes use commercial off-the-shelf (COTS) components primarily to reduce costs. However, ensuring the reliability of systems that extensively use COTS components is extremely challenging and poses significant barriers for long-duration deep space missions. To address this issue, it has been proposed to integrate the transmitter, receiver, and digital signal processing units into a single chip. This approach not only reduces the overall size of the circuitry but also decreases the number of components, thereby potentially enhancing the reliability of the entire module.

In this study, X-band (7.2 GHz / 8.4 GHz) receiver and transmitter circuit chips were designed and evaluated in order to realize the one-chip communication system for deep space probes.

A receiver front-end including a low noise amplifier and down-conversion mixers was designed. A noise-cancelling technique for ultra-high sensitivity was demonstrated by simulations based on IHP SiGe 130 nm BiCMOS process. Besides, a prototype receiver front-end chip was fabricated using TSMC 65 nm CMOS process. Results of direct-probing measurements showed the noise figure of 2.3dB and demonstrated that our CMOS receiver chip achieves comparable sensitivity to that of receivers mounted on past deep space proves. Moreover, the measured input 3rd-order intercept point of –26 dBm proved that the receiver dynamic range of our chip is acceptable for operations in deep space explorations.

The overall structure of the X-band receiver was also studied and analyzed. Since deep space probes move at high speeds, the frequency of the received signal is deviated due to the Doppler effect. To compensate for this, we proposed an analog carrier tracking loop, which is suitable for the CMOS one-chip implementation. The proposed architecture was designed and analyzed in phase domain based on the measured front-end performance, and its superiority over conventional digital processing using an FPGA was discussed.

A transmitter front-end including a single-stage power amplifier and an up-conversion mixer was designed and fabricated using the TSMC 65 nm CMOS process, the operating frequency of which is 8.45 GHz for the satellite communications. Our simulations and actual measurements demonstrated that the power amplifier

could achieve approximately twice the efficiency compared to previous research on wideband power amplifiers by narrowing the operating frequency band.

Due to the presence of high-energy radiation in the space environment, integrated circuits will be susceptible to single event effects (SEE) and total ionizing dose effects (TID). Consequently, an evaluation printed-circuit-board for the future irradiation test was designed.

Design of Time-Domain Neuron Devices and Evaluation of Learning Systems

Tetsuya Iizuka, Byambadorj Zolboo,
Ckristian Duran, Nanako Kimura

With growing trends of Artificial Intelligence (AI), advancements are necessary to fit recent updates. Lately, implementations of Large Language Models (LLM) like ChatGPT demonstrate the capabilities of AI to solve complex problems. Unfortunately, the implementation of such models requires specialized computation equipment with very strong capabilities. This implementation limits the usability of such AI to connect to a centralized server. These limitations create problems such as privacy concerns due to sending and receiving data to a third party. This creates also a dependency on the internet due to incapabilities in personal devices. Moreover, the energy consumption of such computation is too high to be sustainable in the future. An alternative needs to be found such that it improves both computation power and energy efficiency.

Analog computing is a solution to the previously mentioned problem. A simple implementation of adders and multipliers can be achieved with low area and low power. The caveat of using analog computers is precision due to mismatches and noise. Fortunately, implementations of Neural Networks (NN) have demonstrated that they do not require fine precision. Our chosen implementation of analog computing is Spiking Neural Networks (SNN) using Integrate-Leakage and Fire (LIF) neurons. A LIF neuron performs calculations by integrating a series of pulses. The state of the neuron leakages over time, and also determines the fire of pulses to other neurons. The design of the LIF neuron consists of MOS capacitors to do the integration, triggering P/N transistors to do accumulations in excitations/inhibitions, and a Voltage-Controlled Oscillator (VCO) to emit the output pulses.

The LIF neuron designs were tested in different simulation environments (SPICE, Matlab, Python) of the neuron and the network to verify the capability of learning of the circuit. This circuit was designed in a commercial 65nm CMOS technology from TSMC. The simulation tests the capability of learning according to different models using Reservoir computing. The reservoir consists of the LIF neurons connected randomly or in specific configurations. Each of the neurons must be measured in real time. With the weighted sum of the neurons, different kinds of learning can be possible. Currently, the simulations support simple tasks like Short-Term Memory (STM) and eXclusive-OR(XOR), or more complex learning like waves at a certain range of frequencies and voice recognition.

To implement the SNN, LIF neurons must be interconnected together. This interconnection should support different kinds of computing paradigms including Reservoir computing. We designed a Field-Programmable Gate Array (FPGA) architecture to enable random connectivity between neurons. This FPGA is composed of Complex Logic Blocks (CLB) that contain the LIF neurons. The FPGA implementation is possible because the signals can travel digitally due to the nature of pulses of the input/output of the LIF neuron. Any kind of SNN can be translated into a schematic and be converted into a bitstream which contains the network. This FPGA system contains helper elements like frequency counters to provide the measurement of the neurons. Each frequency is extracted from the neurons and converted back into a voltage by an external device.

A neural network chip is implemented this year in a 65nm CMOS technology from TMSC. The chip contains the FPGA with 100 LIF neurons. This chip demonstrated the random connectivity of 100 possible neurons. The chip spans an area of 2000x2000μm. When implemented, the neurons consume a total of 21.7 pJ/pulse. Due to

resource limitations of the FPGA, this implementation implements a maximum of 50 neurons as a reservoir. We demonstrated the learning capabilities of waves in feedback configuration, and simple tests like STM/XOR.

Deep neural networks (DNNs), the second generation of artificial neural networks (ANNs), have been actively used in recent years. However, their huge power consumption has become a major problem, and a solution to this problem is being sought. One promising solution is the spiking neural network (SNN), which is called the third generation of ANN. The brain is known to have low power consumption of about 20W, and SNNs are thought to be able to reduce power consumption because they process information more like the brain. SNNs are composed of neurons that change their state over time according to neuronal mechanisms and transmit information by firing. The characteristic feature of SNNs is that the information is not carried in the value itself, as in conventional ANNs, but in the timing of firing.

From the perspective of electronic circuits, time-domain circuit technology has an affinity for SNNs. With the scaled transistors, the time delay of signal transitions is decreasing, and an increase in operating speed is occurring. The sharpening of signal transitions allows analog information to be transmitted more efficiently in the time interval and time direction of the signal. Furthermore, since time-domain circuits are often composed of inverters and logic gates, they have the advantage of not consuming DC power. This is consistent with our policy of low power consumption.

To construct an SNN in an electronic circuit, it is necessary to create neuron circuits and connect them together. There are many ways to realize neuron circuits. There is a model called Leaky Integrate and Fire (LIF) model which is simple and often used for engineering purposes. Circuits that follow the LIF model use comparators for setting threshold, which leads to an increase in area and power consumption. Also, power is consumed for reproducing leakage without being utilized for anything. Therefore, this research group created a neuron circuit that employs a voltage-controlled oscillator (VCO) as the firing mechanism and realized a circuit that consumes less power by performing firing without using a comparator and using the leakage to drive the VCO.

The neuron circuit was created last year and a simulation of SNN with reservoir computing method was conducted using this circuit. However, there were two issues. First, the simulation using the neuron circuit created last year assumed the use of an ADC to read the control voltage of the VCO. In order not to lose the advantage of the system, it is desirable to realize SNN without using an ADC, which is generally considered to have high power consumption. Therefore, this fiscal year, a counter was used to read the frequency of the VCO. In addition, the task performed in that simulation was the auto-generation of a sine wave. In general, in reservoir computing, the properties required of reservoirs are short-term memory, nonlinearity, and high dimensionality. It is difficult to analyze to which extent the fact that a sine wave can be generated attributes to which performance. Therefore, this fiscal year the task that was more appropriate to explore the characteristics of the network was performed.

Based on the above modifications, simulation environment for SNN circuits was created with Python. To simulate the behavior as close as possible to that of a real circuit, a behavioral model based on the results of Hspice simulations was created, and it was used to create the environment. To test the short-term memory capability, discrete input data was put into the system and it was checked how many steps before the input data could be replayed. In addition, a temporal XOR task was performed to verify the non-linearity and high dimensionality of the system. As a result, we confirmed that the system has short-term memory, nonlinearity, and high dimensionality. As an application, we also performed a speech recognition task for the numerical values 0-9. As a result, we obtained a high accuracy which was comparable to other previous studies.

Compared to other physical reservoir computing studies, the advantage of our system is the use of CMOS, which is widely used today. In addition, the results show

that performance increases as the number of neurons used in the SNN is increased. We can say this system, which can be easily integrated with current processes, is promising for improving accuracy.

Antenna Measurement and Testing Techniques for Wireless Communications

Tetsuya Iizuka, Mai Khanh Nguyen Ngoc, Byambadorj Zolboo

In 5G technologies, over the air (OTA) measurements are necessary for 5G antennas due to the technologies rely on millimeter-wave frequencies and small-sized terminals. The conventional OTA measurement is based on far-field measurement. However, the far-field measurement is almost infeasible in the millimeter-wave due to high path loss and low measurement accuracy. Therefore, near-field measurement takes place of OTA measurement in the millimeter-wave range. The far-field measurement data can be achieved from near-field measurement by using near-field to far-field methods.

In the past, we have used different types of antennas as a probe and antennas under test (AUT). It is well known that the measurement time and the probe design are the most important factors in near-field measurement.

This fiscal year, we successfully designed a dual-feed multi-probe with a target frequency of 28GHz. The multi-probe is capable of receiving dual-polarization signals in multiple positions simultaneously. Based on the measurement results, we have confirmed that the polarization ratio was more than 20 dB.

Using this multi-probe, the near-field measurement time can be significantly reduced by taking multiple samples in the scanning space. To capture these multiple signals, a new capturing system has been developed as the typical VNA has only several ports. As a proof-of-concept for the system and the multi-probe, we have successfully captured several AUT and reconstructed comparably good far-field characteristics.

Design of High-Sensitivity On-Chip Network Analyzer Circuits

Tetsuya Iizuka, Yuyang Zhu, Zhenyu Cheng, Jiaao Yu

Spin waves (SWs) are the collective excitation of electron spin. By the spin wave, the transmission and control of information can be realized without the physical movement. However, until now, there is no on-chip detection system to detect the response of the spin-wave, making it possible to be applied in next generation chips. Consequently, we proposed a spin-wave detection system. This circuit comprises several key blocks: a phase locked loop (PLL), a phase interpolator (PI), a low-noise amplifier (LNA), a lock-in amplifier (LIA), and analog-to-digital converters (ADCs).

Until now, we have successfully designed and fabricated chips for the blocks used in the system. For the transmitter side of the proposed spin-wave detection system, we started by designing a wide-band inductorless PI. Then proceeded to validate the design through simulations, ensuring its functionality and performance for the intended application in the spin-wave detection circuit. Based on the measurement results, the PI chip was implemented in 65nm CMOS technology. Subsequent measurements were conducted to assess the function and performance of the fabricated chips. Measurement results show a phase range of 0° to 360°, with DNL and INL at 0.6LSB and — 5.17LSB, respectively. Additionally, the PI core consumes 1.89mW at 5GHz.

Then we focus on the enhancement of self-dithered MASH (multi-stage noise shaping) digital delta-sigma modulators (DDSMs) within fractional-N frequency synthesizers. To solve the problem of spurs with low input bit widths in conventional self-dithered MASH 1-1-1 DDSMs employing shaped dithering, we introduce to use self-dithering in a MASH 1-1-1-1 structure. The novel self-dithered MASH 1-1-1-1 structure suppresses fractional spurs effectively, even with low input bits, and does not require an external LFSR. This approach also offers an additional order of noise shaping, enhancing the PLL's phase noise and spur performance.

For the receiver side, we designed an LNA with a chopper-stabilized LIA for weak signal detecting and amplifying. According to the measurement, the proposed LNA has demonstrated a maximum gain exceeding 31 dB in experimental measurements. Furthermore, the proposed LNA achieves reasonable power consumption of 11mW, occupied area of 0.066mm^2 , –3 dB bandwidth of approximately 1.2 GHz and minimum NF of approximately 3 dB during testing. Turning to the LIA, With the determination of the phase relationship established, we proceeded to measure the output-input characteristics of I/Q paths across various chopper frequencies. The proposed LIA achieves SNR greater than 0 dB at the listed chopper frequencies, which is proved to be feasible for 56 the measurement of the spin-wave device.

The next step of the work aims to measure the proposed blocks with the real spin-wave device, verifying the function and performance of the proposed system. And do more improvements based on the existing version of the system.

Millimeter-Wave Integrated Circuit Techniques

Tetsuya Iizuka, Taizo Yuasa

A Phase-Locked Loop (PLL) is a circuit that receives a reference signal, synchronizes its phase, and outputs a signal with multiplied frequency. PLLs have diverse applications, and in this research, we aim to apply them to RF testers. RF testers need to handle various high-frequency devices, so stringent requirements exist for operating frequency and jitter. Specifically, our goals include a tuning range of 50~100 GHz with low jitter. Different PLL architectures, such as Fractional-N PLL and Cascaded PLL, exist, and the optimal architecture depends on the operating conditions. Therefore, we determine the best architecture for our application based on simulations and proceed with circuit design.

To widen the tuning range of PLLs, we need to expand the tuning range of a Voltage Controlled Oscillator (VCO) inside PLLs. Typically, LC-VCOs use varactors for continuous frequency tuning and capacitors/inductors which can be switched with a transistor switch for discrete frequency tuning. However, this circuit configuration involves trade-offs. For instance, increasing the varactor size to widen the tuning range also increases the resonator's capacitance, leading to a lower oscillation frequency. Additionally, switches used for frequency switching require larger sizes to reduce on-resistance, but this increases parasitic capacitance between drain and source. In the millimeter-wave band, capacitor Q-factor degradation is significant, affecting phase noise performance. Promising techniques include multi-core VCOs and switching operation without transistor switch, which we are currently investigating.

On the other hand, designing circuits operating in the millimeter-wave band poses challenges related to the reliability of device models. Besides the effects of parasitic elements, foundries often lack verification for millimeter-wave characteristics, resulting in discrepancies between simulations and actual behavior. Even if we design the layout of elements and do the electro-magnetic simulation, obtaining accurate device characteristics remains difficult. Therefore, creating device models before circuit design is essential in the millimeter-wave band.

To create accurate device models usable in the millimeter-wave band, measurement results are necessary. In our research, we designed a chip using the TSMC 28nm CMOS process, incorporating basic elements for analog circuit design (transmission lines, transistors, resistors). Additionally, we included a single-stage common-source amplifier circuit to validate model accuracy. By measuring this chip and creating device models from the obtained results, we enable more precise circuit design.

Hiramoto & Kobayashi Laboratory

(https://vlsi.iis.u-tokyo.ac.jp/, https://nano-lsi.iis.u-tokyo.ac.jp/)

Low Temperature Characteristics of Nano-Scale CMOS Devices

Toshiro Hiramoto and Masaharu Kobayashi

The quantum computing has attractive much attention for a future computing technology that is fundamentally

different from classical computing by CMOS circuits. In the quantum computing systems, conventional CMOS circuits are utilized to control quantum bits. Therefore, it is essential to clarify and model CMOS transistor characteristics at low temperature. In this study, we revealed the origin of the increase of the variability in MOS transistors at low temperature. Currently, we are evaluating random telegraph noise at low temperature.

Stacked Silicon quantum bits

Toshiro Hiramoto and Masaharu Kobayashi

Semiconductor, particularly, silicon quantum bit is getting attention as a quantum bit for quantum computing. For practical quantum computing, more than ten-thousands of quantum bit should be integrated. In this laboratory, to realize highly scalable integrated system, we are studying 3D integration by stacked silicon qubit structure. Stacked silicon quantum bit structure is proposed by simulation. Currently, we are prototyping the device for demonstrating the feasibility.

Silicon Power Devices

Toshiro Hiramoto

Semiconductor power devices are fundamental products for power electronics used in consumer products, electric cars, and railways. Although new materials such as SiC or GaN are widely studied for power devices, it is still possible to increase performance of silicon power devices. In this study, we are demonstrating insulate gate bipolar transistor (IGBT) with scaling and dual gate structure for high performance. In addition, to integrate power devices into CMOS circuits, we are studying new lateral super-junction power MOSFET.

Research on atomic layer deposition of oxide semiconductor and its application for 3D integrated memory devices.

Masaharu Kobayashi, Toshiro Hiramoto

While 2D scaling is getting challenging, 3D monolithic integration that requires active device formation in BEOL layers is getting more attentions. Oxide semiconductor is attractive because it can be formed in BEOL layers at low process temperature. Sputtering has been used for flat panel display device of oxide semiconductor, but cannot be used for conformal deposition on 3D structure. In this research, we developed Atomic Layer Deposition (ALD) process for nanosheet oxide semiconductor, which is necessary for scaling oxide semiconductor transistors. Then, we clarified the trade-off relation ship among mobility, threshold voltage and bias-stress instability for device design. Furthermore, we introduced double-gate device structure and realized high mobility, normally-off operation and high reliability.

Research on energy-efficient fabrication process and reliability for HfO_2-based ferroelectric devices

Masaharu Kobayashi, Toshiro Hiramoto

Crystallization anneal is one of the most important process to form ferroelectric phase in HfO_2-based ferroelectric material. In this research, we employed LED anneal process which has high selectivity regarding wave length instead of conventional rapid thermal anneal using halogen light source. Then, we realized highly energy-efficient fabrication process by the LED light source which has the same wavelength for light emission as ferroelectric capacitors for light absorbance.

We also developed an in-situ and non-destructive evaluation method of ferroelectric property and laser PEEM spectrum of HfO_2 ferroelectric capacitors by collaborating with The Institute for Solid State Physics, the University of Tokyo. By using this method, we clarified the spatial and temporal relationship between electrical dielectric breakdown and PEEM spectrum.

Takagi Laboratory

(https://sites.google.com/g.ecc.u-tokyo.ac.jp/mosfet/)

Ge Metal-Oxide-Semiconductor (MOS) FETs and the 3-dimensional integration

Shinichi Takagi, Xueyang Han,
Kasidit Toprasertpong, Mitsuru Takenaka

We are investigating the technology to realize ultra-thin

Ge-On-Insulator (GOI) structures on Si substrates, the performance improvement of high-performance GOI CMOS using these structures, and the device physics that determines the electrical characteristics, with the aim of applying them to 3D integrated CMOS. In this fiscal year, we have been studying the fabrication of a (111) GOI substrate, which is expected to have high electron mobility due to suppressed surface roughness scattering, and the demonstration of n-channel MOSFETs on it. The (111) GOI channel with excellent crystalline and interface qualities can be formed by thinning the GOI layer formed by the smart cut method and then transferring it to another Si substrate. This GOI channel is further thinned by a digital etching method, and the operation of a (111) GOI n-channel MOSFET with a thickness of down to about 2 nm has been demonstrated.

HfO_2-based Ferroelectric devices

Shinichi Takagi, Kasidit Toprasertpong, Zuocheng Cai, Seong-Kun Cho, Masaki Ootomo, Zhenhong Liu, Kosuke Ito, Mitsuru Takenaka

MOSFETs using ferroelectrics (FeFETs) with polarization reversal as gate dielectrics and FeRAM using metal sandwich structures (MFM structures) as memory cells are expected to be future devices for ultra-low power memory and logic. In particular, devices based on ferroelectric and anti-ferroelectric materials such as $Hf_{1-x}Zr_xO_2$ and ZrO_2, which have been discovered recently, are of great interest because of their extremely high compatibility with current Si CMOS technology. We are studying the properties of these ferroelectric thin films deposited by an ALD method, the device operation principle of FeFETs, and the optimum device structures to realize excellent device characteristics. In this fiscal year, we systematically investigated the effect of HZO film thickness scaling on FeFET characteristics to realize FeFET memory with low-voltage operation and high reliability. We found that low-voltage operation can be realized by HZO thinning and that the degradation mode of memory window changes with lowering the operating voltage, leading to the recovery of memory window degradation by applying recovery pulses. Furthermore, the low-voltage disturb characteristics of FeFET memory and their physical mechanisms were investigated. It was clarified that the long-term disturb characteristics cannot be represented simply by integrating it over applied total pulse time. Here, two mechanisms are involved: the electric field modulation effect by charge de-trapping and the relaxation of the polarization itself. Furthermore, we found that an imprint phenomenon observed in MFM capacitors for FeRAM applications is caused by charge trapping/de-trapping in electrode/HZO interface regions.

Reservoir computing based on ferroelectric devices

Shinichi Takagi, Kasidit Toprasertpong, Eishin Nako, Rikuo Suzuki, Mingxia Wan, Mitsuru Takenaka, Ryosho Nakane

Reservoir computing has recently attracted attention as an AI computation method with computational load for learning. We have proposed that FeFETs and FeRAMs with memory-in-logic and nonlinear analog computation capabilities are promising hardware for the physical implementation of reservoir computing. Thus, we are searching for methods to improve AI performance of reservoir computing based on ferroelectric devices by examining operating schemes and device characteristics. In this fiscal year, we systematically investigated the device operation conditions that maximize reservoir performance, and showed that reservoir performance can be improved by choosing the center value of polarization switching as the center voltage of gate input and using an optimal drain voltage of about 1 V. For application to speech recognition, we have improved the performance of the proposed reservoir computing system for the spoken digit classification task using parallel-operation FeFET reservoirs and have achieved a classification accuracy of 98.1% by increasing the number of combinations of different frequency channels.

Understanding of Si CMOS operation under ultra-low temperatures for quantum computing application

Shinichi Takagi, Yutong Chen, Zhao Jin,
Kasidit Toprasertpong, Mitsuru Takenaka

In quantum computing systems, Si CMOS circuits that can operate at cryogenic temperatures such as 4 K must be placed close to the qubit chip to improve the number of qubits. For this purpose, we are conducting experimental and theoretical studies to quantitatively describe the electrical characteristics of MOS transistors at cryogenic temperatures and to clarify their physical mechanisms. In this fiscal year, we experimentally evaluated the change in SS (sub-threshold swing) values from room temperature to 4 K for Si n-MOSFETs and p-MOSFETs with different substrate concentrations. It was found that SS saturates at temperatures below 10 K for n-MOSFETs, whereas increases with decreasing temperature for p-MOSFETs. We have revealed that this result can be explained quantitatively by considering the low-energy part of tail states near the band edge as localized states and the high-energy part as mobile states.

Takenaka Laboratory

(https://sites.google.com/g.ecc.u-tokyo.ac.jp/takenaka-lab/)

On-chip/Off-chip optical interconnect

Mitsuru Takenaka, Rui Tang, Yuto Miyatake,
Tipat Piyapatarakul, Tomohiro Akazawa,
Sheng Fu, Hiroya Sakumoto, Dhruv Ishan Bhardwaj,
Kentaro Komatsu

We are advancing research on optical interconnects and I/O for LSIs using silicon photonics and other technologies. By utilizing a high-sensitivity phototransistor with an InP thin film integrated on a Si waveguide, we successfully monitored the optical intensity in the waveguide with low insertion loss. Simultaneously, we also succeeded in monitoring the output intensity of an optical switch driven by an integrated hybrid MOS phase shifter.

Si photonic integrated circuit for AI

Mitsuru Takenaka, Rui Tang, Yuto Miyatake,
Jooyoung Yoo, Mingzhi Huang, Tomohiro Akazawa,
Masahiro Fujita, Yosuke Wakita, Tomohiro Anda

We are advancing research on deep learning for AI using programmable optical circuits such as universal optical circuits. By using a new phase-change material, GeSbTeS (GSTS), at a wavelength of 1.55 μm, we successfully demonstrated an optical intensity modulator with low insertion loss. Furthermore, by applying the GSTS optical modulator to optical computing circuits, we showed that it is possible to perform calculations for convolutional neural networks.

Ge mid-infrared photonic integrated circuit

M. Takenaka, Yuto Miyatake, Tipat Piyapatarakul,
Chao Zhang

We are advancing research on mid-infrared optical integrated circuits using Ge waveguides formed on Ge-on-insulator (GeOI) substrates. By analyzing the operating principles of avalanche photodetectors with PIN junctions formed on Ge waveguides using GeOI substrates, we theoretically demonstrated that they have higher sensitivity compared to Si.

Uchida Laboratory

(http://www.ssn.t.u-tokyo.ac.jp)

In the Internet-of-Things (IoT) era, every physical device will be connected to network. In this framework, any physical devices will have sensors that will continuously obtain various kinds of physical as well as chemical information around us. We expect that big data consisting of these sensor outputs will be analyzed with AI and valuable information will be extracted to improve our quality of life. In our group, low-energy sensors and information processing devices have been developed by pursuing physics of nano-mateials and nano-devices. Recent research topics are as follows.

1. Metal nano-film sensors for breath diagnosis
2. Thermal transport analysis of nano-meterials for

low-energy sensors
3. Electron-phonon interactions at the interface of insulator and semiconductor
4. Supramolecular sensors
5. Information processing devices beyond von Neumann architecture

Someya-Yokota-Yamagishi Laboratory

(http://www.ntech.t.u-tokyo.ac.jp/, https://fles.t.u-tokyo.ac.jp/)

Fabrication of Self-adhesive Organic Thin Film Transistors on Elastomeric Nanofilms

Chika Okuda, Sunghoon Lee, Kento Yamagishi, Tomoyuki Yokota, and Takao Someya

Devices that can be intimately contacted with our skin are increasingly gaining attention because of their huge potential in collecting long-term vital data for future healthcare, nursing, or sports activities. One of the key components is flexible or stretchable transistors, since they are necessary for signal amplification close to the body, or sensor matrixes to collect spatial data. Although these devices can contact well to the human skin, adhesiveness and robustness needed improvement in order to achieve long-term signal collection. Nanofilms, which are below 2 μm thick and are made of elastomeric materials, have shown sufficient adhesiveness and robustness to be worn on skin for over a week. These elastomeric nanofilms has become a candidate for wearable devices' interface, but only electrodes have been fabricated on them, due to difficulty in handling and adhesiveness issues during the fabrication.

We fabricated novel device structure and process of organic thin film transistors (OTFT) on elastomeric nanofilms. The substrate film is ultrathin with average thickness of 1～2 μm, enabling the film to be self-adhesive requiring ~130 μJ/cm^2 for detachment from artificial skin. This film was fabricated by dip-coating electrospun polyurethane nanofibers into polydimethylsiloxane solution. The film was then placed onto a flexible supporting substrate with release agent. Bottom gate was formed by thermally evaporating gold through a shadow mask, followed by chemical vapor deposition of parylene as the dielectric layer. Subsequently, organic semiconducting layer of dinaphthothienothiophene (DNTT) and gold contact electrodes were formed by thermal evaporation. Finally, OTFTs on nanofilms were delaminated manually from the supporting substrate to become free-standing state. The fabricated transistors exhibited electrical characteristics comparable to those fabricated on conventional substrates. They showed excellent yield (over 90%), with mobility of 0.19 ± 0.02 cm^2/Vs and maximum on/off ratio of above 10^5.

Mita Laboratory

(http://www.if.t.u-tokyo.ac.jp)

TopoMEMS: Development of Ideal Variable MEMS in view of Future Topological Quantum Computing

Y. Mita, R. Takahashi, K.Tsuji, A.-C.Eiler, S. Yasunaga, A.Higo, T.Iizuka, M.Ezawa (Dept. Applied Physics)

Recently, new computation methods that use Topological nature are drawing much attentions in view of future Quantum computing. Calculation takes advantages Topological natures existing in several different fields ex-pressed as Hamiltonian matrices. Our team, granted by JST CREST project, tries to explore electrical expression of Hamiltonian matrices used for computation. Team Mita will develop ideal variable electrical devices as well as ideal MEMS devices. We named such devices and systems "TopoMEMS". As an initiating study, we have taken Su-Schriffer-Heeger model. We have newly proposed a method to make use of magnetic coupling instead of electrostatic coupling to establish topological circuit. The successful demonstration have been accepted in an international conference. In parallel, a new concept of making use of MEMS movement directly for computation is granted as JSPS Kakenhi Kiban A. A three-stage bistable MEMS actuators have been successfully demonstrated and presented in the international conference.

Study on LSI-MEMS energy-autonomous distributed microsystems

Y. Mita, K.Misumi, G. Hwang (LIMMS, CNRS-UTokyo IIS / CNRS C2N)

As one example of future integrated MEMS that is expected to open new research and industrial application fields, the authors are trying to show a top-down application of energy-autonomous harmonized distributed mi-crorobots. A number of identical tiny robots, sized below 1cm, will be released in an environment. Individual robot can communicate with their neighbor, stick each other, and share energy, to realize cooperative function. The French National Research Center (ANR) grant that the PI received on behalf of host professor of CNRS laboratory in the Institute of Industrial Science (LIMMS, CNRS-IIS, UMI 2820), together with FEMTO-ST Laboratory and PSA-Peugeot Laboratory, named Programmable Matter", has concluded with some PoC devices. The project is fol-lowed by microrobots for biological applications with Dr Gilgueng Hwang.

Integration of electrode devices on MEMS fluidic devices

Y. Mita, A.-C. Eiler, A. Higo, E.Ota, A. Mizushima, N. Kawai, Y.Okamoto (AIST), N.Washizu (Advantest), M. Fujiwara, T.Sawamura

Towards the goal of production of brand-new sensor devices with higher sensitivity and functionality, the team is working on small-gap electrode fabrication process. This year, we have developed a post-process on Ful-ly-Depleted SOI VLSI device for massively parallel measurement and its integration is underway. Variation of I-V characteristics has been the issue but we could identify the root cause. In addition, additive (electroplating) fab-rication of micro and nano structure has been inisiated.

Fine Large-Area Electron Beam Lithography Exposure Methods

A. Higo, Y. Ochiai, M. Fujiwara, T.Sawamura, Y. Mita

The team explores newly-acquired (in 2013) rapid electron beam writer F7000S-VD02. The capability of high electron dose and sharp edge due to cell (character) projection machine configuration is being examined. The breakthrough in question is to extend the large-area EB lithography, whose pattern approximation have been limited to rectangular shapes, into expressing free-form smooth shapes and a number of periodical small patterns. This year, pattern and process design has been successful to obtain gap structure less than 16-nm wide. The result has been presented as a peer-reviewed journal.

Universities-Industries collaborative research on highly-functional system by MEMS post-process of CMOS-VLSI

Y. Mita, R. Shimamura, F. Sakuma, S. Yasunaga, T. Lévi(IMS-CNRS,Bordeaux), G. Larrieu (LAAS-CNRS,Toulouse), Y.Ikeuchi (IIS), A. Tixier-Mita (IIS), K.Saito (Nihon Univ.)

The research targets are new sensor devices, made by post-process at clearnrooms such as d.lab Takeda Supercleanroom and others, of VLSI wafer made through d.lab/VDEC. The important finding has been that VLSI wafer acquired just after transistor fabrication could sustain processes even with heat treatment, such as deposition, ion implantation, and drive-in. In 2016, a VLSI device made on Silicon-on-Insulator (SOI) wafer was successfully Deep-RIE processed. The industrial interest is its versatility – many different types of application devices, which differ one from another according to request of market, can be fabricated by using the same technology. More and more companies are interested in the scheme and are working on the technology on the collaborative research projects, including international cooperative research projects. This year we have realized a new scheme "Bio-Chiplet" that enables agile measurement system preparation. We have successfully demonstrated dual-modal measurement of Albumin and pH by composed chiplets. Also, in view of vertical (stack) integration, we have demonstrated "nano cone-shaped penetrator" that breaks isolation layers (both intentional and unintentional ones) between chiplet pads. The fabrication and measurement results were presented in IEEE MEMS conference (world's top conference) and

the presenter student (Mr. Shimamura) obtained IEEE MEMS Outstanding Poster Presentation Award, which is the top award in MEMS area.

Test Structure for high-density CMOS-MEMS hybrid integrated Technology

Y.Mita, A.Mizushima, K. Misumi, H. Matsuoka,
M. Yamagata, A.Higo, R. Nakane,
K.Tsumura (Toshiba), T.Yoda (TITech),
K. Higashi (Toshiba), and Y.Ochiai

Chip-level highly-dense bonding integration is drawing high attention to simply obtain high-functional system; preventing slip misalignment is one of challenges towards million-level micron-square pads bonding. We try to introduce passive alignment mechanism inspired by teeth clenching. Preliminary results have been accepted in an international conference.

Appendix

A.1 VDEC CAD Tools

Since 1996, VDEC has provided CAD software licenses to the registered researchers in universities and colleges in Japan. The CAD tools we provided in 2024 through the activities of VDEC in Systems Design Lab (d.lab) are shown in Table A.1.1. The researchers can use those CAD tools when their local machines, whose IP addresses are registered in advance, are authorized by one of VDEC license server located in the ten VDEC subcenters shown in Figure A.1.1. For each CAD tool, VDEC provides 10-1000 floating licenses. Those CAD tools can be utilized only for research and education activities in national universities, other public universities, private universities, and colleges. When one is going to use VDEC CAD tools and chip fabrication service, some faculty member of his/her research group in a university or a collage needs to do user registration.

Table A.1.1 VDEC CAD tools

Name	Function	Vendor
Cadence tool set	Verilog-HDL/VHDL entry, Simlation, Logic synthesis, Test pattern generation, Cell-based (including macros) place, route, and back-annotation, Interactive schematic and layout editor, Analog circuit simulation, Logic verification, Circuit extraction	Cadence Design Systems, Inc.
Synopsys tool set	Verilog-HDL/VHDL simulation, Logic synthesis, Test pattern generation, Cell-based (including macros) place, route, and back-annotation, Circuit simulation, Device simulation	Synopsys, Inc.
Siemens tool set	Layout verification, Design rule check	Siemens Electronic Design Automation Japan K.K.
Silvaco tool set	Fast circuit simulation	Silvaco Japan Co., Ltd.
ADS/Golden Gate	Design and verification of high-frequency circuits	Keysight Technologies
Bach system	BachC-based design, synthesis, and verification	Sharp
LAVIS	Layout visualization platform	TOOL

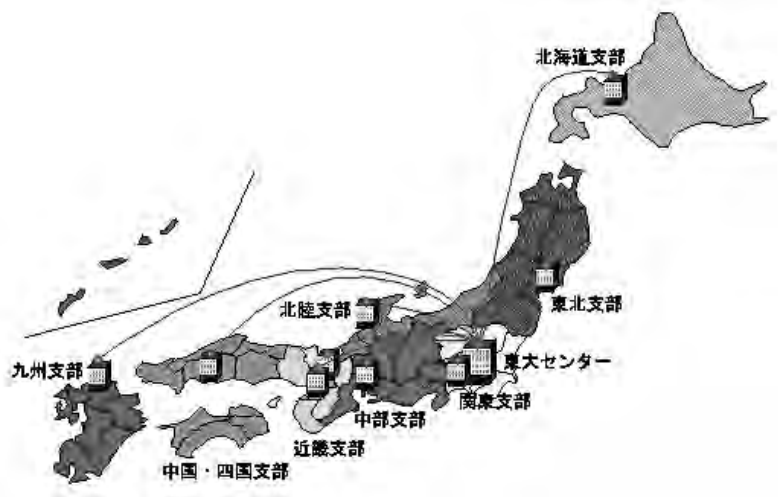
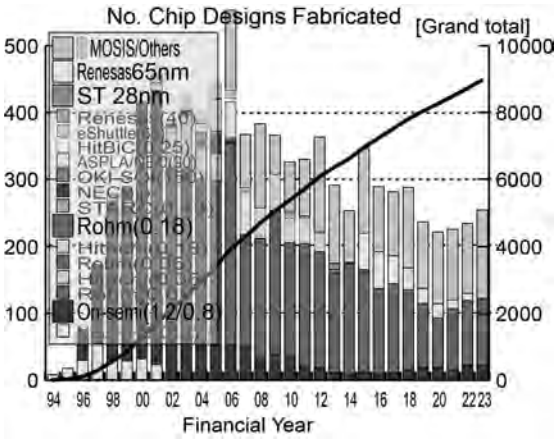


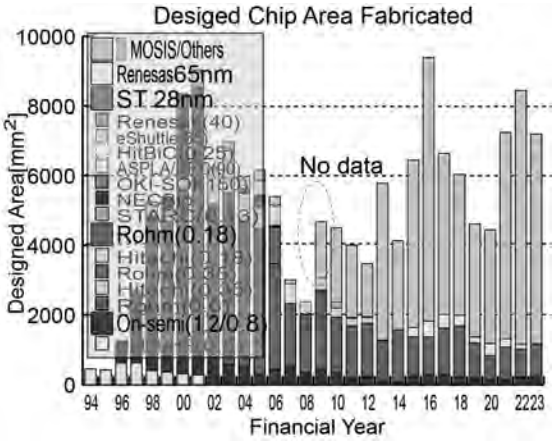
Fig. A.1.1 VDEC Subcenters

A.2 Status of Chip Fabrication Support at Platform Design Research Division

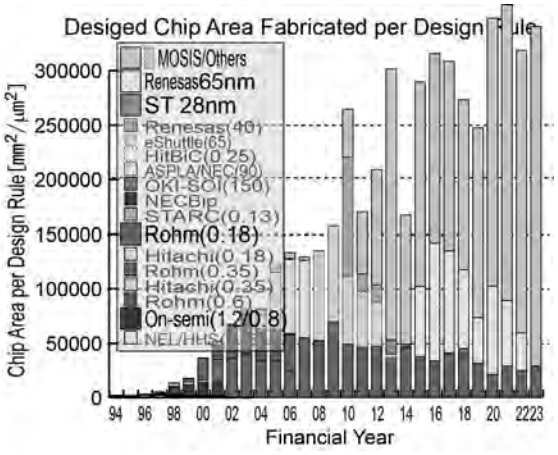
As for the support for VLSI chip prototyping, in the pilot project in FY 1994 and 1995, there was only one foundry, NEL's CMOS 0.5μm (the process was later continued by Hitachi Hokkai Semiconductor). After the inauguration of VDEC in 1996, the 1.2-μm CMOS process of Motorola Japan (which was continued by ON Semiconductor in 1999) started cooperation, and the 0.6-μm CMOS process of ROHM was added in 1997. In 1997, CMOS 0.6μm from ROHM was added, followed by 0.35μm from Hitachi, Ltd. in 1998, and 0.35μm from ROHM in 1999. In addition, as part of the IP development project, a prototype of STARC 0.13μm was developed. Since FY 2001, we have been providing services of CMOS 0.18μm from Hitachi, Ltd. In 2002, under the leadership of Dr. Iwata of Hiroshima University, we conducted a trial trial fabrication service in cooperation with VDEC and MOSIS. This service provides overseas fabs such as TSMC and IBM at low cost through MOSIS. Furthermore, under the leadership of Dr. Shibata of the University of Tokyo, NEC Compound Device, Inc. provided a prototype service for bipolar LSI. In 2004, we started prototyping Oki Electric CMOS SOI 0.15μm process and ASPLA 90nm process as test prototypes, and the 90nm prototype was operated as a regular prototype from 2005 in the form of public solicitation. In FY2006, we started trial production of 0.18μm process by ROHM and test production of 0.25μm SiGeBiCMOS by Hitachi, Ltd. In FY 2007, we started to study an advanced process to succeed 90nm CMOS, which was terminated in FY 2007, and in FY 2008, we started trial production of eShuttle's 65nm CMOS. In addition, as part of the METI-STARC project "Next Generation Semiconductor Circuit Architecture Commercialization Support Project," prototype production using Renesas Electronics' 40nm CMOS was also started. On the other hand, CMOS1.2μm was terminated in September 2011, Renesas Electronics' 40nm CMOS prototyping was terminated in 2012, and eShuttle's 65nm CMOS prototyping was terminated in August 2013. As a successor to CMOS 1.2μm, a test prototype of CMOS 0.8μm was conducted in October 2012 with the cooperation of Onsemi-Sanyo Semiconductor Manufacturing Co.(now JS Foundry).



(a) Trend of number of designs fabricated.



(b) Trend of designed area.



(c) Trend of designed area normalized by design rule.

Figure A.2.1 Trend of number of designs and designed chip area.b

As for the leading-edge prototyping, STMicroelectronics started FD-SOI 28nm CMOS prototyping through CMP of France in FY 2013. In addition, we started SOTB 65nm CMOS prototyping by Renesas Electronics as a regular prototyping in FY2015, and concluded in FY2022. In FY2021, we started BiCMOS 0.18um prototypes under an agreement with IHP of Germany.

Fig. A.2.1(a) shows trends of number of chip designed for VDEC chip fabrication. For the first 6 years until 2001, the number of designed chips shows steady increase, which means drastic improve of the effectiveness researches and education of LSI design, and we assume drastic increase of number of students related to LSI chip design and education. During few years of stable number around 400 chip designs per year, we can see transition of designs toward finer process. In 2007, we saw a large drop, which was caused by sudden process transition from 0.35μm CMOS to 0.18μm CMOS, and in 2008, we also saw another drop by process transition from 90nm CMOS to 65nm CMOS.

Fig. A.2.1(b) shows trends of designed chip area, which shows much clear trends of drop by process migration. On the other hand, Fig. 2.3.1(c) shows trends of designed chip area normalized by design rule, which assume to be strong relation with design efforts. Coming from the fact that the normalized chip area is still growing, we assume the major reason for decrease of number of chips and designed area is increase of design effort per chip and per unit area due to process scaling.

Fig. A.2.2 shows trends number of professors and universities fabricated chip. Number of professors who have contracted NDA for process technologies to access design rules and design libraries are, 304, and 56, respectively, for 0.18 μm CMOS, and 0.8um CMOS.

Table A.2.1 lists chip fabrication schedule in 2023. Please refer to list in Appendix B for details of designers and contents of chip designed.

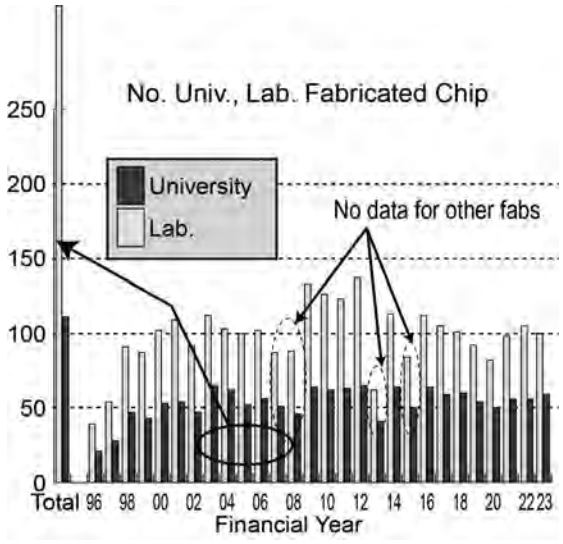


Figure A.2.2 Trend of number of processors and universities fabricated chip.

Table A.2.1 Chip fabrication schedule in 2023

0.8 µm CMOS (JS Foundry (former On-Semiconductor – Sanyo))

	Chip application deadline	Design deadline	Chip delivery
2023#1	2023/7/3	2023/9/25	2023/12/18
2023#2	2024/1/9	2024/3/25	2024/6/24

0.18 µm CMOS (Rohm)

	Chip application deadline	Design deadline	Chip delivery
2023 #1	2023/4/3	2023/6/26	2023/10/13
2023 #2	2023/6/12	2023/9/4	2023/12/16
2023 #3	2023/7/31	2023/10/23	2024/2/9
2023 #4	2023/12/4	2024/2/26	2024/6/7

A.3 Seminar

Seminars are always needed as the advancement of LSI design technology. In 2023, VDEC has held CAD Seminar and Designer's Forum, for academic circuit designers.

A.3.1 CAD Seminar for VDEC users

Along with advancement of circuit design CAD tools, tutorials on these tools are highly demanded. VDEC offers the CAD Seminar twice per year. In the CAD Seminar, VDEC invites lecturers from venders including Cadence, Synopsys and Keysight to give tutorials on their CAD tools. The seminar is held in VDEC, The University of Tokyo and VDEC sub-centers simultaneously in several universities nationally, in March of one fiscal year. Each tutorial takes one or two days.

Table A.3.1 CAD technical seminar in 2023 fiscal year

CAD Seminar I

Date	Tutorial	Venue	Number of Applicants
8/17	Cadence Virtuoso Schematic	online	35
8/18	Cadence Virtuoso Layout	online	37
8/22	Cadence Voltus-Fi	online	10
8/30	Keysight EMPro-FEM	online	20
9/4	Cadence Quantus	online	15
9/14	Cadence Spectre	online	26
9/15	Synopsys: PrimeSim SPICE/HSPICE	online	11
9/28	Synopsys: ICC2 Q&A	online	1
～9/30	Synopsys: ICC2	on-demand	21

CAD Seminar II

Date	Tutorial	Venue	Number of Applicants
3/11	Keysight ADS Fundamental	online	28
3/15	Synopsys Design Compiler & IC Compiler II Q&A	online	13
3/15	Synopsys StarRC Q&A	online	11
3/21	Cadence Virtuoso Layout Editor	online	51
3/22	Cadence Innovus Digital Implementation System	online	23
3/25	Cadence Clarity 3D Solver	online	16
3/26	Synopsys Sentaurus Q&A	online	12
～3/31	Synopsys Design Compiler	on-demand	29
～3/31	Synopsys IC Compiler II	on-demand	22
～3/31	Synopsys StarRC	on-demand	24
～3/31	Synopsys Sentaurus Basic & Post Basic	on-demand	18
～3/31	Synopsys Photonics Solutions	on-demand	14

A.3.2 Refresh Seminar for industry and academia

The fundamental and advanced knowledges are both imperative to integrated circuit design. VDEC offers the Refresh Seminar for industrial and academic people. University professors and highly experienced engineers are invited to give lectures on circuit design, covering the topics on analog, digital, RF, MEMs, and basic design flow. The seminar was originally launched in 1998, with the support of Ministry of Education Technical Education Division. It is now being supported by several industrial/academic societies.

Table A.3.2 Refresh Seminar

Date	Course	Contents	Lecture	Attendees
8/28, 29	VDEC Digital Circuit Design Flow	Digital circuit design flow using VDEC-collaborated CAD environment and process	Kazutoshi Kobayashi (Kyoto Institute of Technology) Ryo Kishida (Toyama Prefectural Univ.) Shinichi Nishizawa (Waseda Univ.)	8
8/31, 9/1	Transistor-Level Circuit Design Flow	Custom circuit design flow using VDEC-collaborated CAD environment and process	Toru Nakura (Fukuoka Univ.)	7
9/5, 6	MEMS I	Basics of MEMS MEMS Simulation and Layout	Yoshio Mita (Univ. of Tokyo)	6
9/11, 12,13	MEMS II	MEMS design MEMS fabrication and measurement at Takeda Cleanroom	Yoshio Mitai (Univ. ok Tokyo)	4
9/20, 21, 22	Analog Circuit Design	Analog Circuit Design and simulation Integrated Circuits Verification (LVS, DRC)	Masahiro Sugimoto (Chuo Univ.) Tetsuya Iizuka (Univ. of Tokyo) Koji Kotani (Akita Prefectural Univ.)	14
9/25, 26	CMOS-RF Circuit Design	Modulation/Demodulation Cascaded connection Basic Performance Transceiver Architecture Circuit Element Design Flow	Hiroyuki Ito (Tokyo Inst. of Tech.)	6

Fig. A.3.1 Refresh Seminar at VDEC seminar room at the University of Tokyo, VDEC.

A.3.3 Designer's Forum for academia

VDEC LSI designer forum intended for students and young teachers were held. The VDEC LSI designer forum has aimed to sharing the information that generally hard to be obtained common technical reports or academical papers, such as the failure an LSI designer had been through and the solution, and the construction method in the design milieu in the laboratory.

Table A.3.3 Program of Designers Forum in 2023

9/29-30 Hybrid Attendees: On-Site 29, Online 2	
9/29	
13:00-	Reception
13:30-13:35	Opening
13:35-14:35	Keynote Speech
14:35-14:45	Break
14:45-16:05	Design Award Presentation I
16:05-16:10	**Break**
16:10-17:55	Design Award Presentation II
9/30	
9:00-10:15	Idea Contest Presentation
10:15-10:25	Break
10:25-11:35	PhD Session
11:35-	Voting and Award Ceremony

A.4 Venture companies related to VDEC

Some professors related to VDEC started venture companies. The following is a list of the venture companies related to VDEC.

[1] AIL Co.,Ltd. (http://www.ailabo.co.jp/)

Related professor : Professor Kazuo Taki, Kobe Univ. (Representative Director)

Description of business : (1) LSI design service
(2) Engineer dispatching service
(3) Recruitment
(4) Management consulting

[2] Synthesis Corporation

(Merged with Soliton Systems on July 1st in 2017, http://www.synthesis.co.jp/)

Related professor : Professor Emeritus Isao Shirakawa, Osaka Univ. (Director)

Description of business : (1) System LSI development and design service
(2) IP development and sales
(3) Development and sales of IPs
(4) Development of EDA tools

[3] ASIP Solutions (http://www.asip-solutions.com/)

Related professor : Professor Masaharu Imai (Representative Director, CTO)

Description of business : (1) R&D, education and consulting of IoT application system
(2) Sales of ASIP design tool and consulting of ASIP development

[4] Nanodesign Corporation (http://www.nanodesign.co.jp/)

Related professor : Professor Kazuyuki Nakamura, Kyushu Institute of Technology. (Representative Director)

Description of business : (1) LSI design and development
(2) Development of LSI CAD and LSI evaluation tools
(3) Design consulting, etc.

[5] A-R-Tec Corp. (http://www.a-r-tec.jp/)

Related professor : Professor Emeritus Atsushi Iwata, Hiroshima Univ. (Representative Director)

Description of business : (1) Analog IC design and measurement
(2) PCB noise analysis
(3) Develop human resources, OJT, Lecture

[6] Ishijima Electronics (http://ishi.main.jp/)

Description of business : (1) Electronic circuit and board development
(2) Software development
(3) Consulting

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