Clock data recovery evaluation report on September 17 – September 19, 2014

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Background

A new digital clock and data recovery (CDR) algorithm was developed for a serial receiver. The algorithm is designed to allow recovery data from a signal with unknown transmission rate. It is also designed to have a low bit-error rate even when the received signal has a significant amount of timing jitter. The intended application for this is for communication in low-power circuits which do not have a stable clock reference. For example, in the Hirose tactile sensor system, there is no crystal oscillator on the sensor node circuit. The clock reference is a simple RC-based oscillator so communication between devices must allow for clock drift or timing jitter. Additionally, a high-speed variant of the algorithm was developed to demonstrate that the algorithm can be useful for a wide range of applications. The low-power variant was implemented for a 60 Mbps data rate, and the high-speed variant was implemented at 550 Mbps. 550 Mbps was the maximum data rate that could be achieved on the test board because of the speed limitation of the I/O of the FPGA.

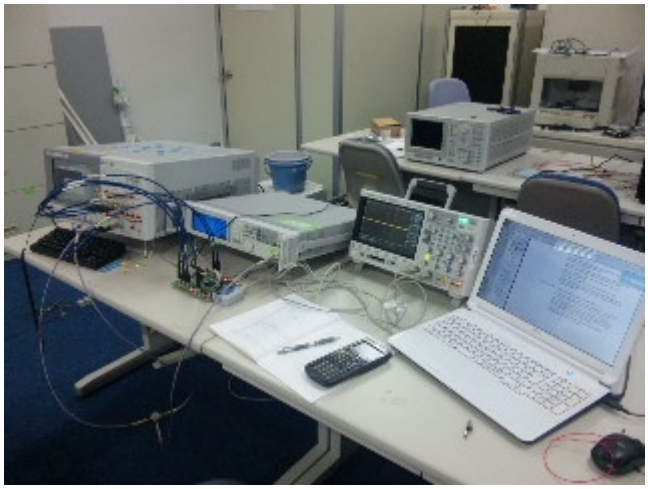
In order to demonstrate the practicality of the new CDR, it is necessary to evaluate the data rate, timing tolerance, power consumption and size compared to existing CDR algorithms. Evaluating timing tolerance requires a special bit-error rate tester (BERT) which can measure the bit error rate while different types and amounts of timing jitter are applied to the inputs of the design under test (DUT). In this way, the performance of the DUT (BER) can be clearly seen as a function of timing jitter. Jitter tolerance is an important metric for both low-power applications and high-speed applications. This is because in the case of low-power systems, there is no stable clock. In the case of high-speed systems it is also very difficult to have a low amount of timing jitter.

Evaluation and outcome

Originally, we intended to use the Agilent N4903B BERT along with a DC power supply and oscilloscope for hardware debugging. This BERT seemed very suitable for our evaluation. It has built-in calibrated jitter sources, which means that jitter tolerance can be evaluated without any additional equipment in the test setup. However, when we began using the equipment, we found that the N4903B BERT has a minimum data rate of 620 Mbps. Unfortunately, we had not realized this before we arrived at the VDEC lab. With our DUT limited to 550 Mbps, our testing plan was disrupted by this incompatibility.

We tried a number of different approaches to work around the problem. The first was to try to get the N4903B BERT to work at 550 Mbps data rate. We did find a way for this by using an external 550 MHz clock source (Agilent N5181A). Unfortunately, data alignment was unavailable and jitter

sources were limited at this data rate for the BERT. These are necessary features, so without them the test could not proceed.



Test setup with N4903B BERT, N5181A signal generator, oscilloscope, and DUT

The second work-around was to use the Agilent ParBERT 81250. This device is similar to the N4903B BERT but it does not have built-in jitter sources. Instead, a very basic circuit was developed to create jitter for the DUT stimulus signal. Using the ParBERT 81250, we were able to setup the test environment. However, it seems there was some installation problem with the BERT software. When trying to run the measurement, the software gave an error message saying "LabVIEW Run-Time Engine 7.1.1 not installed, please insert disk." We did not have enough time to both establish a functioning software installation and run the tests.

Instead, the best approach seems to be to upgrade the FPGA evaluation board so that 620 Mbps can be reached. Once this is accomplished, it will be possible to use the Agilent N4903B BERT as originally intended. Porting the design to the upgraded hardware should be relatively simple because it is a digital design. We hope to return to the VDEC lab to evaluate the design once this upgrade has been completed.