Self-Dithered Digital Delta-Sigma Modulators for Fractional-N PLL

Zule XU, Jun Gyu LEE, *and* Shoichi MASUI†
Research Institute of Electrical Communication, Tohoku University
†E-mail: shomasui@riec.tohoku.ac.jp, Tel: 022-217-5472

SUMMARY Digital delta-sigma modulators (DDSMs) applied in fractional-N frequency synthesizers suffer from spurious tones which undermine the synthesizer's spectral purity. We propose a solution featuring no hardware overhead while achieving equivalent spur elimination effect as using LFSR-dithering. This method can be implemented on MASH and single-loop DDSMs of 3rd- and 2nd-order.
key words: *Digital delta-sigma modulator (DDSM), fractional-N PLL, dither.*

1. Introduction

Digital Delta Sigma Modulators (DDSMs) are widely used in fractional-N phase locked loops (PLLs) which are indispensable in modern communication systems [1]. In a fractional-N PLL, shown in Fig. 1, the DDSM quantizes *n*-bit DC input X into an m-bit time-variant integer Y to instantly modulate the programmable divider's modulo ($n > m$). On a long run, the average modulo becomes ($N + X/2^n$), and the average of PLL's output frequency f_{vco} becomes the product of the reference frequency f_{ref} and average modulo; thus the output frequency with high resolution is available. The quantization noise is shaped into high frequencies and suppressed by the loop filter.

The basic building block of a DDSM is an accumulator, or 1st-order DDSM, unused in PLL applications due to its non-white quantization noises. Higher-order DDSMs are preferred for better noise-shaping and whither quantization noise. Higher-order DDSMs are generally classified into two types – MASH and single-loop. The former possesses advantages of stability and considerable noise-shaping; the latter is conditionally stable but enables a flexibly optimized noise transfer function (NTF).

The DDSM suffers from spurious tones which through the loop appear at the PLL's output spectrum, known as "fractional spurs", higher than the noise floor and hard to be suppressed, degrading the PLL's spectral purity [2]. To solve this problem, several solutions have been proposed which will be discussed in the following sections. In this paper, we propose an effective alternative, called self-dithering, featuring extremely simple implementation and no hardware overhead.

2. Spurious Tones from DDSMs

DDSMs are implemented with accumulators with a DC input so that periodic patterns are prone to appear at their output sequences. In other words, in the DDSM's output spectrum more power converges onto some certain frequency tones. Even for higher-order DDSMs of both types, spurious tones are observed for some certain DC inputs. Since the PLL acts as a low-pass filter to the quantization noise, shrinking the loop bandwidth lowers the out-of-band spur level. By doing this, however, spurs are not eliminated and the settling of the loop may be intolerably slowed, failing to achieve the spec. Therefore, techniques for eliminating the DDSM's spurious tones are highly demanded.

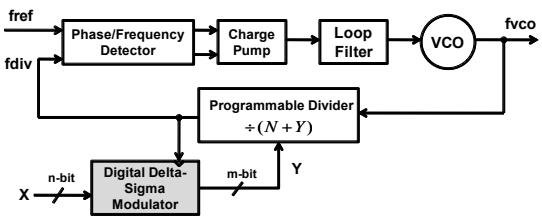

Fig. 1 Block diagram of a fractional-N PLL.

3. Previous Solutions

Previous solutions are classified into two types – deterministic [3][4] and stochastic [2][5]. Deterministic approaches modify the DDSM's structure or set up an irrational condition to disrupt the modulator's internal states. The advantages of this type of solutions are the controllable sequence length, or period, and no low-frequency noise floor incurred, yet so far they are mainly used for MASH. On the other hand, the stochastic solution, also called dithering, is used for both types of modulators. It exerts a 1-bit pseudorandom (PN) sequence to scramble the DDSM's input. Since dithering introduces an elevated noise floor at low frequencies, shaped dithering has been proposed to transfer the additive noise into a high-pass characteristic [5].

An unwanted task to implement the dithering is that the PN generator has to be specifically designed with extra circuits. It is commonly realized with linear feedback shift registers (LFSR) [4], while a recently published method employs another accumulator together with an 11-stage LFSR to dither the DDSM's coefficients [2]. Indeed, such extra endeavor can be avoided by applying the method proposed in the following section.

4. Proposed Self-Dithering Method

The proposed method circumvents the design of the PN generator; instead, utilizes the DDSM's own quantization noise which is generally approximated to be white, thus suitable as a dithering source. For a MASH DDSM, the quantization noise of interest is generated at its last-stage accumulator's sum, while for a single-loop modulator, it lies at the n LSBs of the data before the quantizer, where n is the DDSM's input bit width. Fig. 2 and Fig. 3 illustrate the implementations of 3rd-order self-dithered DDSMs of MASH and single-loop, respectively, where in the adder, A, B, S, C_i and C_o are n-bit inputs, sum of A and B, carry input, and carry output, respectively. The z-transfer functions of Fig. 2 and Fig. 3 of unshaped and shaped ditherings are shown in (1) ~ (4).

$$Y_{MASH,unshaped}(z) = X(z) + D_n(z) + (1-z^{-1})^3 E(z) \quad (1)$$

$$Y_{SL,unshaped}(z) = z^{-3}(X(z) + D_n(z)) + (1-z^{-1})^3 E(z) \quad (2)$$

$$Y_{MASH,shaped}(z) = X(z) + (1-z^{-1})D_n(z) + (1-z^{-1})^3 E(z) \quad (3)$$

$$Y_{SL,shaped}(z) = z^{-3}X(z) + z^{-2}(1-z^{-1})D_n(z) + (1-z^{-1})^3 E(z) \quad (4)$$

As shown in Fig. 2 and Fig. 3, the quantization noise's most significant bit D_n is extracted and fed back to the C_i of 1st-stage for unshaped dithering. This 1-bit sequence introduces a noise level elevation whose power spectral density (PSD) is calculated with (5), where f_{clk} is clock frequency of the DDSM. To lower this noise, shaped dithering can be applied by feeding D_n into C_i of 2nd-stage.

$$S_{LSB} = 10 \times \log\left[\frac{2^{-2n}}{f_{clk}}\right] \quad (5)$$

It can be seen from Fig. 2 and Fig. 3 that not any extra circuits but only 1-bit wire is required in our proposal.

5. Simulations

MASH and single-loop modulators with proposed self-dithering are simulated with MATALB and Simulink. The DDSM's input bit width is 16, i.e. input values range from 0 to 65535. The number of stages of LFSR is 16. The power spectral density (PSD) of DDSM's output is calculated using FFT of Welch method with 65536-point hanning window and 50% overlapping [4], for which f_{clk} is 20 MHz. Thus, S_{LSB} equals -170 dB/Hz calculated from (5).

Fig. 4 shows the PSDs of a 3rd-order single-loop DDSMs with the input equal to 1024. Without dithering, tones are higher than the spectrums with LFSR-dithering and self-dithering. Unshaped ditherings elevate low-frequency noise levels both around -170 dB/Hz as same as S_{LSB}. As to shaped ditherings, entire spectrums of LFSR-dithering and self-dithering are equivalent.

Fig. 5 illustrates the PSDs of a 2nd-order MASH DDSM with the input equal to 64. Since there is no guaranteed shaped dithering scheme for 2nd-order DDSMs, unshaped dithering is applied. The results are compared with using LFSR and HK-MASH, a MASH DDSM with deterministic spur reduction [3]. We do not consider

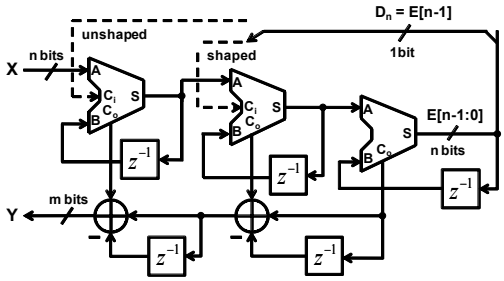

Fig. 2 Self-dithered 3rd-order MASH DDSM.

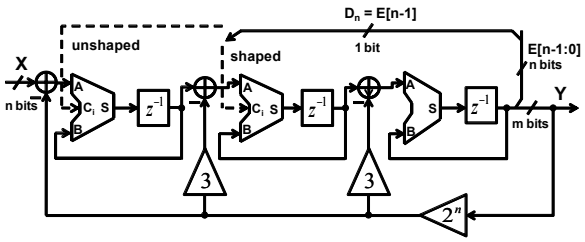

Fig. 3 Self-dithered 3rd-order single-loop DDSM.

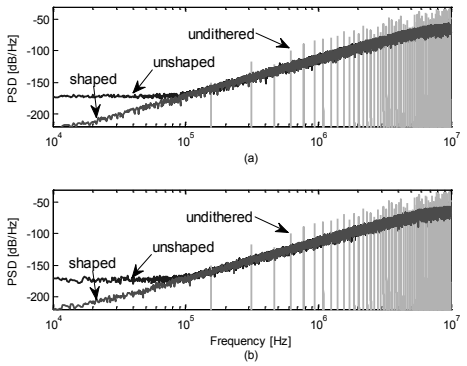

Fig. 4 PSDs of 3rd-order single-loop with undithering, (a) unshaped/shaped LFSR-dithering, and (b) unshaped/shaped self-dithering.

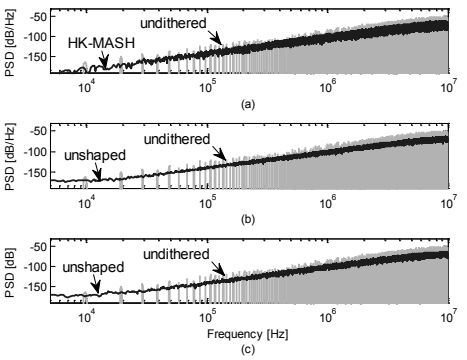

Fig. 5 PSDs of 2nd-order MASH with undithering, (a) HK_MASH, (b) unshaped LFSR-dithering, and (c) unshaped self-dithering.

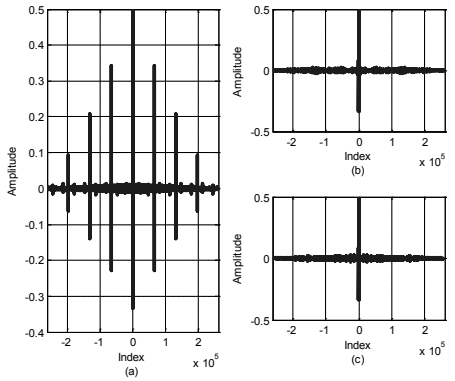

Fig. 6 Auto-correlations of 2nd-order (a) HK-MASH, LFSR-dithered MASH, and (c) self-dithered MASH DDSMs.

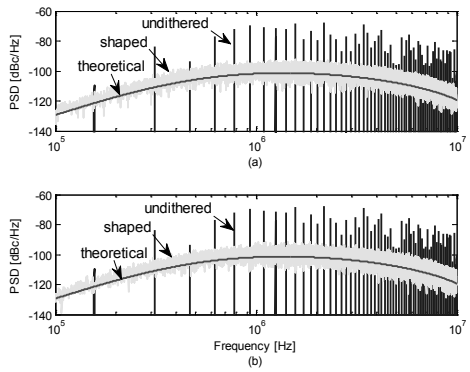

Fig. 7 Fractional-N PLL phase noises due to the quantization noises of 3rd-order single-loop DDSMs in theory, with undithering, (a) shaped LFSR-dithering, and (b) shaped self-dithering.

initial-condition method since it is ineffective for 2nd-order MASH according to [4]. Seen from Fig. 4, three methods all effectively suppress the spurs but HK-MASH's spectrum is "thicker" meaning that the noise floor is less whitened than the other two.

Fig. 6 shows the autocorrelations of 2nd-order MASH DDSM output under the same condition as in Fig. 5. Except for the spike at the center, the 1st spike's x-index represents the sequence length. In Fig. 6, no spikes are observed for LFSR-dithering and self-dithering so that their sequence lengths are longer than the number of simulation samples, 2^{18}, while for HK-MASH we obtain the sequence length as 65521, less than one fourth of 2^{18}. Table 1 summarizes characteristics of the 16-bit 2nd-order MASH DDSMs for three solutions.

Fig. 7 shows the PLL's phase noises attributed to the 3rd-order DDSM quantization. According to [6], PLL's phase noise due to the quantization noise is calculated from (6), where N, is divider's division ratio, G(s) is the open-loop transfer function, and S_{qn} is the PSD of the DDSM, theoretically defined in (7). DDSM spurious tones can be mapped to the PLL fractional spurs using (6). Our PLL loop is designed for a fast settling application used in a wireless sensor network with the spec of 5 μs settling time and -80 dBc/Hz spur level. To achieve the spec, we

Table 1 Summary of 16-bit 2nd-order MASH DDSMs

	Proposed	LFSR	HK-MASH
Input Range	0~65535	0~65535	1~65521
Mean Value Deviation (max)	$0.5/2^{16}$	$0.5/2^{16}$	$15/2^{16}$
Hardware Overhead	None	16 flip-flops + some logic gates	1 multiplexer + some flip-flops

set the loop bandwidth to 303 kHz. In Fig. 7, undithered DDSM contributes fractional spurs with maximum level of -68 dBc/Hz violating the spec. For each frequency bin, LFSR-dithering and self-dithering remove spurs, and the maximum noise powers are around -100 dBc/Hz. Also, two spectrums are both similar to the theoretical one calculated with (6). If we try to decrease the spur levels to below -100 dBc/Hz by decreasing the loop bandwidth to 72 kHz while maintaining the loop stability, the settling time drastically increases to around 20 μs, 4 times of the spec requirement. Therefore, shrinking the loop bandwidth is ineffective; instead, dithered DDSMs are necessary.

$$\Gamma_{\Delta\Sigma,div} = S_{qn} \cdot \frac{(2\pi)^2}{\left|1-z^{-1}\right|^2} \cdot \frac{1}{N^2} \cdot \left| N \cdot \frac{G(s)}{1+G(s)} \right|^2 \tag{6}$$

$$S_{qn} = \left|E(z) \cdot NTF(z)\right|^2 = \frac{1}{12 f_{ref}} \cdot \left|NTF(z)\right|^2 \tag{7}$$

6. Implementations and Experimental Results

The test element group (TEG) of 3rd-order 16-bit MASH and single-loop DDSMs has been implemented with 0.18um CMOS process. The TEG also includes a 16-stage LFSR, a 41-bit shift register, and some control logic.

Fig. 8 shows the TEG's block diagram and its data flow. The DDSM's input and the control bits are serially shifted into the TEG. Control bits and control logic enable one DDSM, set its input and dithering scheme which is either LFSR-dithering or self-dithering. The 4-bit output of the enabled DDSM is output in parallel and recorded by an external controller for spectrum plotting. This design follows a typical digital IC design flow from RTL to chip integration. The power consumption estimated by Synopsis IC Compiler is 630 μW at 1.8V power supply and 26MHz operating frequency.

Fig. 9 shows the die photo of the TEG. Its active area is 0.06 mm^2. Since the area of flip-flops is dominant, each block's area can be estimated with number of flip-flops. There are 48 in one DDSM, 16 in the LFSR, 41 in the shift register, and more than 32 in the control logic for the input and output data latching. Therefore, one DDSM occupies less than 0.02 mm^2 area. On the other hand, compared with LFSR-dithered DDSM, self-dithered DDSM reduces the area by 1/4 which is the portion of the 16-stage LFSR.

The TEG is mounted on VDEC-MOT48-160FP socket

board [7], and measured at the power supply of 3.3 V for IOs and 1.8 V for the core. An FPGA evaluation board XtremeDSP™ Starter Platform powered by Spartan®-3A DSP 1800A is employed as the external controller which provides the TEG with 41-bit serial data, reset signal, clocks, etc.. It transfers the DDSM's parallel output to PC via RS232 cable. These output data is processed by MATLAB programs on PC.
Fig. 10 and Fig. 11 show the PSDs of fabricated single-loop and MASH DDSMs. Equivalent performances can be observed by using LFSR-dithering and self-dithering.

7. Conclusion

Spur suppression techniques are important to fractional-N PLLs. Conventional LFSR-dithering and HK-MASH require extra hardware. We have proposed self-dithering method holding the equivalent performance of LFSR-dithering featuring no hardware overhead. Therefore, for a 16-bit DDSM with dithering, 1/4 area can be reduced by removing 16-stage LFSR circuits.

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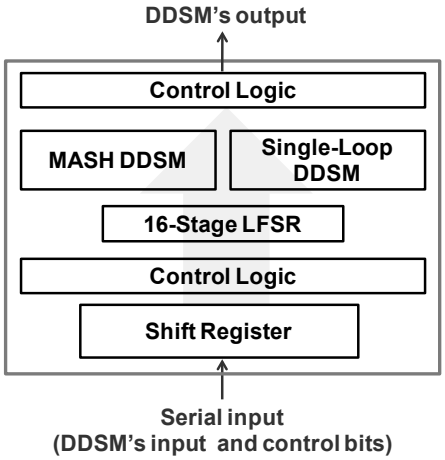

Fig. 8 DDSM TEG and data flow

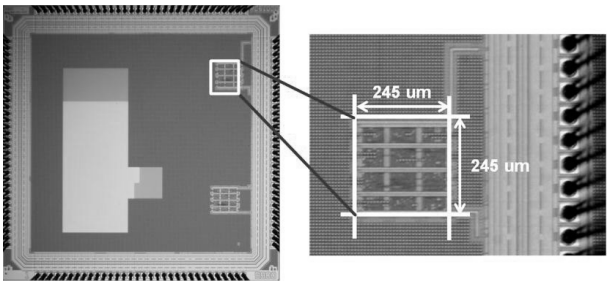

Fig. 9 Die photo of DDSM TEG

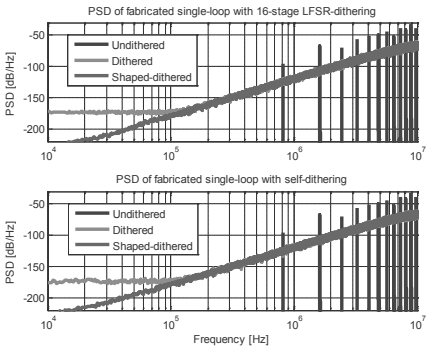

Fig. 10 PSDs of fabricated single-loop DDSM with undithering, shaped/unshaped LFSR-dithering, and shaped/unshaped self-dithering.

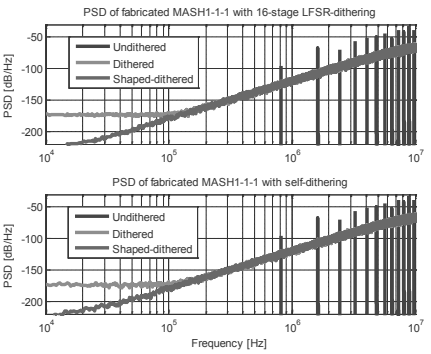

Fig. 11 PSDs of fabricated MASH DDSM with undithering, shaped/unshaped LFSR-dithering, and shaped/unshaped self-dithering.